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TM 11-6625-3062-14

TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL

SIGNAL GENERATOR
HEWLETT-PACKARD MODEL 8656A

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HEADQUARTERS, DEPARTMENT OF THE ARMY
15 NOVEMBER 1985

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5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1 DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

2 IF POSSIBLE , TURN OFF THE ELECTRICAL POWER

3 IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL

4 SEND FOR HELP AS SOON AS POSSIBLE

5 AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

SAFETY CONSIDERATIONS

GENERAL – This is a Safety Class I instrument (provided with terminal for protective earthing).

OPERATION – BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNINGS

Servicing instructions are for use by qualified personnel only. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.

BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two conductor outlet is not sufficient protection.

If this instrument is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal is likely to make this instrument dangerous. Intentional interruption is prohibited.

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS

⚠	Instruction manual symbol: the apparatus will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the apparatus against damage.
ϟ	Indicates dangerous voltages.
⏚	Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).
WARNING	The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.
CAUTION	The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the equipment. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

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Technical Manual)
)
No. 11-6625-3062-14)

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 15 November 1985

OPERATOR'S ORGANIZATIONAL AND DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL

8656A
SIGNAL GENERATOR
0.1-990 MHz
(INCLUDING OPTIONS 001 AND 002)

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed 2035A.

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed 2032A, 2027A, 2026A, 2025A, 2024A, 2023A, 2022A, 2018A, 2014A, and 2009A.

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of this manual direct to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, NJ 07703-5007.

In either case, a reply will be furnished direct to you.

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A8 Frequency Multiplier Assembly	3	BD2
A9 Attenuator Assembly	7	BD2
A10 Audio/Power Supply Assembly		
Modulation and RF Amplitude Control	6	BD2
Attenuator Control	7	BD2
Frequency Modulation Control	12	BD3
Power Supply	22	BD1
A11 Microprocessor/Memory/ HP-IB Assembly		
Microprocessor, Interrupt Processing and Restart	14	BD4
Address Buffering and Decoding, Serial I/O and Control	15	BD4
Memory	16	BD4
HP-IB Interface	17	BD4
A12 Voltage Regulator Assembly	22	BD1
A13 HP-IB Connector Assembly	17	BD4
A14 Filter Bank Assembly	14, 22	—
A15 Line Power Module	22	BD1
A16 10 MHz Reference Oscillator Assembly (Option 001)	13, 22	BD3
A17 Front Feedthrough Assembly	6,18 19, 22	—

APPENDICES

APPENDIX A. REFERENCES A-1
B. COMPONENTS OF END ITEM LIST. B-1
C. ADDITIONAL AUTHORIZATION LIST(NOT APPLICABLE) . . .
D. MAINTENANCE ALLOCATION . . . D-1
E. EXPENDABLE SUPPLIES AND MATERIAL LIST(NOT APPLICABLE)
F. MANUAL CHANGES F-1

SECTION 0

INTRODUCTION

0-1. SCOPE

This manual describes Signal Generator, Hewlett-Packard Model 8656A and provides instructions for operation and maintenance.

0-2. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

0-3. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/ NAVMATINST 4355.73A/AFR 400-54/MCO 4430.3F.

c. Discrepancy in Shipment Report (DISREP)(SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP)(SF 361) as prescribed in AR 55-38/ NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

0-4. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)

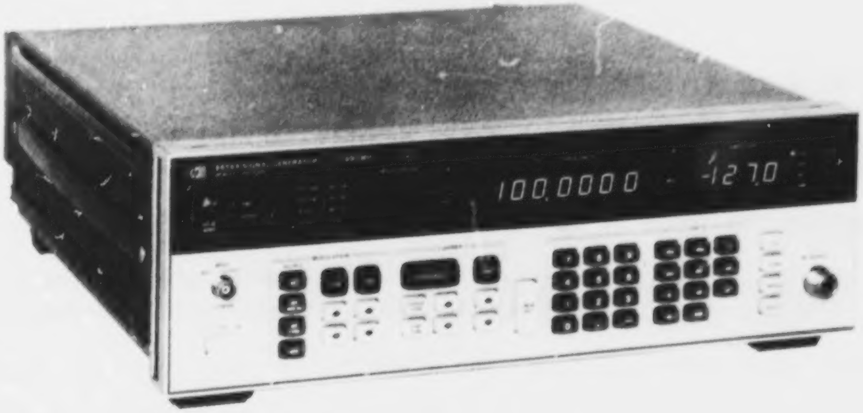
If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, NJ 07703-5007. We'll send you a reply.

0-5. ADMINISTRATIVE STORAGE

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts for storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage is covered in paragraph 2-14.

0-6. DESTRUCTION OF ARMY ELECTRONICS MATERIEL

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

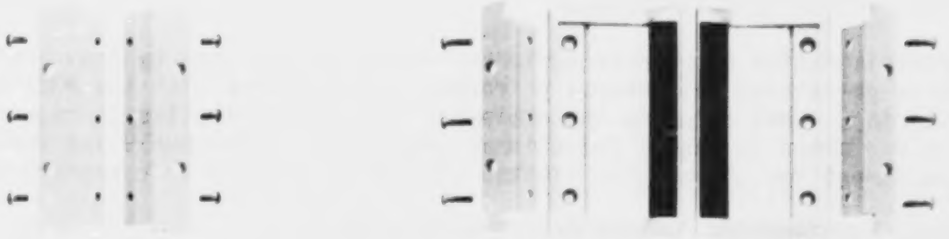


MODEL 8656A

LINE POWER CABLE

OPTION 001
TIME BASE CABLE

OPTION 907
FRONT HANDLE KIT



OPTION 908
RACK FLANGE KIT

OPTION 909
RACK FLANGE AND FRONT HANDLE
COMBINATION KIT

NOTE: Refer to ACCESSORIES SUPPLIED for more details.

Figure 1-1. HP Model 8656A Signal Generator with Option 001 and Accessories Supplied

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

This manual contains information required to install, operate, test, adjust, and service the Hewlett-Packard Model 8656A Signal Generator. The Model 8656A will generally be referred to as the Signal Generator throughout this manual. Figure 1-1 shows the Signal Generator with all of its externally supplied accessories. This manual also documents Signal Generators supplied with the high stability time base, Option 001 and rear panel connectors, Option 002.

This section of the manual describes the instruments documented by this manual and covers instrument description, options, accessories, specifications, and other basic information. The other sections contain the following information:

Section II, Installation: provides information about initial inspection, preparation for use (including time base selection and HP-IB address selection for remote operation), and storage and shipment.

Section III, Operation: provides information about panel features and includes operator's checks, operating instructions for both local and remote operation, and operator's maintenance information.

Section IV, Performance Tests: provides the information required to check performance of the instrument against the critical specifications listed in Table 1-1.

Section V, Adjustments: provides the information required to properly adjust the instrument.

Section VI, Replaceable Parts: provides ordering information for all replaceable parts and assemblies.

Section VII, Manual Changes: with the backdating information, this manual applies to all instruments as indicated on the title page.

Section VIII, Service: provides the information required to repair the instrument.

Two copies of the operating information are supplied with the Signal Generator. One copy is in the form of an Operating Manual. The Operating Manual is simply a copy of the first three sections of the Operating and Service Manual. The Operating Manual should stay with the instrument for use by the operator. Additional copies of the Operating Manual may be ordered separately through your nearest Hewlett-Packard office. Its part number is listed on the title page of this manual.

Also listed on the title page of this manual, below the manual part number, is a "Microfiche" part number. This number may be used to order 100 x 150 millimetre (4- x 6-inch) microfilm transparencies of this manual. Each microfiche contains up to 96 photo-duplicates of the manual's pages. The microfiche package also includes the latest MANUAL CHANGES supplement, as well as all pertinent Service Notes.

1-2. SPECIFICATIONS

Instrument specifications are listed in Table 1-1. These specifications are the performance standards or limits against which the instrument may be tested. Supplemental characteristics are listed in Table 1-2. Supplemental characteristics are not warranted specifications, but are typical characteristics included as additional information for the user.

1-3. SAFETY CONSIDERATIONS

This product is a Safety Class I instrument, that is, one provided with a protective earth terminal. The Signal Generator and all related documentation must be reviewed for familiarization with safety markings and instructions before operation. Refer to the Safety Considerations page found at the beginning of this manual for a summary of the safety information. Safety information pertinent to the task at hand, that is, installation, operation, performance testing, adjustment, or service is found throughout this manual.

1-4. INSTRUMENTS COVERED BY THIS MANUAL

This instrument has a two-part serial number in the form 0000A00000 which is stamped on the serial number plate attached to the rear of the instrument. The first four digits and the letter con-

INSTRUMENTS COVERED BY THIS MANUAL (Cont'd)

stitute the serial number prefix and the last five digits form the suffix. The prefix is the same for all identical instruments. It changes only when a change is made to the instrument. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply directly to instruments having the same serial number prefix(es) as listed under SERIAL NUMBERS on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates that the instrument is different from those documented in this manual. The manual for this newer instrument is accompanied by a yellow MANUAL CHANGES supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest MANUAL CHANGES supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard

For information concerning a serial number prefix that is not listed on the title page or in the MANUAL CHANGES supplement, contact your nearest Hewlett-Packard office.

1-5. DESCRIPTION

The Hewlett-Packard Model 8656A is a synthesized signal generator with a carrier frequency range of 100 kHz to 990 MHz. Its output amplitude is leveled and calibrated from +13 to −127 dBm. AM and/or FM functions can be individually selected. The carrier frequency, output amplitude, and modulation functions can be remotely programmed via the Hewlett-Packard Interface Bus. The unique modular design and incorporated service features permit rapid and easy calibration and service.

1-6. Carrier Frequency

The Signal Generator covers a carrier frequency range of 100 kHz to 990 MHz (10 kHz to 990 MHz with underrange) which can be extended to 1.8 GHz with an external doubler. Frequency resolution is 100 Hz or 250 Hz depending on the carrier frequency selected. An 8-digit LED display of the carrier frequency in MHz is provided. Pushbutton keys permit coarse tuning, fine tuning, and incrementing of the carrier frequency.

Frequency accuracy and stability are dependent on the reference source being used, either the internal 50 MHz reference oscillator or an external source that operates at 1, 5, or 10 MHz. An optional 10 MHz crystal reference is available for increased accuracy and stability.

1-7. Output Amplitude

The Signal Generator has precise power levels from +13 to −127 dBm (+1.00V to +0.100 μV) with overrange at decreased accuracy. The output amplitude from +13 to −127 dBm is accurate to less than or equal to ±1.5 dB from 100 kHz to 990 MHz. Level flatness is less than or equal to ±1.0 dB with an output amplitude setting of 0.0 dBm. Output amplitude resolution is 0.1 dB. A 3-1/2-digit LED display of output amplitude is provided with 7 LED annunciators used to display unit information. Easy conversion of units between dBm, μV, EMF, and so forth is possible.

1-8. Modulation Capabilities

The Signal Generator features a versatile internal and external modulation capability for AM and FM. This includes internal 400 Hz or 1 kHz tones; mixed modulation, such as AM/FM, AM/AM, or FM/FM; and the capability to accept low frequency digital unsquelching signals. A 2-digit display of AM depth or FM peak deviation frequencies is provided with 10 LED annunciators used to display internal or external modulation source information. Simple keyboard entries of AM depth up to 99% with a resolution of 1% and FM peak deviation frequencies up to 99 kHz with resolutions of 100 Hz (for deviations less than 10 kHz) or 1 kHz (for deviations greater than or equal to 10 kHz) are possible.

1-9. OPTIONS

The following options are available and may have been ordered and received with the Signal Generator. If they were not received with the original shipment and are now desired, except for option

OPTIONS (Cont'd)

002, they may be ordered from your nearest Hewlett-Packard office using the part number included in each of the following paragraphs.

1-10. Electrical Options

Option 001 provides a 10 MHz crystal reference for increased frequency accuracy and stability. Order HP part number 08656-60079.

1-11. Mechanical Options

The mechanical options except Option 002 are shown in Figure 1-1.

Rear Panel Inputs and Outputs Option 002. RF Output and Modulation Input/Output Connectors are located on the rear panel. The SEQ (sequencing) input is eliminated.

Front Handle Kit Option 907. Ease of handling is increased with the front panel handles. Order HP part number 5061-0089.

Rack Flange Kit Option 908. This kit contains all necessary hardware and installation instructions for mounting the Signal Generator in a rack with 482.5 millimeter (standard 19-inch) spacing. Order HP part number 5061-0077.

Rack Flange and Front Handle Combination Kit Option 909. This kit is not simply a front handle kit and rack flange kit packaged together. The combination is made up of unique parts which include both functions. Order HP part number 5061-0083.

1-12. HEWLETT-PACKARD INTERFACE BUS

HP-IB*

1-13. Compatibility

The Signal Generator has an HP-IB interface and can be used with any HP-IB computing controller or computer for automatic system applications. The Signal Generator is fully programmable via the HP Interface Bus. The Signal Generator's complete compatibility with HP-IB is defined by the following list of interface functions: SH0, AH1, T0, L2, SR0, RL1, PP0, DC1, DT0, and C0. The Signal Generator interfaces with the bus via open-collector TTL circuitry. An explanation of the compatibility codes can be found in the IEEE Standard 488 and the identical ANSI Standard MC1.1.

For more detailed information relating to programmable control of the Signal Generator, refer to Remote Operation, Hewlett-Packard Interface Bus in Section III of this manual.

1-14 Selecting the HP-IB Address

Five miniature HP-IB address switches are located inside the Signal Generator. These switches represent a five-bit binary number (00 through 31 in decimal). HP-IB addresses greater than 30 (decimal) are invalid. When the instrument is shipped from the factory, the HP-IB address is preset to 07 (decimal). To determine the Signal Generator's HP-IB address, refer to HP-IB Address Display in Section III of this manual. To change the HP-IB address, refer to paragraph 2-8, HP-IB Address Selection.

1-15. ACCESSORIES SUPPLIED

The accessories supplied with the Signal Generator are shown in Figure 1-1. The power cable and fuse supplied are selected at the factory according to the Mains voltage available in the country of destination. For the part numbers of the power cables and Mains plugs available, refer to paragraph 2-6, Power Cables. For the part numbers and ratings of the fuses available, refer to paragraph 2-5, Line Voltage and Fuse Selection. If the Signal Generator is equipped with Option 001, a coaxial time base cable is supplied. This cable must be connected between the rear panel TIME BASE HIGH STABILITY OPTION connector and the TIME BASE INPUT connector.

1-16 RECOMMENDED TEST EQUIPMENT

Table 1-3 lists the test equipment required for testing, adjusting, and servicing the Signal Generator. The Critical Specifications column describes the essential requirements for each piece of test equipment. Other equipment can be substituted if it meets or exceeds these critical specifications.

The Recommended Model column may suggest more than one model. The first model listed is usually the least expensive, single-purpose model. Alternate models are suggested for additional features that would make them a better choice in some applications. For example, reasons for recommending an alternate model might be:

- HP-IB programmablility

  — or —
- Multi-function capability (that is, one model can replace two or more single-purpose models)

Table 1-4 presents the advantages of the alternate suggestions.

---

* HP-IB Systems Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

Table 1-1. Specifications (1 of 3)

Electrical Characteristics	Performance Limits	Conditions
FREQUENCY		
Range	100 kHz to 990 MHz	
Resolution	100 Hz 250 Hz	
SPECTRAL PURITY		
Spurious Signals:		
Harmonics	<-30 dBc	≤+7 dBm output levels
Non-harmonics	<-60 dBc	>5 kHz from carrier in CW mode
Sub-harmonics	None	
Residual Modulation CW Mode:		
AM (0.05 to 15 kHz Post Detection Noise Bandwidth)	<-70 dBc	0.1 to 990 MHz
FM (0.3 to 3 kHz Post Detection Noise Bandwidth)	<15 Hz rms	0.1 to 123.5 MHz
	<3 Hz rms	123.5 to 247 MHz
	<6 Hz rms	247 to 494 MHz
	<15 Hz rms	494 to 990 MHz
FM (0.05 to 15 kHz Post Detection Noise Bandwidth)	<30 Hz	0.1 to 123.5 MHz
	<8 Hz	123.5 to 247 MHz
	<16 Hz	247 to 494 MHz
	<30 Hz	494 to 990 MHz
OUTPUT		
Level Range	+13 dBm to -127 dBm	Into 50 ohms
Resolution	0.1 dB	
Absolute Level Accuracy[1]	≤±1.5 dB	Output levels of +13 dBm to -127 dBm; frequencies from 100 kHz to 990 MHz
Level Flatness	≤±1.0 dB	Output level setting of 0.0 dBm; frequencies from 100 kHz to 990 MHz
AMPLITUDE MODULATION		
Depth[2]	0 to 99%	Output levels of +7 dBm and below; frequencies from 100 kHz to 990 MHz
	0 to 30%	Output levels of +10 dBm and below; frequencies from 100 kHz to 990 MHz
Resolution	1%	
Incidental Phase Modulation	<0.3 radian peak	30% AM depth and internal rates

[1] Absolute level accuracy includes allowances for detector linearity, temperature, flatness, attenuator accuracy, and measurement error.

[2] AM depth is further limited by the Indicator Accuracy specification.

Table 1-1. Specifications (2 of 3)

Electrical Characteristics	Performance Limits	Conditions
AMPLITUDE MODULATION (Cont'd)		
Indicator Accuracy[2]	±2% (±4% of reading)	Depths <90% and internal rates
AM Rates:		
Internal	400 and 1 kHz, ±3%	
External	25 Hz to 25 kHz	1 dB bandwidth, ac coupled
AM Distortion (internal rates)	<1.5%	0 to 30% AM
	<3%	31 to 70% AM
	<5%	71 to 90% AM
FM MODULATION		
Maximum Peak Deviation (Δfpk):[3]		
Rates ≥60 Hz	99 kHz	0.1 to 123.5 MHz (fc)
	25 kHz	123.5 to 247 MHz (fc)
	50 kHz	247 to 494 MHz (fc)
	99 kHz	494 to 990 MHz (fc)
Rates <60 Hz	1600 x Rate	0.1 to 123.5 MHz (fc)
	400 x Rate	123.5 to 247 MHz (fc)
	800 x Rate	247 to 494 MHz (fc)
	1600 x Rate	494 to 990 MHz (fc)
		(FM not specified for fc — Δfpk <100 kHz)
Resolution	0.1 kHz	Deviations <10 kHz
	1 kHz	Deviations ≥10 kHz
Incidental AM	<0.1%	<20 kHz peak deviation and internal rates and carrier frequency ≥500 kHz.
Indicator Accuracy[3]	±5% of reading	At internal rates. Add ±5%, if 250 Hz frequency increments are used.
FM Distortion (Total Harmonic Distortion)	<0.5%	100 Hz to 99 kHz peak deviations and internal rates.
FM Rates:		
Internal	400 and 1 kHz, ±3%	
External	25 Hz to 25 kHz	1 dB bandwidth, ac coupled
GENERAL		
Operating Temperature Range	0 to 55°C	
Power Requirements Line Voltage	100, 120, 220, or 240 Vac, +5%, −10%	

[2] AM depth is further limited by the Indicator Accuracy specification.

[3] FM deviation is further limited by the Indicator Accuracy specification.

Table 1-1. Specifications (3 of 3)

Electrical Characteristics	Performance Limits	Conditions
GENERAL (Cont'd)		
Line Frequency	48 to 66 Hz	
Power Dissipation	125VA maximum	
Conducted and Radiated Electromagnetic Interference	MIL STD 461A, VDE 0871	Conducted and radiated interference is within the requirements of methods CE03 and RE02 of MIL STD 461A, VDE 0871, and CISPR Publication 11.
	<1.0 μV	Induced in a two-turn 2.5 cm (1 inch) diameter loop held 2.5 cm (1 inch) away from the front surface.
Net Weight	18.1 kg (40 lb)	
Dimensions (Full Envelope):		
Height	133 mm (5.25 in.) nominal	NOTE: For ordering cabinet accessories, the module sizes are 5-1/4H, 1MW, 17D.
Width	425 mm (16.75 in.) nominal	
Depth	520 mm (20.5 in.) nominal.	

Electrical Characteristics	Features
REMOTE OPERATION	
HP-IB (IEEE 488) Capability:	
Interface	Hewlett-Packard Interface Bus (HP-IB). HP-IB is Hewlett-Packard's implementation of IEEE Standard 488 (and the identical ANSI Standard MC1.1). The Signal Generator's compatibility with HP-IB is defined by the following list of interface functions: SH0, AH1, T0, L2, SR0, RL1, PP0, DC1, DT0, and C0.
Functions Controlled	All functions controlled from the front panel with the exception of DISPLAY, DISPLAY in conjunction with SEQ, Backspace, COARSE TUNE, FINE TUNE, and display HP-IB ADRS are programmable with the same accuracy and resolution as in local operation.

Table 1-2. Supplemental Characteristics

Supplemental characteristics are intended to provide information useful in applying the instrument by giving typical, but non-warranted performance parameters.

FREQUENCY

Accuracy and Stability: same as internal time base.

Time Base Characteristics:

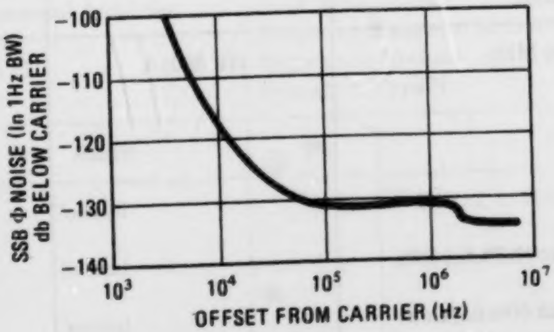
Characteristic	Standard Time Base	Option 001 Time Base
Aging Rate	±2 ppm/year	1×10^{-9}/day
Temperature	±10 ppm (0—55°C)	7×10^{-9} (0—55°C)
Line Voltage	—	2×10^{-9} (+5 to −10%)
Frequency	50 MHz	10 MHz
Time Base Reference Signal (Rear Panel)	Available at a level of >0.15 Vrms into 50 ohms (output of 10, 5 or 1 MHz is selectable via internal jumper). If the Option 001 or another external reference is used, only that reference frequency is available as an output.	
External Reference Input (Rear Panel)	Accepts any 10, 5 or 1 MHz (±0.002%) frequency standard at a level >0.15 Vrms into 50 ohms.	

Frequency Switching Speed: <2 seconds to be within 100 Hz of selected frequency.

SPECTRAL PURITY

SSB ϕ Noise (CW only):

Offset from Carrier	0.1 to 123.5 MHz (dBc/Hz)	123.5 to 247 MHz (dBc/Hz)	247 to 494 MHz (dBc/Hz)	494 to 990 MHz (dBc/Hz)
20 kHz	<−115	<−127	<−121	<−115
500 kHz	<−125	<−135	<−131	<−125



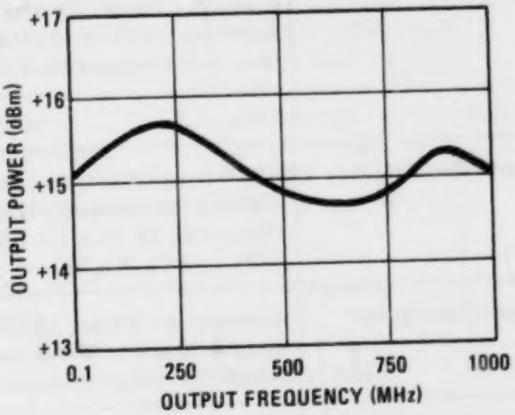
Typical SSB ϕ Noise, f_c = 450 MHz.

OUTPUT

SWR: <2, 0.1 to 990 MHz and <+13 dBm; < 1.5, 1.0 to 990 MHz and <−5 dBm.

Impedance: 50 ohms nominal.

Reverse Power Protection: protects Signal Generator from application of up to 50 watts of RF power to 990 MHz into RF OUTPUT connector; dc voltage cannot exceed 25V.



Typical maximum power output versus frequency (output set to +17 dBm).

MODULATION

(Amplitude and Frequency Modulation)

External Sensitivity: 1V peak for indicated accuracy. Front-panel annunciators indicate application of 1V peak signal ±5%.

External Modulation Input: front-panel BNC; ac-coupled, 600 ohms.

Modulating Signal Output: internal modulating signal is provided at the front-panel BNC connector at 1V peak, ±5% into 600-ohm resistive load.

Digital FM Modulation: will accept digital unsquelching signals. Sag of resultant demodulated signal is less than 8% at 1 kHz deviation for a 10 Hz square-wave modulating signal.

Simultaneous Modulation: internal and external AM and FM. Internal/external AM/FM, FM/AM, AM/AM, and FM/FM.

AM Incidental to FM: <1% for 200 kHz $\leq f_c <$ 500 kHz and <5% for 100 kHz $\leq f_c <$ 200 kHz.

Table 1-3. Recommended Test Equipment (1 of 3)

Instrument	Critical Specifications	Recommended Model	Use^1
AM/FM Test Source (required for modulation analyzer verification)	Range: 10 to 400 MHz Residual AM^2 FM Flatness: ±1% (dc to 250 kHz) Peak Deviation: to 100 kHz)	HP 11715A	P
Attenuator, Fixed	Attenuation: 20 dB Frequency Range: 10 MHz to 990 MHz SWR: <1.2	HP 8491A Option 020	A
Attenuator, Fixed	Attenuation: 60 dB Frequency Range: 100 kHz to 990 MHz Accuracy: ±2 dB ±0.16 dB at Standards Calibration Lab, Frequencies of 10, 100, 201, 801, 901, and 990 MHz. SWR: <1.3	HP 8491A Option H56	P
Controller, HP-IB	HP-IB compatibility as defined by IEEE Standard 488 and the identical ANSI Standard MC1.1: SH0, AH1, T4, TE0, L0, LE0, SR0, RL0, PP0, DC0 DT0, and C1, 2, 3, 28.	HP 9825A/98034A/ 98213A or HP 9835A/ 98332A/98034A (see Table 1-4)	A, T
Digital Multimeter	Accuracy: 4-1/2 digit, ±0.02% of reading ±1 digit Ranges: 20 mV to 30 Vdc and 2 Vac Sensitivity: 100 μV	HP 3465A or HP 3455A (see Table 1-4)	P, A, T
Distortion Analyzer	Distortion Range: <0.1% Range: 25 Hz to 25 kHz	HP 339A or HP 8903A (see Table 1-4)	P, T
Frequency Counter	Range: 10 MHz Resolution: 1 Hz	HP 5328A Option 031 or HP 5328A Options 001 and 031 (see Table 1-4)	A
Frequency Counter	Range: 990 MHz Resolution: 10 Hz	HP 5328A Option 031	T
Loop Antenna 2.5 cm (1 in.)	To ensure measurement accuracy, no substitution is possible. Fabrication depends upon machining and assembling to close tolerances.	HP 008640-60501	P
Modulation Analyzer	Frequency Range: 150 kHz to 990 MHz Input Level: −20 to +13 dBm Amplitude Modulation: Rates^3: 25 Hz to 25 kHz Depth: to 99% Accuracy: ±2% at 1 kHz Flatness: ±0.5% Demodulated Output Distortion: (0.3% for 50% depth; <0.6% for 90% depth Incidental ΦM: <0.05 radians for 50% depth at 1 kHz rate (50 Hz to 3 kHz bandwidth) Residual AM^2	HP 8901A	P, A

Table 1-3. Recommended Test Equipment (2 of 3)

Instrument	Critical Specifications	Recommended Model	Use[1]
Modulation Analyzer (Cont'd)	Frequency Modulation: Rates: 25 Hz to 25 kHz Deviation: to 99 kHz Accuracy: ±2% at 1 kHz Demodulated Output Distortion: <0.3% Incidental AM[3]: Residual FM: <8 Hz rms at 1300 decreasing linearly with frequency to <1 Hz rms for 100 MHz and below (50 Hz to 3 kHz bandwidth).		
Oscilloscope	Vertical Sensitivity: 10 mV/div Bandwidth: 50 MHz	HP 1222A or HP 1801A/1820C/181A (see Table 1-4)	A, T
Power Meter and Sensor	Frequency Range: 100 kHz to 990 MHz Power Range: +17 to −25 dBm with HP 8482A Frequency Range: 10 to 990 MHz Power Range: −20 to −60 dBm with HP 8484A Accuracy: ±0.2 dB	HP 436A or HP 436A Option 022 with HP 8484A and HP 8484A (see Table 1-4)	P, A, T
Signal Source	Frequency: 50 to 300 MHz Level: −20 dBm	HP 8640B	A, T
Signature Analyzer	Provides perferred method for troubleshooting digital circuitry.	HP 5004A	T
Spectrum Analyzer, RF	Frequency Range: 0.1 to 990 MHz Resolution Bandwidth: <1 kHz to 3 kHz	HP 8568A or HP 8558B/P/181T or (see Table 1-4)	P, A, T
Spectrum Analyzer, RF	Frequency: 10 to 990 MHz Resolution Bandwidth: <100 kHz Video Average: 25 Sweeps	Model 8568A	P, A, T
Test Oscillator	Level: 0.0 to 1 Vpk into 50 and 600 ohms Frequency: 25 Hz to 25 MHz	HP 651B	P, T
Wideband Amplifier	Gain: 20 or greater Frequency Range: 10 MHz to 990 MHz Impedance: 50 ohms Connector: Type N	HP 8447D Option 010	P

Adapter	Qty.	Type	Recommended Model	Use[1]
Coaxial	1	BNC(f) to BNC(f)	HP 1250-0080	A, T
Coaxial	1	N(f) to BNC(m)	HP 1250-0077	A
Coaxial	3	N(m) to BNC(f)	HP 1250-0780	P, A, T
Probe	2	SMC(f) to RF Test Point	HP 1250-1598	A, T

Table 1-3. Recommended Test Equipment (3 of 3)

Cable	Qty.	Type	Recommended Model	Use[1]
RF	2	BNC(f) to BNC(f)	HP 08662-60080	P
RF	1	Connector: UG-210/U Type N(m)	HP 11500A	P, A, T
RF	2	Connector: UG-210/U Type N(m)	HP 11500B	P, A, T

[1] A = Adjustments; P = Performance Tests; T = Troubleshooting.

[2] The residual AM specification of both the HP 8901A Modulation Analyzer and HP 11715A AM/FM Test Source are stated in a 50 Hz to 3 kHz bandwidth. In order to assure the validity of the residual AM measurement in the bandwidths stated for the HP 8656A Signal Generator (namely, 50 Hz to 15 kHz) the combined performance of both the HP 8901A and HP 11715A must be verified to be better than 0.022% rms for the 50 Hz to 15 kHz bandwidth. See paragraph 4-7, step 4, for the verification procedure.

[3] The incidental AM specification of the Signal Generator is not equivalent to the published specification of the Model 8901A Modulation Analyzer. In order to assure the validity of the incidental AM measurement, the incidental AM of the modulation analyzer must be verified to be less than 0.02% for the 300 Hz to 3 kHz bandwidth and 20 kHz peak deviation at internal rates. Refer to paragraph 4-10, step 18, for the verification procedures.

Table 1-4. Alternate Test Equipment

Instrument	Recommended Model	Suggested Alternative	Advantages of Alternative
Controller, HP-IB	HP 9825A/98213A/ 98034A	HP 9835A/98332A/ 98034A	CRT Display HP Enhanced BASIC Larger Memory
Digital Voltmeter (DVM)	HP 3465A	HP 3455A	HP-IB* Compatible
Distortion Analyzer	HP 339A	HP 8903A	HP-IB* Compatible
Frequency Counter	HP 5328A Option 031	HP 5328A Options 001 and 031	HP-IB* Compatible
Power Meter	HP 436A	HP 436A Option 022	HP-IB* Compatible
Oscilloscope	HP 1222A	HP 1801A/1820C/ 181A	Satisfies all requirements for testing the Signal Generator. Also has increased vertical sensitivity (0.05 mV/div) and a Persistance Display that makes it possible to troubleshoot the Low Frequency Loop circuits.
Spectrum Analyzer, RF	HP 8568A	HP 8558B/P/181T or HP 8554B/8552B/ 141T	Satisfies most of the requirements for testing the Signal Generator. The exception is the Low Level Accuracy test. In this case, the spectrum analyzer's noise level is high enough that the measurements are meaningless.

*HP-IB is Hewlett-Packard's implementation of IEEE Standard 488 and the identical ANSI Standard MC1.1.

SECTION II
INSTALLATION

2-1. INTRODUCTION

This section provides the information needed to install the Signal Generator. Included is information pertinent to initial inspection, power requirements, line voltage and fuse selection, power cables, time base selection, HP-IB address selection, interconnection, mating connectors, operating environment, instrument mounting, storage, and shipment.

2-2. INITIAL INSPECTION

WARNING

To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the outer enclosure (covers and panels).

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as shown in Figure 1-1. Procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the electrical performance test, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for the carrier's inspection.

2-3. PREPARATION FOR USE

2-4. Power Requirements

WARNING

To avoid the possibility of hazardous electrical shock, do not operate this instrument at line voltages greater than 126.5 Vac with line frequencies greater than 66 Hz. Leakage currents at these settings may exceed 3.5 mA.

The Signal Generator requires a power source of 115 (90 to 126) Vac or 230 (198 to 252) Vac, 48 to 66 Hz single phase. Power consumption is 125 VA maximum.

WARNINGS

This is a Safety Class I product (i.e., provided with a protective earth terminal). An uninterruptible safety earth ground must be provided from the Mains power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an external autotransformer for voltage reduction, make sure that the common terminal is connected to the earthed pole of the power source.

2-5. Line Voltage and Fuse Selection

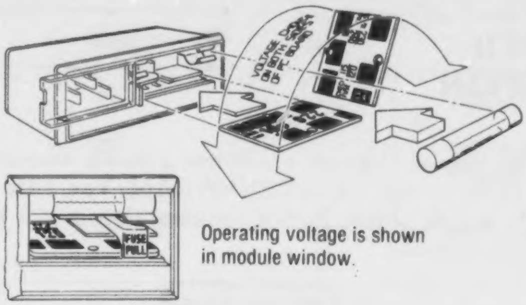
CAUTION

BEFORE PLUGGING THIS INSTRUMENT into the Mains (line) voltage, be sure the correct voltage and fuse have been selected.

A rear panel, line power module permits operation from 100, 120, 220, or 240 Vac. The number visible in the window (located on the module) indicates the nominal line voltage to which the instrument must be connected. Verify that the line voltage selection card and the fuse are matched to the power source. Refer to Figure 2-1, Line Voltage and Fuse Selection. Table 2-1 lists the ratings and HP part numbers for the replaceable fuses.

WARNING

For protection against fire hazard, the line fuse should only be a 250V slow blow fuse with the correct current rating.



Operating voltage is shown in module window.

SELECTION OF OPERATING VOLTAGE

1. Open cover door, pull the FUSE PULL lever and rotate to left. Remove the fuse.
2. Remove the Line Voltage Selection Card. Position the card so the line voltage appears at top-left corner. Push the card firmly into the slot.
3. Rotate the FUSE PULL lever to its normal position. Insert a fuse of the correct value in the holder. Close the cover door.

WARNING

To avoid the possibility of hazardous electrical shock, do not operate this instrument at line voltages greater than 126.5 Vac with line frequencies greater than 66 Hz (leakage currents at these line settings may exceed 3.5 mA).

Figure 2-1. Line Voltage and Fuse Selection

Table 2-1. Line Fuse Ratings and Part Numbers

Line Voltage	Rating	Part Number
100/120V	1.25A, 250V, SLO-BLO	HP 2110-0305
220/240V	0.6A, 250V, SLO-BLO	HP 2110-0016

2-6. Power Cables

WARNING

BEFORE CONNECTING THIS INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (Mains) power cord. The Mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.

This instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle, this cable grounds the instrument cabinet. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to Figure 2-2 for the part numbers of the power cables and Mains plugs available.

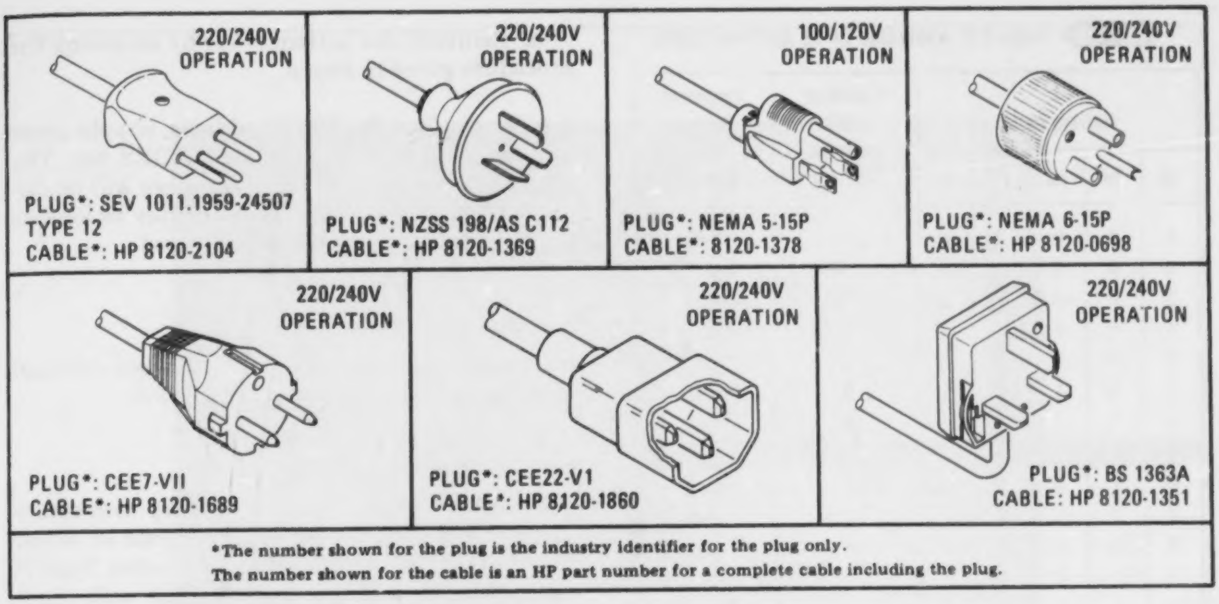
2-7. Time Base Selection

One of three time base output signals (1, 5, or 10 MHz at a level greater than 0.15 Vrms into 50 ohms) is accessible at the rear panel TIME BASE OUTPUT connector. This output signal is derived from the internal reference oscillator frequency and is jumper-selectable through an inductor located inside the Signal Generator on the Low Frequency Loop Assembly — A3. When the instrument is shipped from the factory, the inductive-jumper is hard-wired to provide a 10 MHz time base output signal. If the Option 001 or another external 10 MHz reference is applied to the rear panel TIME BASE INPUT connector, only that reference frequency will be available as an output signal. Also, if either a 1 or 5 MHz output signal is desired, the internal inductive-jumper will have to be repositioned. Similarly, if an external 1 or 5 MHz reference input is to be applied to the rear panel TIME BASE INPUT connector, the inductive-jumper will have to be repositioned to the position that corresponds to the frequency of the external reference input. The top cover of the Signal Generator will have to be removed to gain access to the time base jumper. The following procedure describes how to change the location of the inductive-jumper.

a. Remove the top cover from the Signal Generator by first removing the two screws used to secure the strap handle to each side of the instrument. Next, remove the front and rear caps, slide the side cover in the direction of the arrow, then lift the side cover away from the frame. Finally, lift the top cover away from the frame.

b. Locate the time base jumper on the Low Frequency Loop Assembly — A3 (see Figure 2-3).

c. Unsolder one end of the inductive-jumper and resolder it in the position that corresponds to the desired time base output or to the external reference input.


220/240V OPERATION
PLUG*: SEV 1011.1959-24507 TYPE 12
CABLE*: HP 8120-2104
220/240V OPERATION
PLUG*: NZSS 198/AS C112
CABLE*: HP 8120-1369
100/120V OPERATION
PLUG*: NEMA 5-15P
CABLE*: 8120-1378
220/240V OPERATION
PLUG*: NEMA 6-15P
CABLE*: HP 8120-0698
220/240V OPERATION
PLUG*: CEE7-VII
CABLE*: HP 8120-1689
220/240V OPERATION
PLUG*: CEE22-V1
CABLE*: HP 8120-1860
220/240V OPERATION
PLUG*: BS 1363A
CABLE: HP 8120-1351

*The number shown for the plug is the industry identifier for the plug only.
The number shown for the cable is an HP part number for a complete cable including the plug.

Figure 2-2. Power Cable and Mains Plug Part Numbers

Time Base Selection (Cont'd)

d. Reinstall the top cover by reversing the procedure given in step a.

e. If the Signal Generator is equipped with Option 001, ensure that the coaxial time base cable (A16W2) is connected between the rear panel TIME BASE HIGH STABILITY OPTION connector and the TIME BASE INPUT connector.

2-8. HP-IB Address Selection HP-IB

The Signal Generator is strictly a listener, never a talker, and therefore only its HP-IB (listen) address can be selected. This HP-IB address is switch-selectable through five miniature rocker-switches located inside the Signal Generator on the Microprocessor/Memory/HP-IB Assembly — A11. These switches provide the means to select one of 31 valid HP-IB addresses (00 through 30). HP-IB addresses greater than 30 (decimal) are invalid. Refer to Table 2-2 for the allowable HP-IB address codes. Listed are the valid address switch settings and the equivalent ASCII character and decimal value. When the instrument is shipped from the factory, the HP-IB address is preset to 07 (decimal). (In binary, this is 00111; the ASCII equivalent character is an apostrophe.) This preset address is shown shaded in Table 2-2. The bottom cover of the Signal Generator will have to be removed to gain access to the HP-IB switches. The following procedure describes how to change the settings of the HP-IB address switches.

NOTE

The HP-IB address stored in memory will only change when the instrument is powered up or reset. Therefore, the instrument must be unplugged or reset once the settings of the HP-IB address switches have been changed, otherwise, the stored HP-IB address will remain unchanged.

a. Remove the bottom cover from the Signal Generator by first removing the two screws used to secure the strap handle to each side of the instrument. Next, remove the front and rear caps, slide the cover in the direction of the arrow, then lift the side cover away from the frame. Finally, lift the bottom cover away from the frame.

b. Locate the HP-IB address switches S3 and S4 on the Microprocessor/Memory/ HP-IB Assembly — A11 (see Figure 2-4).

c. Use a pencil to set the switches to the desired HP-IB address in binary (see Figure 2-4). The five switches are labeled A1 through A5, where A1 is the least significant address bit and A5 is the most

HP-IB Table 2-2. Allowable HP-IB Address Codes

Address Switch					Equivalent ASCII Character (LISTEN)	Equivalent Decimal Value (LISTEN)
A5	A4	A3	A2	A1		
0	0	0	0	0	SP	00
0	0	0	0	1	!	01
0	0	0	1	0	"	02
0	0	0	1	1	#	03
0	0	1	0	0	$	04
0	0	1	0	1	%	05
0	0	1	1	0	&	06
0	0	1	1	1	'	07
0	1	0	0	0	(	08
0	1	0	0	1	)	09
0	1	0	1	0	*	10
0	1	0	1	1	+	11
0	1	1	0	0	,	12
0	1	1	0	1	-	13
0	1	1	1	0	.	14
0	1	1	1	1	/	15
1	0	0	0	0	0	16
1	0	0	0	1	1	17
1	0	0	1	0	2	18
1	0	0	1	1	3	19
1	0	1	0	0	4	20
1	0	1	0	1	5	21
1	0	1	1	0	6	22
1	0	1	1	1	7	23
1	1	0	0	0	8	24
1	1	0	0	1	9	25
1	1	0	1	0	:	26
1	1	0	1	1	;	27
1	1	1	0	0	<	28
1	1	1	0	1	=	29
1	1	1	1	0	>	30

▨ Indicates factory-set address.

HP-IB Address Selection HP-IB (Cont'd)
significant address bit. Pressing the right-hand side of the switch (as viewed from the front of the instrument) "sets" the corresponding address bit (bit=1), while pressing the left-hand side "clears" the bit (bit=0). Setting all of the address bits to "1" will result in an invalid HP-IB address (31 decimal). In this case, an HP-IB address of 30 (decimal) will be stored in memory once the instrument is powered up or reset.

d. Reinstall the bottom cover by reversing the procedure given in step a.

e. To confirm the HP-IB address, simply press and hold the front panel HP-IB ADRS key. The internally-set, decimal HP-IB address will be displayed in the MODULATION Display as long as the HP-IB ADRS key remains pressed.

2-9. Interconnection

Interconnection data for the Hewlett-Packard Interface Bus is provided in Figure 2-5.

2-10. Mating Connectors

Coaxial Connectors. Coaxial mating connectors used with the Signal Generator should be either 50-ohm BNC male connectors or 50-ohm Type N male connectors that are compatible with those specified in US MIL-C-39012.

Interface Connector. HP-IB mating connector is shown in Figure 2-5. Note that the two securing screws are metric.

2-11. Operating Environment

The operating environment should be within the following limitations:

Temperature .... 0°C to +55°C
Humidity .... <95% relative at 40°C
Altitude............... <4570 metres (15 000 feet)

2-12. Bench Operation

The instrument cabinet has plastic feet and fold-away tilt stands for convenience in bench operation. (The plastic feet are shaped to ensure self-alignment of instruments when they are stacked.) The tilt stands raise the front of the Signal Generator for easier viewing of the front panel.

2-13. Rack Mounting

WARNING

The Signal Generator weighs 18.1 kg (40 lb); therefore, care must be exercised when lifting to avoid personal injury. Use equipment slides when rack mounting.

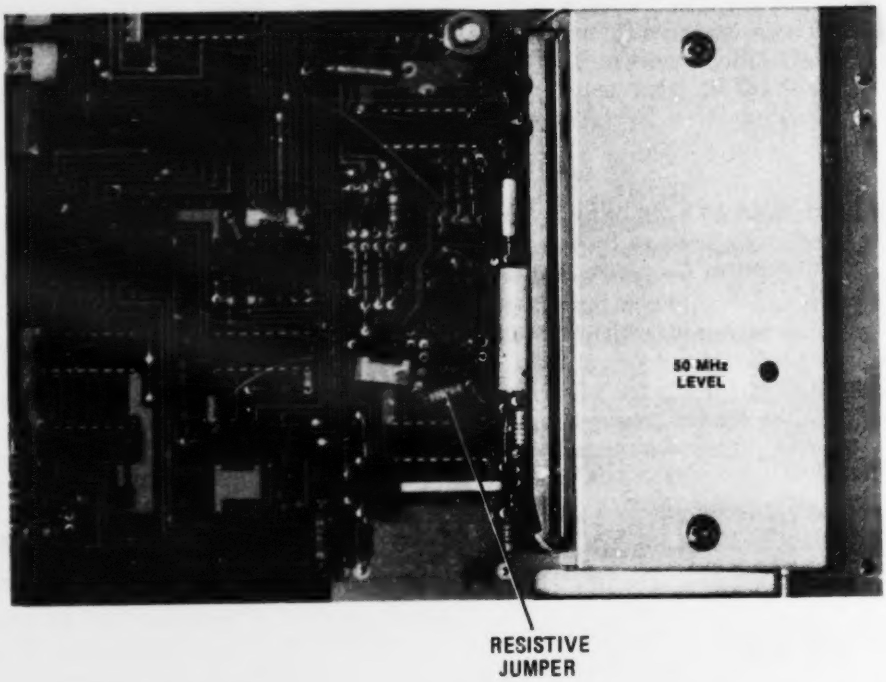
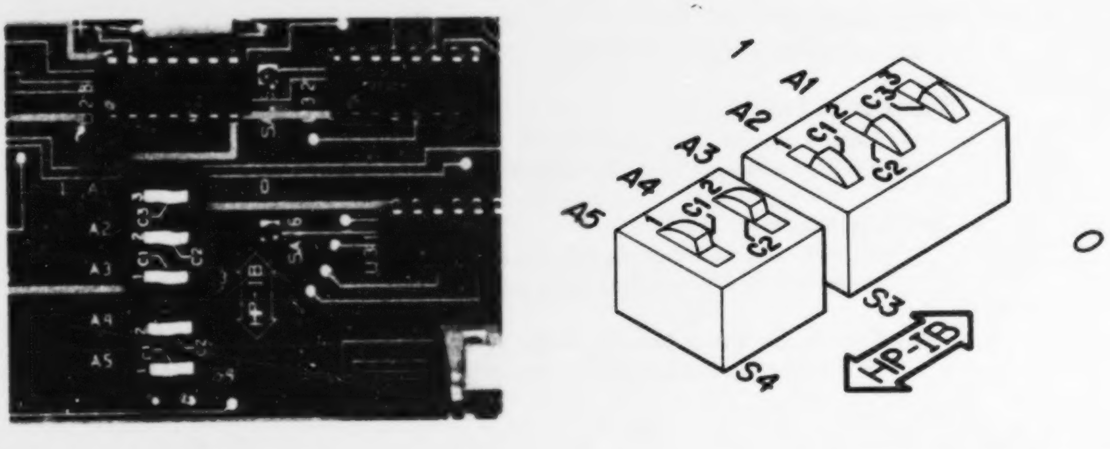
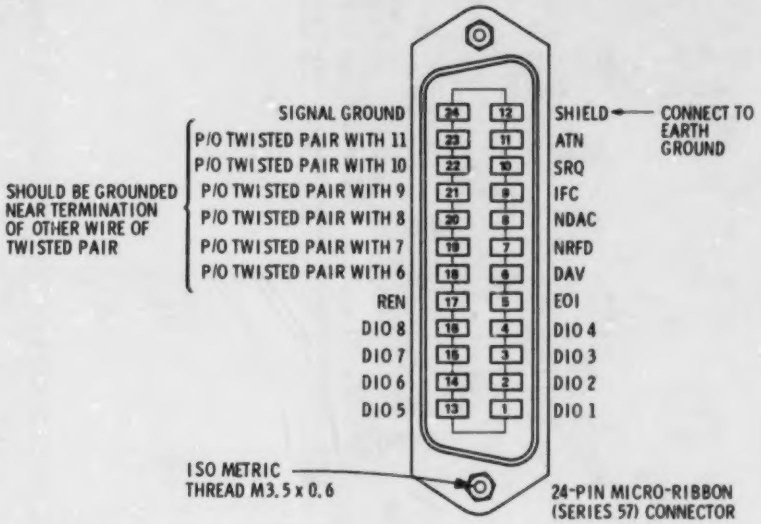

50 MHz
LEVEL
RESISTIVE
JUMPER

Figure 2-3. Time Base Jumper Location


1
A1
A2
A3
A4
A5
0
C1
C2
C3
S3
S4
HP-IB

HP-IB Figure 2-4. HP-IB Address Switch Location and Settings


SIGNAL GROUND
P/O TWISTED PAIR WITH 11
P/O TWISTED PAIR WITH 10
P/O TWISTED PAIR WITH 9
P/O TWISTED PAIR WITH 8
P/O TWISTED PAIR WITH 7
P/O TWISTED PAIR WITH 6
REN
DIO 8
DIO 7
DIO 6
DIO 5
SHOULD BE GROUNDED NEAR TERMINATION OF OTHER WIRE OF TWISTED PAIR
24 23 22 21 20 19 18 17 16 15 14 13
12 11 10 9 8 7 6 5 4 3 2 1
SHIELD
CONNECT TO EARTH GROUND
ATN
SRQ
IFC
NDAC
NRFD
DAV
EOI
DIO 4
DIO 3
DIO 2
DIO 1
ISO METRIC THREAD M3.5 x 0.6
24-PIN MICRO-RIBBON (SERIES 57) CONNECTOR

Logic Levels

The Hewlett-Packard Interface Bus Logic Levels are TTL compatible, i.e., the true (1) state is 0.0 Vdc to +0.4 Vdc and the false (0) state is +2.5 Vdc to +5.0 Vdc.

Programming and Output Data Format

Refer to Section III, Operation.

Mating Connector

HP 1251-0293; Amphenol 57-30240.

Mating Cables Available

HP 10833A, 1 metre (3.3 ft), HP 10833B, 2 metres (6.6 ft)
HP 10833C 4 metres (13.2 ft), HP 10833D, 0.5 metres (1.6 ft)

Cabling Restrictions

1. A Hewlett-Packard Interface Bus system may contain no more than 2 metres (6.6 ft) of connecting cable per instrument.

2. The maximum accumulative length of connecting cable for any Hewlett-Packard Interface Bus system is 20.0 metres (65.6 ft).

Figure 2-5. Hewlett-Packard Interface Bus Connections

Rack Mounting (Cont'd)

Rack mounting information is provided with the rack mounting kits. If a kit was not ordered with the Signal Generator as an option, it may be ordered through the nearest Hewlett-Packard office. Slide rack mount kits are discussed in the following paragraphs; refer to paragraph 1-11, Mechanical Options, in Section I for information and part numbers pertaining to other rack mount kits.

Slide rack mount kits allow the convenience of rack mounting with the flexibility of easy access. The slide kits for the Signal Generator are listed below.

Standard Slide Kit for HP rack enclosures	HP 1494-0018
Standard Tilt Slide Kit for HP rack enclosures	HP 1494-0025
Slide Adapter Bracket Kit for Standard Slides (for non HP rack enclosures)	HP 1494-0023

2-14. STORAGE AND SHIPMENT

2-15. Environment

The instrument should be stored in a clean, dry environment. The following environmental limitations apply to both storage and shipment.

Temperature	−55°C to +75°C
Humidity	<95% relative
Altitude	15 300 metres (50 000 feet)

2-16. Packaging

Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to assure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

Other Packaging. The following general instructions should be used for repackaging with commercially available materials.

a. Wrap the instrument in heavy paper or plastic. (If shipping to a Hewlett-Packard office or service center, attach a tag indicating the type of service required, return address, model number, and full serial number).

b. Use a strong shipping container. A double-wall carton made of 2.4 MPa (350 psi) test material is adequate.

c. Use enough shock-absorbing material (75 to 100 millimetre layer; 3 to 4 inches) around all sides of the instrument to provide a firm cushion and to prevent movement in the container. Protect the front panel with cardboard.

d. Seal the shipping container securely.

e. Mark the shipping container FRAGILE to assure careful handling.

SECTION III
OPERATION

3-1. INTRODUCTION

This section provides complete operating information for the Signal Generator. Included are both general and detailed operating instructions; detailed descriptions of each front and rear panel key, connector, switch, and display; information on remote operation; operator's checks; and operator's maintenance procedures.

3-2. Operating Characteristics

Table 3-2 briefly summarizes the major operating characteristics of the Signal Generator. This table is not intended to be an in-depth listing of all characteristics. For more detailed information on the Signal Generator's characteristics, refer to Table 1-1, Specifications and Table 1-2, Supplemental Characteristics. For information on the instrument's HP-IB capabilities, refer to the summary contained in Table 3-4, HP-IB Message Reference Table.

3-3. Local Operation

Information covering front panel operation of the Signal Generator is presented in five areas of this section, namely Simplified Front Panel Features, Simplified Operation, General Operating Instructions, Detailed Panel Features, and Detailed Operating Instructions.

Simplified Front Panel Features. Figure 3-1 on the backside of this foldout illustrates the front panel of the Signal Generator and provides simplified descriptions of each key, connector, switch, and display. In addition, references are provided to the more detailed descriptions.

Simplified Operation. The instructions on the backside of this foldout provide a quick introduction to front panel operation of the Signal Generator. These instructions are designed to rapidly acquaint the novice user with the basic operation of the instrument. Included are instructions for setting carrier functions, setting modulation functions, and changing parameter values. This is a good starting point for the first-time user. Table 3-3 provides an index (in functional order) to the detailed operating instructions. This index is intended to direct the user to the more complete operating instructions which are arranged alphabetically at the end of this section.

General Operating Instructions. Instructions relating to the Signal Generator's power-on procedure, power-on sequence, various keystroke sequences, and time base selection are presented to acquaint the user with the general operation of the instrument.

Detailed Panel Features. Front and rear panel features are described in detail in Figures 3-2 through 3-7.

Detailed Operating Instructions. The detailed operating instructions present the most comprehensive information about all of the Signal Generator's functions. These instructions are arranged alphabetically by subject and are included at the end of this section for easy reference. They are indexed in functional order in Table 3-3.

3-4. Remote Operation HP-IB

The Signal Generator is capable of remote operation via the Hewlett-Packard Interface Bus. Knowledge of local operation is essential for HP-IB programming since most of the data messages contain the same keystroke-like sequences. HP-IB information is presented in the following areas of this section:

a. General HP-IB information begins with paragraph 3-17.

b. A summary of HP-IB capabilities is provided in Table 3-4.

c. A summary of program codes is provided in Tables 3-8 and 3-9.

d. Detailed information relating to the Signal Generator's HP-IB programmable features together with tables and examples of associated program codes are presented in the detailed operating instructions which are arranged alphabetically at the end of this section.

3-5. Operator's Checks

Operator's checks are simple procedures designed to verify that the main functions of the Signal

Generator operate properly. Two procedures are provided, one for basic (front panel) functional checks and the other for HP-IB functional checks.

Basic Functional Checks. This procedure requires only a frequency counter, a spectrum analyzer, and the interconnecting cables and adapters. It provides assurance that most of the front panel controlled functions are being properly executed by the Signal Generator.

HP-IB Functional Checks. This series of procedures requires only an HP-IB compatible computing controller and an HP-IB interface with its interconnecting cable. These procedures assume that front panel operation has been previously verified, that is, that the basic functional checks have been previously performed. The procedures check all of the applicable bus messages summarized in Table 3-4.

3-6. Operator's Maintenance

The only maintenance that the operator should normally perform is the replacement of the primary power fuse. All other maintenance should be referred to qualified service personnel.

3-7. GENERAL OPERATING INSTRUCTIONS

WARNINGS

Before the Signal Generator is switched on, all protective earth terminals, extension cords, autotransformers, and devices connected to it should be connected to a protective earth grounded socket. Any interruption of the protective earth grounding will cause a potential shock hazard that could result in personal injury.

For continued protection against fire hazard, replace the line fuse, with only a 250V slo-blo fuse of the same rating. Do not use repaired fuses or short circuited fuseholders.

CAUTIONS

Before the Signal Generator is switched on, it must be set to the same line voltage as the power source or damage to the instrument may result.

The Signal Generator is protected against reverse power applications up to 50 watts; however, for greatest protection of expensive internal components be careful not to apply any reverse power to the RF OUTPUT connector.

3-8. Power-On Procedure

The Signal Generator has a standby state and an on state. Whenever the power cable is plugged in, the internal power supply is activated. If the instrument is equipped with the high stability reference (Option 001), the oven will be energized to keep the reference oscillator stable. If the Signal Generator is already plugged in, set the RESET/STBY/ON switch to ON. If the power cable is not plugged in, follow these instructions:

1. Check that the line voltage setting matches the power source. Refer to paragraph 2-5.
2. Check that the fuse rating is appropriate for the line voltage being used. Refer to paragraph 2-5.
3. Plug in the power cable.
4. Set the RESET/STBY/ON switch to ON.

3-9. Power-On Sequence

When the RESET/STBY/ON switch is set to ON after the instrument is first connected to Mains power or after it is reset, an internal memory check is initiated. This check tests for a failure in ROM (read-only memory) and in RAM (read-write memory). During this check, all front panel indicators will light for approximately 1.5 seconds to provide a quick visual inspection of each front panel annunciator and display segment. If a memory failure is detected, all front panel annunciators and display segments will remain lit until any front panel key is pressed. If the memory check was successful, the front panel indicators will display a carrier frequency of 100.0000 MHz, an output amplitude of −127.0 dBm, and no modulation. All annunciators (except dBm) will remain off. Table 3-1 lists the conditions of the Signal Generator as a result of a successful initialization sequence.

Table 3-1. Initialized Conditions

Parameter	Initialized Condition
Carrier Frequency	100.0000 MHz
Output Amplitude	−127.0 dBm
AM Depth	0%
FM Peak Deviation Frequency	0.0 kHz
Carrier Frequency Increment	10.0000 MHz
Output Amplitude Increment	10.0 dB
AM Depth Increment	1%
FM Peak Deviation Frequency Increment	1.0 kHz
Coarse and Fine Tune Pointer	10.0000 MHz
Sequence Counter	0
All 10 Internal Storage Registers	100.0000 MHz and −127.0 dBm with no modulation

3-10. Keystroke Sequences

The Signal Generator's functions can be selected in any order; however, each function selection requires a prescribed sequence of keystrokes. A keystroke sequence might contain only a single keystroke, such as, to read the internally-set, decimal HP-IB address or to return to local operation. More often though, the sequence will contain several keystrokes which must be entered in a specific order. This is true whenever one of the four main functions (Frequency, Amplitude, AM, or FM) is selected. Once one of these functions has been selected, the instrument will remain in that function until one of the following events occurs:

a. One of the three remaining functions is selected.

b. One of the STORE-RECALL-DISPLAY keys is pressed.

c. The instrument is reset or unplugged.

As long as a function remains in effect, it is not necessary to re-select that function before entering new data. The following paragraphs discuss multiple-entry keystroke sequences.

Carrier Keystroke Sequence. The parameters used to set the carrier's frequency and amplitude are entered in a Function-Data-Units format. Data entered following a function selection will be interpreted for that function. Data previously entered remains unaffected until the new data entry is terminated by pressing a valid unit key. If any other function key is pressed before the data entry is terminated, that entry will be rejected and the last valid display will be restored so that it agrees with the actual output of the Signal Generator.

Table 3-2. Operating Characteristics

Frequency

Range: 100 kHz to 990 MHz

Resolution: 100 Hz
250 Hz

Amplitude

Range: +13 dBm to −127 dBm (+1.00V to +.100 μV)

Resolution: 0.1 dB

Absolute Level Accuracy: ≤±1.5 dB

Level Flatness: ≤±1.0 dB (100 kHz to 990 MHz with output level setting of 0.0 dBm)

Modulation

AM
Depth: 0% to 99% to +7 dBm
0% to 30% to +10 dBm

Resolution: 1%

FM
Peak Deviation:

Carrier Frequency (MHz)	Maximum Peak Deviation	
	Rates ≥60 Hz	Rates <60 Hz
0.1 — 123.5	99 kHz	1600 × Rate
123.5 — 247	25 kHz	400 × Rate
247 — 494	50 kHz	800 × Rate
494 — 990	99 kHz	1600 × Rate

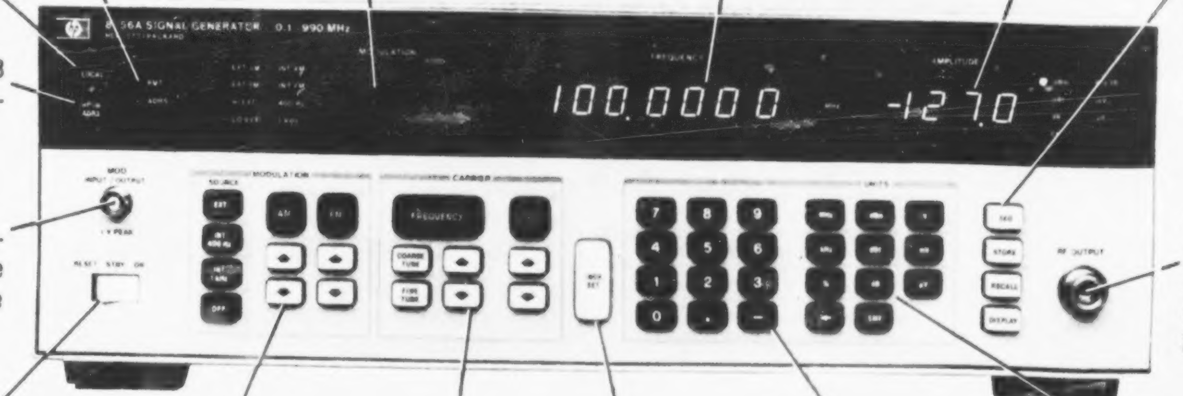
Resolution: 0.1 kHz (deviations <10 kHz)
1 kHz (deviations ≥10 kHz)

Rates: 400 Hz or 1 kHz ±3%, internal
25 Hz to 25 kHz, external (ac coupled, 1 dB bandwidth)

External Modulation Source: 600 ohms nominal, ac coupled

Mixed Modulation: Any combination of internal AM, internal FM, external AM, or external FM is possible.

SIMPLIFIED FRONT PANEL FEATURES AND OPERATION



Remote Annunciators

2 LED annunciators used to indicate remote operation status (see Figure 3-2).

MODULATION Display

2 digit display of AM depth, FM peak deviation frequency, or modulation increment. 10 LED annunciators display internal and external modulation source information. Also used to display the internally-set, decimal HP-IB address (see Figure 3-2).

AMPLITUDE Display

3-1/2 digit display of RF output level or amplitude increment. 7 LED annunciators display unit information. Also used to display the current contents of the internal sequence counter and to indicate that a reverse power condition has been detected (see Figure 3-2).

LOCAL Key

Returns the Signal Generator to local operation, provided that it is not in local lockout (see Figure 3-2).

FREQUENCY Display

8 digit display of frequency or frequency increment in megahertz (see Figure 3-2).

STORE-RECALL-DISPLAY-SEQUENCE Keys

Stores up to ten complete front panel settings for selectable recall or display at a later time. The SEQ key permits a sequential recall of stored front panel settings or a display of the internal sequence counter contents when it is used in conjunction with the DISPLAY key (see Figure 3-6).

HP-IB ADRS Key

Causes the internally-set, decimal HP-IB address to be displayed in the MODULATION Display (see Figure 3-2).

MOD INPUT/OUTPUT Connector

AC-coupled input for an external modulation source or DC-coupled output for the internal modulation source (see Figure 3-4).

RF OUTPUT Connector

Provides an AC-coupled, reverse-power protected RF output signal with a frequency range of 100 kHz to 990 MHz and a leveled output of +13 dBm to −127 dBm (see Figure 3-3).

RESET/STBY/ON Switch

Controls the operating state of the internal microprocessor. The internal power supply (and optional reference oscillator) remain energized as long as the power cable is connected to Mains power (see Figure 3-6).

Data Entry Keys

Ten numeric entry keys, a decimal point key, and a minus sign key used for frequency, amplitude, AM, FM, or increment value data entry. Numeric entry keys are also used in conjunction with the STORE, RECALL, or DISPLAY keys to select one of the ten internal storage registers (see Figure 3-5).

UNITS Entry Keys

Terminates a data entry for any one of the four main functions. The backspace key (←) clears the last digit or decimal point visible in a display to permit the entry to be corrected (see Figure 3-5).

CARRIER Keys

Selects and permits tuning of the basic carrier functions (see Figure 3-3).

MODULATION Keys

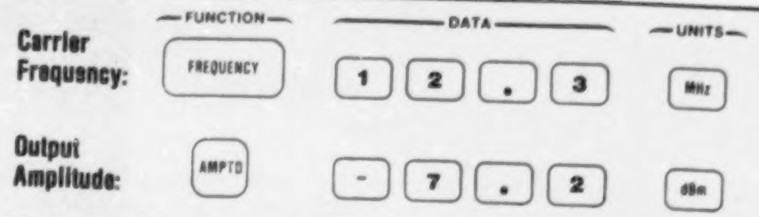
Selects either internal, external, or mixed AM or FM functions (see Figure 3-4).

INCR SET Key

Selects the value of the frequency, amplitude, AM, or FM increment. Also used to display the stored increment value for each of the four main functions (see Figure 3-6).

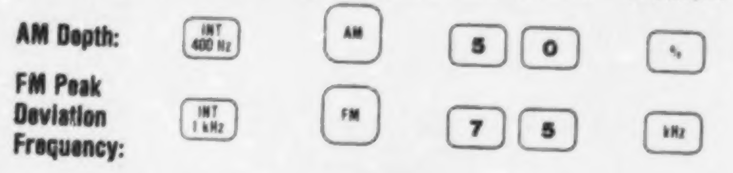
Figure 3-1. Simplified Front Panel Features

SETTING CARRIER FUNCTIONS



Both of the Signal Generator's carrier functions have value-selectable parameters. These parameters are selected in the Function-Data-Units format as shown in the examples above.

SETTING MODULATION FUNCTIONS



Internal, external, or mixed AM or FM functions can be selected. Modulation parameters are selected in the Source-Function-Data-Units format as shown in the examples above. One of the two internal modulation sources (400 Hz or 1 kHz) and/or a signal from an external modulation source (ac coupled through the front panel connector) may be used to modulate the carrier.

CHANGING PARAMETERS VALUES

Value-selectable parameters can be changed by making new Function-Data-Units entries, or by using the step up or down keys associated with each of the four main functions. These keys are used in conjunction with the INCR SET key.

Step Up and Down Keys

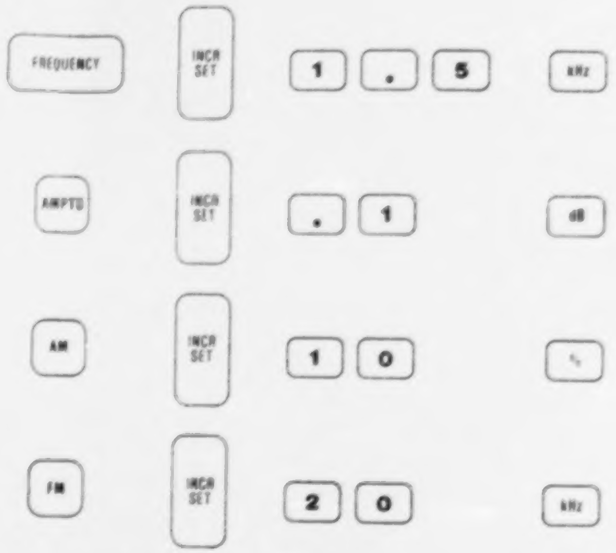
The step up and down keys are always enabled to change the value of the associated main function. The initialized value of each increment is listed as follows:

Carrier Frequency	10 MHz
Output Amplitude	10 dB
AM Depth	1%
FM Peak Deviation Frequency	1 kHz

The value of each increment can be displayed or modified by using the INCR SET key. The stored increment value will be displayed as long as the INCR SET key remains pressed.

CHANGING PARAMETERS VALUES (Cont'd)

The increment value for the four main functions can be modified as follows:



The maximum allowable increment value for each of the four main functions is as follows:

Carrier Frequency	≤989.99 MHz
Output Amplitude	≤144 dB
AM Depth	≤99%
FM Peak Deviation Frequency	≤99 kHz

NOTE

The carrier frequency increment is rejected if it is not a multiple of 100 Hz or 250 Hz.

In addition, value-selectable carrier frequency parameters can be changed using the COARSE TUNE or FINE TUNE keys in conjunction with the step up or step down keys associated with the carrier frequency function. The COARSE TUNE key causes the carrier frequency tuning value to be increased by a factor of 10 each time it is pressed, while the FINE TUNE key causes the carrier frequency tuning value to be decreased by a factor of 10. Pressing the INCR SET key disables the affect of these keys and enables the original carrier frequency increment value.

STORE-RECALL-DISPLAY-SEQUENCE

Up to ten complete front panel settings (exclusive of increment values) can be stored for either selectable or sequential recall at a later time. The output of the Signal Generator will be changed so that it agrees with the recalled parameter values. Stored front panel settings can also be displayed without actually changing the output signal.

Table 3-3. Index of Detailed Operating Instructions

Instruction	Page
Frequency	3-39
Frequency, Coarse and Fine Tune	3-41
Frequency, Up/Down	3-43
Amplitude	3-32
Amplitude Conversion	3-34
Amplitude, Up/Down	3-36
Modulation, AM	3-49
Modulation, AM Up/Down	3-50
Modulation, External Source	3-51
Modulation, FM	3-52
Modulation, FM Up/Down	3-54
Modulation, Mixed	3-55
Modulation, Off	3-59
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Increment Value Display	3-48
Display	3-37
Display Sequence	3-38
Recall	3-61
Sequence	3-62
Store	3-63
HP-IB Address Display	3-44

The actual detailed operating instructions are arranged in alphabetical order at the end of this section.

Modulation Keystroke Sequence. Internal, external, or mixed AM or FM functions can be selected. Modulation parameters are selected in a Source-Function-Data-Units format. The modulation source, either one of the two internal modulation signals (400 Hz or 1 kHz) and/or a signal from an external modulation source (ac coupled through the front panel connector), may be selected before or after the AM depth or FM peak deviation frequency parameters are selected. The internal 400 Hz or 1 kHz modulation source will be common to both AM and FM functions whenever they are simultaneously selected.

Store-Recall-Display Keystroke Sequence. Up to ten complete front panel settings (exclusive of increment values) can be stored for either selectable or sequential recall at a later time. Stored front panel settings can also be displayed without actually changing the output signal. A two keystroke sequence is necessary to store, recall, or display front panel settings. First, the desired function is entered followed by a numeric entry (0—9). This numeric entry represents the location of the internal storage register.

3-11. Time Base Selection

The Signal Generator is shipped from the factory with an inductive-jumper hard-wired to provide a 10 MHz time base output signal at the rear panel TIME BASE OUTPUT connector. If either a 1 or 5 MHz output signal is desired, this internal inductive-jumper will have to be repositioned. Also, if an external 1 or 5 MHz reference input is to be applied at the rear panel TIME BASE INPUT connector, this internal inductive-jumper will have to be repositioned. In either case, this internal inductive-jumper has to be installed in the position that corresponds to the frequency of the time base input or output signal being used. Refer to paragraph 2-7 for the time base selection procedure.

3-12. OPERATOR'S MAINTENANCE

WARNING

For continued protection against fire hazard, replace the line fuse with only a 250V slo-blo fuse of the same rating. Do not use repaired fuses or short circuited fuseholders.

The only maintenance that the operator should normally perform is the replacement of the primary power fuse located within the Line Power Module — A15. For instructions on how to change the fuse, see Figure 2-1, steps 1 and 3.

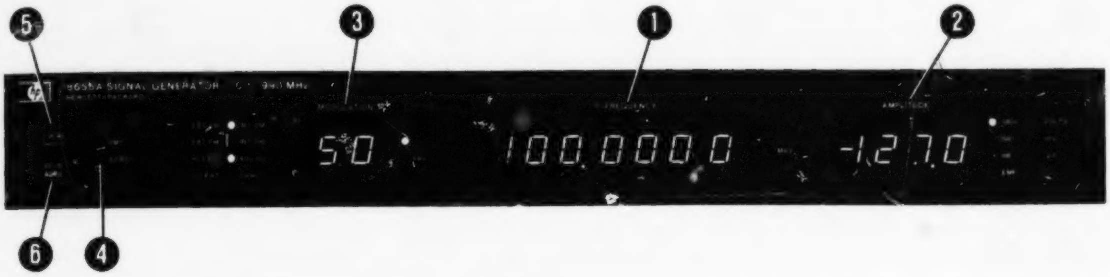
Fuses may be ordered under HP Part Numbers 2110-0305 (1.25A, 250V, slo-blo) for 100/120 Vac operation and 2110-0016 (0.6A, 250V, slo-blo) for 220/240 Vac operation.

3-13. DETAILED PANEL FEATURES

The Signal Generator is designed to be simple and easy to operate through the front panel. The front panel primarily consists of 48 pushbutton keys, three digital displays, and 19 LED annunciators. Each key has a single purpose and only one key should ever be pressed at any given time. In most cases, keys are pressed, then released, with the action occurring as the key is pressed. In some cases, a key must be pressed and held for the action to occur. The four main functions of the Signal Generator are selected by the four dark gray colored keys labeled FREQUENCY, AMPTD, AM, and FM. The 27 medium gray colored keys are used to control the modulation source, enter numeric data, and select the unit(s) which terminates the data entry. The 15 light gray colored keys are used to set an increment value for each of the four main functions, change main function parameters by the set increment values, and store up to ten complete front panel settings (exclusive of increment values) for either selectable or sequential recall or display at a later time. The two remaining dark gray colored keys (located in the upper left-hand corner of the front panel) select local operation and display the internally-set, decimal HP-IB address.

The three digital displays show the frequency of the carrier in megahertz (the least significant or eighth digit will either be blanked or a numeral 5 depending on the frequency selected), the output amplitude of the carrier in one of fourteen possible units, and the percentage of AM depth or frequency of FM peak deviation used to modulate the carrier. In addition, the FREQUENCY Display can show the value of the carrier frequency increment; the AMPLITUDE Display can show the value of the output amplitude increment or current contents of the internal sequence counter; and the MODULATION Display can show the value of the modulation increment or internally-set, decimal HP-IB address.

The 19 LED annunciators are used to indicate remote operation status, internal or external modulation source and unit information, and amplitude unit information. All of the front and rear panel features are described in detail in Figures 3-2 through 3-7.



① FREQUENCY Display

The FREQUENCY Display provides an 8 digit display of carrier frequency from 10 kHz to 990 MHz with a resolution of 100 Hz or 250 Hz. Carrier frequencies are always displayed in megahertz. Any selected frequency between 10 kHz and 100 kHz will result in an uncalibrated output amplitude. When the selected carrier frequency is a multiple of 100 Hz, the resolution will be 100 Hz and the least significant (eighth) digit will be blanked. In cases where the selected carrier frequency is a multiple of 250 Hz, the resolution will be 250 Hz and the least significant digit will be a 5. Digits selected beyond the specified resolution will be truncated and leading zeros will be blanked.

The FREQUENCY Display is also used to display the value stored in the internal carrier frequency increment register. This stored value is used in conjunction with the step up and step down keys associated with the frequency function to change the carrier frequency.

② AMPLITUDE Display

The AMPLITUDE Display provides a 3-1/2 digit display of output amplitude from +17 to -127 dBm with a resolution of 0.1 dB. Amplitude levels are displayed in dBm, dBf, V, mV, and μV, while relative levels are displayed in dB and EMF. Calibrated levels from +13 to -127 dBm are possible with overrange to the maximum available power (amplitude set to +17 dBm). Digits selected beyond the specified resolution will be truncated and leading zeros will be blanked.

The AMPLITUDE Display is also used to display the value stored in the internal output amplitude increment register. This stored value is used in conjunction with the step up and step down keys associated with the amplitude function to change the output amplitude.

Further, the least significant digit of the AMPLITUDE Display is used to display the stored contents of the internal sequence counter.

Also, whenever a reverse power condition is detected, all segments and all seven LED annunciators associated with the AMPLITUDE Display will flash until the source of reverse power is removed and the AMPTD key is pressed.

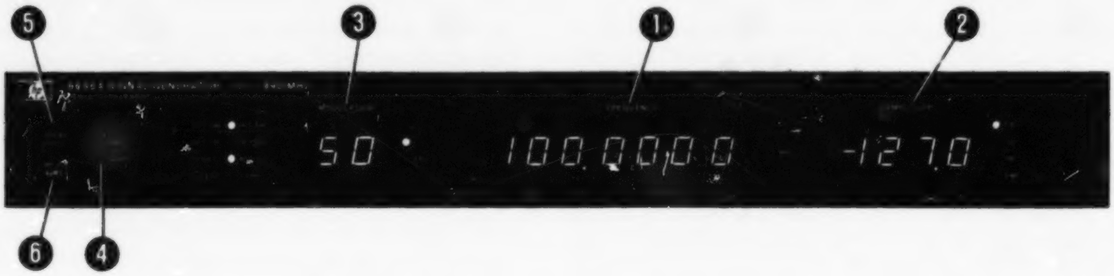
Seven LED annunciators are used to display output amplitude unit information. Fourteen unit combinations are possible which will cause one or more LED's to light. The valid output amplitude units are listed as follows:

dBm
dBf
dB V
dB mV
dB μV
dB EMF V
dB EMF mV
dB EMF μV
V
mV
μV
EMF V
EMF mV
EMF μV

③ MODULATION Display

The MODULATION Display provides a 2 digit display of AM depth from 0 to 99% with a resolution of 1% or FM peak deviation frequency from 0 to 99 kHz with a resolution of 0.1 kHz (for deviations <10 kHz) or 1 kHz (for deviations ≥10 kHz). AM depth is always displayed in percent,

Figure 3-2. Display and Remote Features (1 of 2)



③ MODULATION Display (Cont'd)

and FM peak deviation frequency is always displayed in kHz. Digits selected beyond the specified resolution will be truncated and leading zeros will be blanked.

If one modulation parameter is being displayed when the other modulation function is selected, the MODULATION Display will be updated to display the newly selected parameter. Selecting the other function will restore the original display.

If a change in carrier frequency causes the FM peak deviation frequency allowed for that frequency band to be exceeded, the MODULATION Display will flash until a carrier frequency within the correct band is selected or the FM, FM step up, or FM step down key is pressed. In this later case, the maximum FM peak deviation frequency permitted for the currently selected carrier frequency will automatically be selected.

The MODULATION Display is also used to display the values stored in the internal AM depth and FM peak deviation frequency increment registers. These stored values are used in conjunction with the step up and step down keys associated with the modulation functions to change the percentage of AM depth or FM peak deviation frequency.

Further, the MODULATION Display is used to display the internally-set, decimal HP-IB address. HP-IB addresses from 0 to 30 (decimal) are valid, all others will be interpreted as 30. (Refer to Section II, Installation when changing the HP-IB address.)

Ten LED annunciators are used to display internal and external modulation source information. The HI EXT and LO EXT annunciators serve as an aid in adjusting the level of the external modulation source. They indicate that the input level is too high or too low for a calibrated display of AM depth or FM peak deviation frequency. The HI EXT annunciator will light if the external modulation signal is greater than 1.02 Vpk (0.721 Vrms), and the LO EXT annunciator light if the signal is less than 0.98 Vpk (0.693 Vrms). Both annunciators will be off when the input level is 1.00 ±0.02 Vpk (0.707 ±0.014 Vrms).

④ Remote Annunciators

Two LED annunciators are used to display remote operation status. The RMT annunciator lights when the instrument is in remote operation. The ADRS annunciator lights when the instrument has been addressed to listen via the bus (regardless of whether or not the instrument is in remote operation).

⑤ LOCAL Key

The LOCAL key returns the instrument to local operation (full front panel control) from remote operation provided that it is not in Local Lockout.

⑥ HP-IB ADRS Key

The HP-IB ADRS key is used to display the internally-set, decimal HP-IB address in the MODULATION Display.

Figure 3-2. Display and Remote Features (2 of 2)

CARRIER Keys

FREQUENCY
COARSE TUNE
FINE TUNE

The FREQUENCY key is one of the four main function keys. It is used in conjunction with the numeric entry keys, decimal point key, and UNITS entry keys to enter carrier frequency parameters. In addition, it is used in conjunction with the INCR SET key to enter carrier frequency increment values.

The step up and step down keys associated with the frequency function permit the carrier frequency to be changed by the value stored in the internal carrier frequency increment register. The value of the carrier frequency increment initially stored is 10.0000 MHz. Its minimum value is 100 Hz, and its maximum value is ≤989.99 MHz. The carrier frequency will be changed once for each keystroke or repeatedly if either key remains pressed.

The COARSE TUNE and FINE TUNE keys are used in conjunction with the frequency step up and step down keys to tune the carrier frequency. They are used to increase (COARSE TUNE) or decrease (FINE TUNE) the carrier frequency tuning value by a factor of 10. The affect of these keys is disabled and the original carrier frequency increment value is enabled when the INCR SET key is pressed.

If a change in carrier frequency causes the FM peak deviation frequency allowed for that frequency band to be exceeded, the MODULATION Display will flash until a carrier frequency within the correct band is selected or the FM, FM step up, or FM step down key is pressed. In this later case, the maximum FM peak deviation frequency permitted for the currently selected carrier frequency will automatically be selected.

The AMPTD key is one of the four main function keys. It is used in conjunction with all of the Data and UNITS entry keys to enter output amplitude parameters. In addition, it is used in conjunction with the INCR SET key to enter output amplitude increment values. Further, it is used to reset the internal reverse power protection feature once the source of reverse power has been removed.

The step up and step down keys associated with the amplitude function permit the output amplitude to be changed by the value stored in the internal output amplitude increment register. The value of the output amplitude increment initially stored is 10.0 dB. Its minimum value is 0.1 dB (0.001 μV or 0.001 EMF V), and its maximum value is ≤144.0 dB (≤1.57V or ≤ 3.15 EMF V). The output amplitude will be changed once for each keystroke or repeatedly if either key remains pressed.

RF OUTPUT Connector

Female type-N connector (J2) provides access to the RF output signal. Specified output levels are +13 to −127 dBm (+1.00V to +.100 μV) with a minimum resolution of 0.1 dBm. Nominal impedance is 50 ohms. Reverse power protection is provided up to 50W and 25 Vdc. Pressing the AMPTD key restores RF output signal once the source of reverse power has been removed.

Figure 3-3. Carrier Features

MODULATION Keys

The AM key is one of the four main function keys. It is used in conjunction with the SOURCE keys, numeric entry keys, and UNITS entry keys to enter amplitude modulation parameters. In addition, it is used in conjunction with the INCR SET key to enter AM depth increment values. If the FM peak deviation frequency is being displayed when the AM key is pressed, the MODULATION Display will be updated to show the percentage of AM depth. The default modulation source (internal 1 kHz) will automatically be selected when the AM key is pressed, if no other source has been selected.

The step up and step down keys associated with the AM function permit the percentage of AM depth to be changed by the value stored in the internal AM depth increment register. The value of the AM depth increment initially stored is 1%. This is its minimum value. Its maximum value is ≤99%. The percentage of AM depth will be changed once for each keystroke or repeatedly if either key remains pressed.

The FM key is one of the four main function keys. It is used in conjunction with the SOURCE keys numeric entry keys, and UNITS entry keys to enter frequency modulation parameters. In addition, it is used in conjunction with the INCR SET key to enter FM peak deviation frequency increment values. If the percentage of AM depth is being displayed when the FM key is pressed, the MODULATION Display will be updated to show the FM peak deviation frequency. The default modulation source (internal 1 kHz) will automatically be selected when the FM key is pressed, if no other source has been selected.

The step up and step down keys associated with the FM function permit the FM peak deviation frequency to be changed by the value stored in the internal FM peak deviation frequency increment register. The value of the FM peak deviation frequency increment initially stored is 1.0 kHz. Its minimum value is 0.1 kHz, and its maximum value is ≤99 kHz. The FM peak deviation frequency will be changed once for each keystroke or repeatedly if either key remains pressed.

If an out of range condition exists (MODULATION Display flashing), pressing either the step up, step down, or FM key will automatically select the maximum FM peak deviation frequency permitted for the currently selected carrier frequency.

SOURCE Keys

SOURCE
EXT
INT 400 Hz
INT 1 kHz
OFF

The INT 400 Hz, INT 1 kHz, EXT, and OFF keys are used to select the internal 400 Hz or 1 kHz modulation source, enable an external source to be applied through the front panel MOD INPUT/OUTPUT connector, or disable one or all selected modulation sources.

The internal modulation signal is available at the MOD INPUT/OUTPUT connector when either the 400 Hz or 1 kHz modulation source is selected and the external source is not selected.

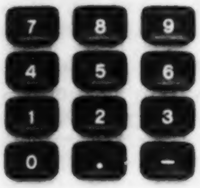
MOD INPUT/OUTPUT Connector

MOD
INPUT/OUTPUT
1 V PEAK

Female BNC connector (J1) accepts either an external modulation signal or a digital unsquelching signal. In addition, it provides access to the 400 Hz or 1 kHz modulation signal from the internal audio oscillator. Source selection is provided by the four MODULATION SOURCE keys. Nominal input impedance is 600 ohms. External input rates are ac coupled with 1 dB of bandwidth. The input signal should be 25 Hz to 25 kHz at 1 Vpk (0.707 Vrms) ±5% minimum into a 600 ohm resistive load to produce calibrated AM depths or FM peak deviations. The HI EXT and LO EXT annunciators provide an indication of the input level available for calibrated modulation. If greater accuracy is required, the signal level should be measured externally.

Figure 3-4. Modulation Features

Data Entry Keys



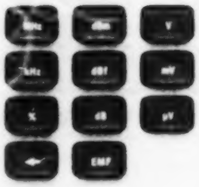
The Data entry keys consist of ten numeric entry keys (0-9), a decimal point key, and a minus sign key.

The ten numeric entry keys are used in conjunction with the four main function keys to enter value-selectable parameters, with the INCR SET key to enter increment values, and with the STORE-RECALL-DISPLAY keys to select one of the ten internal storage registers.

The decimal point key is used to add a decimal point to the numeric entry. A leading zero will be displayed, if the decimal point is added before the numeric entry for carrier frequencies less than 1 MHz and output amplitudes less than ±1 dBm.

The minus sign key is only used when making amplitude Data entries and it can be used at any time before the final UNITS terminator entry is made.

UNITS Entry Keys



The UNITS entry keys consist of ten terminator keys and a backspace (←) key.

The ten terminator keys are used in conjunction with the four main function keys to terminate Data entries. They are also used in conjunction with the INCR SET key to terminate increment value entries.

Frequency entries are always adjusted so that they are displayed in megahertz, even though kHz is a valid terminator.

Fourteen amplitude terminator combinations are possible. They are listed as follows:

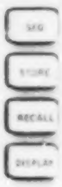
- dBm
- dBf
- dB V
- dB mV
- dB μV
- dB EMF V
- dB EMF mV
- dB EMF μV
- V
- mV
- μV
- EMF V
- EMF mV
- EMF μV

AM entries are always terminated in %, and FM entries are always terminated in kHz.

The backspace key is used to clear the last digit or decimal point visible in a display to permit the entry to be corrected.

Figure 3-5. Data and Units Entry Features

STORE-RECALL-DISPLAY-SEQUENCE Keys



Four keys used to store up to ten complete front panel setups (exclusive of increment values) for either selectable or sequential recall or display at a later time. When the Signal Generator is powered up or reset, the initialized conditions of the instrument are stored in each of the ten internal storage registers. That is, the parameter values for a carrier frequency of 100 MHz with an output amplitude of -127 dBm and no modulation will be stored in each location.

When the STORE key is used in conjunction with a numeric entry key (a single digit register number 0—9), the current front panel settings (exclusive of increment values) will be stored in an internal storage register.

When the RECALL key is used in conjunction with a numeric entry key (a single digit register number 0—9), the stored contents will be recalled and the output of the Signal Generator will be changed so that it agrees with the recalled parameter values.

When the DISPLAY key is used in conjunction with a numeric entry key (a single digit register number 0—9), the stored contents will be displayed, but the actual output of the Signal Generator will not be affected.

The SEQ key is used to sequence the Signal Generator through each of its ten internal storage registers. As the stored contents are sequentially recalled, the output will be changed so that it agrees with the recalled parameter values.

When the DISPLAY key is used in conjunction with the SEQ key, the stored contents of the internal sequence counter will be displayed in the least significant digit of the AMPLITUDE Display.

INCR SET Key

A single key used in conjunction with any one of the four main function keys to store an increment value for that function. The initialized value of each stored increment is listed as follows:

Carrier Frequency	10.0000 MHz
Output Amplitude	10.0 dB
AM Depth	1%
FM Peak Deviation Frequency	1.0 kHz

The minimum allowable increment value for each of the four main functions is listed as follows:

Carrier Frequency	0.1 kHz
Output Amplitude	0.1 dB
AM Depth	1%
FM Peak Deviation Frequency	0.1 kHz

Figure 3-6. Miscellaneous Features (1 of 2)

INCR SET Key (Cont'd)

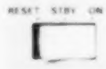
The maximum allowable increment value for each of the four main functions is listed as follows:

Carrier Frequency	≤ 989.99 MHz
Output Amplitude	≤ 144.0 dB
AM Depth	≤ 99%
FM Peak Deviation Frequency	≤ 99 kHz

The stored value of the increment will be displayed in the display associated with the selected function as long as the INCR SET key remains pressed.

The frequency coarse tune and fine tune feature will be disabled and the original carrier frequency increment value will be restored when the INCR SET key is pressed.

RESET/STBY/ON Switch



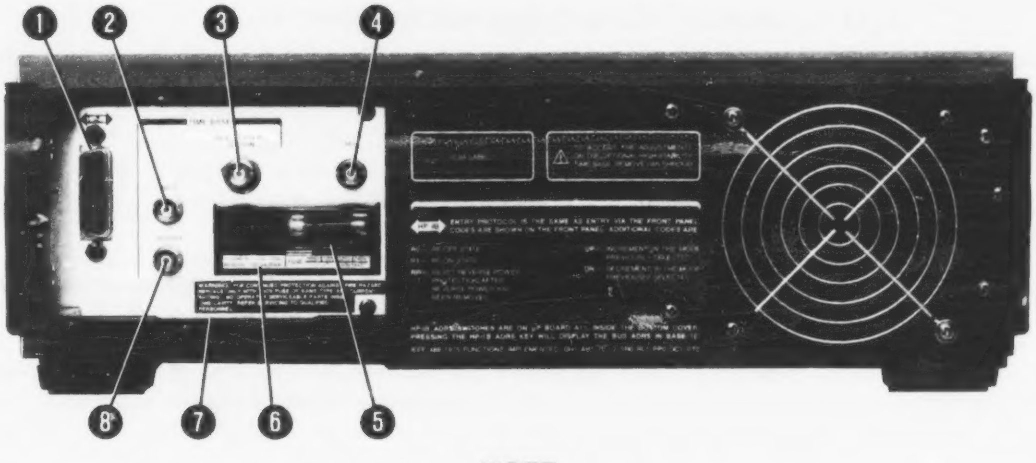
Three position rocker switch used to control the operating state of the internal microprocessor. The Signal Generator (and its optional reference oscillator) will remain energized and the fan will continue to operate as long as the power cord is connected to Mains power.

When momentarily set to RESET, the microprocessor will be halted. Upon release, the microprocessor will initiate its restart operation.

When set to STBY, the microprocessor will initiate an RF quieting operation in which all displays are blanked, the high frequency section is turned off, all attenuator sections (120 dB) are switched in, the internal audio oscillator is turned off, and the instrument will not respond to any HP-IB commands.

When set to ON (return from STBY), the operating state of the instrument (prior to entering the standby state) will be restored. Refer to paragraph 3-9 for information regarding the power-on sequence.

Figure 3-6. Miscellaneous Features (2 of 2)



NOTE

For Option 002 instruments, the RF OUTPUT and MOD INPUT/OUTPUT connectors are located on the rear panel. The RF OUTPUT connector is above ❷ *Time Base Input while the MOD INPUT/OUTPUT connector replaces* ❹ *SEQ. Refer to Figures 3-3 and 3-4 for detailed information concerning the signals found at these ports.*

❶ HP-IB HP-IB Connector

24-pin female connector used to connect the Signal Generator to the Hewlett-Packard Interface Bus for remote operation. Connection information is presented in Section II, Installation.

❷ TIME BASE INPUT

Female BNC connector (J3) accepts an external 1, 5, or 10 MHz (±0.005%) time base reference input at a level of 0.2 to 0.4 Vrms into 50 ohms. Internal jumper must be installed in the position that corresponds to the external time base reference input used (refer to paragraph 2-7).

❸ TIME BASE HIGH STABILITY OPTION

Female BNC connector (A16J1) provides access to the optional 10 MHz time base reference output. With Option 001 installed and its output connected to the TIME BASE INPUT connector through the supplied cable (not shown), the frequency accuracy and stability of the Signal Generator will be increased. The optional reference oscillator is kept at operating temperature in the STBY mode as long as the Signal Generator remains connected to Mains power.

❹ SEQ

Female BNC connector (J5) accepts external contact closure (from foot pedal, pushbutton switch, etc.) which causes the Signal Generator to sequentially recall the stored contents (exclusive of increment settings) from each of its ten internal storage registers.

❺ Fuse

1.25A, 250V, Slo-Blo for 100/120 Vac operation. 0.6A, 250V, Slo-Blo for 220/240 Vac operation. Ordering information is presented in Section II, Installation.

❻ Line Power Module

Permits operation from 100, 120, 220, or 240 Vac. The number visible in the window indicates nominal line voltage to which the instrument must be connected (see Figure 2-1). Center conductor is safety earth ground.

❼ Serial Number Plate

First four digits and letter constitute the prefix which defines the instrument configuration. The last five digits form a sequential suffix that is unique to each instrument. The plate also indicates any options supplied with the instrument.

❽ TIME BASE OUTPUT

Female BNC connector (J4) provides access to an internal 10 MHz time base reference output at a level greater than 0.2 Vrms into 50 ohms which is derived from the internal reference oscillator. An internal jumper may be repositioned to select either a 1 or 5 MHz reference output (refer to paragraph 2-7).

Figure 3-7. Rear Panel Features

3-14. OPERATOR'S CHECKS

Operator's checks are simple procedures designed to verify that the main functions of the Signal Generator operate properly. Two procedures are provided, one for basic (front panel) functional checks and the other for HP-IB functional checks.

3-15. Basic Functional Checks

DESCRIPTION: This procedure requires only a frequency counter, a spectrum analyzer, and the interconnecting cables and adapters. It provides assurance that most of the front panel controlled functions are being executed by the Signal Generator.

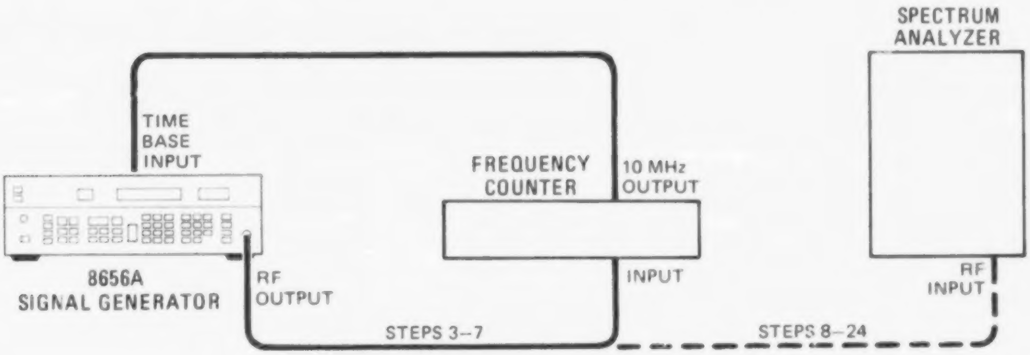


Figure 3-8. Test Setup for Basic Functional Checks

EQUIPMENT: Frequency Counter .... HP 5328A Option 031
Spectrum Analyzer .... HP 8558B/182T

PROCEDURE: **Preliminary Checks**

1. Ensure that the power cable is plugged into a suitable source of Mains power (refer to paragraph 2-4).
2. Momentarily press and release the left-hand side of the RESET/STBY/ON switch to initialize the Signal Generator, then set the switch back to ON.

   An internal memory check will be initiated to test for a failure in ROM (read-only memory) and in RAM (read-write memory). All front panel indicators will light for approximately 1.5 seconds to provide a quick visual inspection of each front panel annunciator and display segment.

   If a memory failure is detected, all front panel annunciators and display segments will remain lit until any front panel key is pressed. If the memory check was successful, the front panel indicators will display a carrier frequency of 100.0000 MHz, an output amplitude of −127.0 dBm, and no modulation. Only the dBm annunciator will be lit, all of the others be off.
3. Connect the RF OUTPUT of the Signal Generator to the input of the frequency counter and the 10 MHz reference output from the frequency counter to the TIME BASE INPUT located at the rear of the Signal Generator as shown in Figure 3-8.

3-15. Basic Functional Checks (Cont'd)

Connecting the 10 MHz reference output of the frequency counter to the TIME BASE INPUT of the Signal Generator will phase lock the two instruments to the same time base reference.

NOTE

If the Signal Generator is equipped with the high stability time base (Option 001), disconnect its cable from the TIME BASE INPUT before performing this step.

Frequency Check

4. Set the output amplitude of the Signal Generator to −10.0 dBm and the carrier frequency to the values listed in the following table:

Carrier Frequency (MHz)
100.0000
140.0000
200.0000
300.0000
400.0000
600.0000
800.0000
990.0000

Verify that the FREQUENCY Display on the Signal Generator agrees with the frequency displayed on the frequency counter (except for the resolution of the frequency counter being used).

5. Set the carrier frequency of the Signal Generator to 111.1111 MHz and the frequency increment value to 111.1111 MHz. Leave the output amplitude set at −10.0 dBm.

   Verify that the FREQUENCY Display on the Signal Generator agrees with the frequency displayed on the frequency counter.

6. Quickly press and release the frequency step up key to increase the carrier frequency.

   Verify that the FREQUENCY Display on the Signal Generator agrees with the frequency displayed on the frequency counter.

OPERATOR'S CHECKS

3-15. Basic Functional Checks (Cont'd)

Continue to increase the carrier frequency to the maximum value listed in the following table:

Carrier Frequency (MHz)
111.1111
222.2222
333.3333
444.4444
555.5555
666.6666
777.7777
888.8888

Verify that the FREQUENCY Display on the Signal Generator agrees with the frequency displayed on the frequency counter each time the carrier frequency is increased.

7. Quickly press and release the frequency step down key to decrease the carrier frequency.

   Verify that the FREQUENCY Display on the Signal Generator agrees with the frequency displayed on the frequency counter.

   Continue to decrease the carrier frequency to the minimum value listed in the previous table.

   Verify that the FREQUENCY Display on the Signal Generator agrees with the frequency displayed on the frequency counter each time the carrier frequency is decreased.

Output Level Checks

8. Connect the RF OUTPUT of the Signal Generator to the input of the spectrum analyzer as shown in Figure 3-8.
9. Set the output amplitude of the Signal Generator to 0.0 dBm, carrier frequency to 0.1 MHz, and frequency increment value to 10 MHz.
10. Set the amplitude scale of the spectrum analyzer to display 1 dB/division and make the necessary adjustments to properly display the output signal from the Signal Generator.

NOTE

This check only verifies level flatness, it does not verify absolute level accuracy.

11. Slowly increase the carrier frequency through its entire frequency range (0.1 to 990.0000 MHz) and observe the level displayed on the spectrum analyzer. The level should not vary more than a total of 3 dB (±1.5 dB from 0.0 dBm).

OPERATOR'S CHECKS

3-15. Basic Functional Checks (Cont'd)

12. Set the carrier frequency of the Signal Generator to 600 MHz, output amplitude to +13 dBm, and output amplitude increment value to 1.0 dB.
13. Adjust the spectrum analyzer as necessary to display the output signal from the Signal Generator. The displayed carrier should be positioned in the center of the graticule with its maximum level positioned near the top of the graticule.
14. Slowly decrease the output amplitude down to -4.0 dBm and observe the level displayed on the spectrum analyzer. The level should decrease in relatively uniform 1 dB steps.
15. Set the output amplitude of the Signal Generator to -10.0 dBm and the output amplitude increment value to 5 dB. Leave the carrier freqeuency set to 600 MHz.
16. Set the amplitude scale of the spectrum analyzer to display 10 dB/division and make the necessary adjustments to properly display the output signal from the Signal Generator. The displayed carrier should be positioned in the center of the graticule with its maximum level positioned near the top of the graticule.
17. Slowly decrease the output amplitude down to -80 dBm and observe the level displayed on the spectrum analyzer. The level should decrease in relatively uniform 5 dB steps.

FM Check

18. Set the output amplitude of the Signal Generator to 0.0 dBm. Leave the carrier frequency set to 600 MHz. Select FM with a peak deviation frequency of 99 kHz using the internal 1 kHz source. Set the FM peak deviation frequency increment value to 1 kHz.
19. Set the spectrum analyzer for a 50 kHz frequency span/division, a resolution bandwidth of 3 kHz, and a reference level of 0 dBm. The waveform displayed should be similar to that shown in Figure 3-9.
20. Slowly decrease the FM peak deviation frequency to zero. The deviation displayed on the spectrum analyzer should decrease in relatively uniform steps.
21. Press FM, then OFF to turn off the FM function.

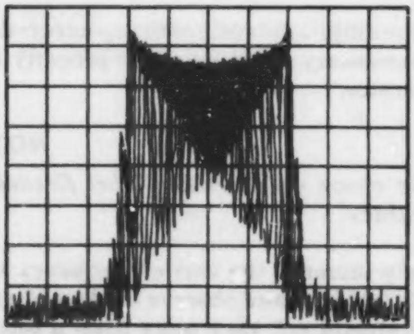


Figure 3-9. FM Functional Check Waveform

3-15. Basic Functional Checks (Cont'd)

AM Check

22. Leave the carrier frequency set to 600 MHz and the output amplitude set to 0.0 dBm. Select AM with a depth of 50% using the internal 400 Hz source.

23. Set the spectrum analyzer to the linear amplitude mode. Set a frequency span/division of zero. Increase the resolution bandwidth, then fine tune for the maximum level of the demodulated signal. The displayed demodulated signal should be a sine wave with a period of 2.5 ms (400 Hz).

24. Press the INT 1 kHz key to change the frequency of the internal modulation source from 400 Hz to 1 kHz. The displayed demodulated signal should be a sine wave with a period of 1 ms (1 kHz).

3-16. HP-IB Functional Checks HP-IB

DESCRIPTION: The following procedures check the Signal Generator's ability to recognize its own HP-IB (listen) address, properly make remote/local transitions, and process all of the applicable HP-IB messages described in Table 3-4. During the process, all of the Signal Generator's HP-IB data input/output bus, control, and handshake lines are checked, except for DIO8 (the most significant data input/output bus line which is not used by the Signal Generator). Only the Signal Generator, a bus controller, and an HP-IB interface with appropriate cabling are required to perform these procedures. These checks are intended to be as independent of one another as possible, since each begins with the instrument being reset to its initialized condition. Nevertheless, it is suggested that the first four checks be performed in order before any other check. Any special initialization steps or requirements for a given check are provided the beginning of the check.

The validity of these checks is based on the following assumptions:

- The Signal Generator performs properly when operated via the front panel keys (that is, in local operation). This can be verified by performing the basic functional checks as outlined in paragraph 3-15.
- The bus controller properly executes HP-IB operations.
- The bus controller's HP-IB interface properly transfers the controller's instructions.
- The select code of the bus controller's interface is set to 7.
- The HP-IB address of the Signal Generator is set to 07 (the factory-set address).
- The select code address combination (that is, 707) is not necessary for these checks to be valid; however, the program lines presented in the following procedures would have to be modified for any other combination.

If the Signal Generator appears to fail any of the remote functional checks, the validity of the preceding assumptions should be confirmed before attempting to service the instrument.

3-16. HP-IB Functional Checks (Cont'd)

If all of these checks are performed successfully, the Signal Generator's HP-IB capability can be considered to be operating properly. These procedures do not check whether or not all of the Signal Generator's program codes are being properly interpreted and executed by the instrument, however, if the front panel operation is confirmed to be working properly and its HP-IB capability operates correctly, then there is a high probability that the Signal Generator will respond properly to all of its program codes.

INITIAL SETUP: The test setup is the same for all of the checks. That is, the Signal Generator is connected to the bus controller through the bus controller's HP-IB interface via the appropriate cable.

EQUIPMENT:

HP-IB Controller	HP 9825A/98213A (General and Extended I/O ROM's) —or— HP 9835A/98332A (I/O ROM) —or— HP 9845A (I/O ROM)
HP-IB Interface	HP 98034A (use "revised" version with HP 9835A and HP 9845A)

Address Recognition

NOTE This check determines whether or not the Signal Generator recognizes when it is being addressed and when it is not. It is assumed that the Signal Generator is in local operation and that it can properly handshake on the bus. Before beginning this check, set the RESET/STBY/ON switch to RESET, then back to ON to initialize the instrument.

Description	HP 9825A (HPL)	HP 9835A and HP 9845A (BASIC)
Set the Remote Enable (REN) bus control line false.	lcl 7	LOCAL 7
Send the listen address to the Signal Generator.	wrt 707	OUTPUT 707

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT annunciator remains off and that its ADRS annunciator lights.

Unaddress the Signal Generator by sending a different address.	wrt 715	OUTPUT 715

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT and ADRS annunciators are both off.

3-16. HP-IB Functional Checks (Cont'd)

Remote and Local Messages and the LOCAL Key

NOTE This check determines whether the Signal Generator properly switches from local to remote operation, switches from remote to local operation, and whether the LOCAL key can return the instrument to local operation. It is assumed that the Signal Generator is able to both handshake and recognize its own address. Before beginning this check, set the RESET/STBY/ON switch to RESET, then back to ON to initialize the instrument.

Description	HP 9825A (HPL)	HP 9835A and HP 9845A (BASIC)
Send the Remote message which sets the Remote Enable (REN) bus control line true and addresses the Signal Generator to listen.	rem 707	REMOTE 707

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT and ADRS annunciators both light.

Send the Local message to the Signal Generator.	lcl 707	LOCAL 707

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT annunciator turns off and that its ADRS annunciator remains on.

Send the Remote message to the Signal Generator.	rem 707	REMOTE 707

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT and ADRS annunciators are both on. Press the LOCAL key on the front panel of the Signal Generator and verify that the RMT annunciator turns off and that the ADRS annunciator remains on.

Data Message

NOTE This check determines whether or not the Signal Generator properly receives Data messages. Because the Signal Generator is only a listener, it can only receive Data messages, but never send them. It is assumed that the Signal Generator is able to handshake, recognize its own address, and properly make remote/local transitions. The Data message that is sent will cause the 7 least significant HP-IB data lines to be placed in both their true and false states. Before beginning this check, set the RESET/STBY/ON switch to RESET, then back to ON to initialize the instrument.

3-18. HP-IB Functional Checks (Cont'd)

Description	HP 9825A (HPL)	HP 9835A and HP 9845A (BASIC)
Send the first part of the Remote message (which enables the Signal Generator to remote).	rem 707	REMOTE 707
Address the Signal Generator to listen (which completes the Remote message) and send the Data message (which tunes the Signal Generator to 990 MHz).	wrt 707, "fr990mz"	OUTPUT 707; "FR990MZ"

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT and ADRS annunciators both light and that the FREQUENCY Display shows a carrier frequency of 990.0000 MHz.

Local Lockout and Clear Lockout/Set Local Messages

NOTE This check determines whether or not the Signal Generator properly receives the Local Lockout message which disables all of the front panel keys. In addition, this check determines whether or not the Clear Lockout/Set Local message is properly received and executed by the Signal Generator. It is assumed that the Signal Generator is able to handshake, recognize its own address, and properly make remote/local transitions. Before beginning this check, set the RESET/STBY/ON switch to RESET, then back to ON to initialize the instrument.

Description	HP 9825A (HPL)	HP 9835A and HP 9845A (BASIC)
Send the first part of the Remote message (which enables the Signal Generator to remote).	rem 707	REMOTE 707
Send the Local Lockout message.	llo 7	LOCAL LOCKOUT 7
Address the Signal Generator to listen (which completes the Remote message).	wrt 707	OUTPUT 707

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT and ADRS annunciators both light. Press the LOCAL key on the front panel of the Signal Generator and verify that its RMT and ADRS annunciators both remain on.

Send the Clear Lockout/Set Local message.	lcl 7	LOCAL 7

3-16. HP-IB Functional Checks (Cont'd)

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT annunciator is turned off and that its ADRS annunciator remains on.

Clear Message

NOTE This check determines whether or not the Signal Generator properly responds to the Clear message. It is assumedthatthe Signal Generator is able to handshake, recognize its own address, properly make remote/local transitions, and receive Data messages. Before beginning this check, set the RESET/STBY/ON switch to RESET, then back to ON to initialize the instrument.

Description	HP 9825A (HPL)	HP 9835A and HP 9845A (BASIC)
Send the first part of the Remote message (which enables the Signal Generator to remote).	rem 7	REMOTE 7
Address the Signal Generator to listen (which completes the Remote message) and send the Data message (which sets the output amplitude of the Signal Generator to 3.0 dB mV).	wrt 707, "ap3dbmv"	OUTPUT 707; "AP3DBMV"

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT, ADRS, dB, and mV annunciators all light and that the AMPLITUDE Display shows an output amplitude of 3.0 dB mV.

Send the Clear message.	clr 707	RESET 707

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT and ADRS annunciators remain on and that the AMPLITUDE Display now shows the initialized output amplitude of -127.0 dBm. The dB and mV annunciators will now be off and the dBm annunciator will be on.

Abort Message

NOTE This check determines whether or not the Signal Generator becomes unaddressed when it receives the Abort message. It is assumed that the Signal Generator is able to handshake, recognize its own address, and properly make remote/local transitions. Before beginning this check, set the RESET/STBY/ON switch to RESET, then back to ON to initialize the instrument.

Description	HP 9825A (HPL)	HP 9835A and HP 9845A (BASIC)
Send the complete Remote message.	rem 707	REMOTE 707

3-16. HP-IB Functional Checks (Cont'd)

OPERATOR'S RESPONSE Verify that the Signal Generator's RMT and ADRS annunciators both light.

Send the Abort message (which unaddresses the Signal Generator to listen).	cli 7	ABORTIO 7

OPERATOR'S RESPONSE Verify that the ADRS annunciator turns off.

NOTE

The remote annunciator may also turn off when using the 9835A or 9845A.

3-17. REMOTE OPERATION, HEWLETT-PACKARD INTERFACE BUS

The Signal Generator can be operated through the Hewlett-Packard Interface Bus (HP-IB). Bus compatibility, programming, and data formats are described in the following paragraphs.

All front panel functions (except for DISPLAY, DISPLAY in conjunction with SEQ, Backspace, COARSE TUNE, FINE TUNE, and display HP-IB ADRS are programmable through HP-IB.

A quick check of the Signal Generator's HP-IB input/output capability is described in paragraph 3-16, HP-IB Functional Checks. These checks are used to verify that the Signal Generator can respond to each of the applicable HP-IB messages described in Table 3-4.

3-18. HP-IB Compatibility

The Signal Generator has an open-collector, TTL, HP-IB interface which can be used with any HP-IB computing controller or computer for automatic system applications. The Signal Generator is fully programmable via the HP Interface Bus. Its programming capability is described by the twelve HP-IB messages listed in Table 3-4. Foremost among these messages is the Data message. Data messages contain the program codes that control the Signal Generator's output signal. The Signal Generator's complete compatibility with HP-IB is further defined by the following list of interface functions: SH1, AH1, T0, L2, SR0, RL1, PP0, DC1, DT0, and C0. A more detailed explanation of these compatibility codes can be found in the IEEE Standard 488 (and the identical ANSI Standard MC1.1). For more information about HP-IB, refer to the Hewlett-Packard Electronic Instruments and Systems catalog and the booklet titled "Improving Measurements in Engineering and Manufacturing" (HP part number 5952-0058).

3-19. Remote Operation

Remote Capability. In remote operation, the front panel keys are disabled (except for the RESET/STBY/ON switch and the LOCAL key). The Signal Generator can only be addressed to listen. When addressed to listen, the Signal Generator will respond to the following messages: Data, Clear, Remote, Local, Local Lockout, Clear Lockout/Set Local, and Abort. Each is discussed in detail further on in this section.

Local-to-Remote Change. The Signal Generator switches to remote operation upon receipt of the Remote message. The Remote message is comprised of two parts. They are:

- Remote Enable bus control line (REN) set true.
- Device listen address received once (while REN is true).

The Signal Generator's RMT and ADRS annunciators will both light and its output signal and all preselected functions will remain unchanged when the local-to-remote transition occurs.

3-20. Local Operation

Local Capability. In local operation, the Signal Generator's front panel is fully operational and the instrument will respond to the Remote message. Whether addressed or not, the Signal Generator will also respond to the Clear, Local Lockout, Clear Lockout/Set Local, and Abort messages. It will not; however, respond to the Data message unless it has been previously addressed.

Remote-to-Local Change. The Signal Generator returns to local operation upon receipt of the Local message (GTL) or Clear Lockout/Set Local message. The Clear Lockout/Set Local message sets the Remote Enable bus control line (REN) false. The instrument can always be set to local operation by pressing the front panel LOCAL key provided that local lockout is not in effect. The output signal will remain unchanged and all preselected functions will remain unchanged when the remote-to-local transition occurs.

Local Lockout. When a data transmission is interrupted, which can happen by returning the Signal Generator to local operation with the LOCAL key, the data could be lost. This would leave the Signal Generator in an unknown state. To prevent this, a local lockout is recommended. Local lockout disables the LOCAL key and allows return-to-local

Table 3-4. HP-IB Message Reference Table

HP-IB Message	Applicable	Response	Related Commands Controls*	Interface Functions*
Data	Yes	All front panel functions, except for DISPLAY, DISPLAY in conjunction with SEQ, Backspace, COARSE TUNE, FINE TUNE,and display HP-IB ADRS are programmable. The front panel ADRS annunciator lights when the Signal Generator is addressed to listen.		T0, L2 AH1, SH0
Trigger	No	The Signal Generator does not have a Device Trigger (DT0) capability.	GET	DT0
Clear	Yes	Resets the Signal Generator to a carrier frequency of 100 MHz, an output amplitude of −127 dBm, and no modulation. Responds equally to Device Clear (DCL) and Selected Device Clear (SDC) bus commands.	DCL, SDC	DC1
Remote	Yes	Remote operation is entered when the Remote Enable (REN) bus control line is true and the Signal Generator is first addressed to listen. The front panel RMT and ADRS annunciators will both light when remote operation is entered, all front panel keys will be disabled (except for the LOCAL key and the RESET/STBY/ON switch), and the output signal will remain unchanged.	REN	RL1
Local	Yes	The Signal Generator will return to local operation (full front panel control) when either the Go to Local (GTL) bus command is received or the front panel LOCAL key is pressed. The output signal will remain unchanged.	GTL	RL1
Local Lockout	Yes	Disables the front panel LOCAL key so that only the controller can return the Signal Generator to local operation.	LLO	RL1
Clear Lockout/ Set Local	Yes	The Signal Generator will return to local operation and local lockout will be cleared when the REN bus control line goes false.	REN	RL1
Pass Control/ Take Control	No	The Signal Generator has no control capability.		C0
Require Service	No	The Signal Generator does not have the capability to request service.		SR0
Status Byte	No	The Signal Generator does not have the capability to respond to a serial poll.		T0
Status Bit	No	The Signal Generator does not have the capability to respond to a parallel poll.		PP0
Abort	Yes	The Signal Generator stops listening.	IFC	T0, L2

*Commands, control lines, and interface functions are defined in IEEE Standard 488 (and the identical ANSI Standard MC1.1). Knowledge of these might not be necessary if your controller's manual describes programming in terms of the twelve HP-IB Messages shown in the left-hand column above.

Complete HP-IB compatibility as defined in IEEE Standard 488 (and the identical ANSI Standard MC1.1) is: SH0, AH1, T0, L2, SR0, RL1, PP0, DC1, DT0, and C0.

Local Operation (Cont'd)
ables the LOCAL key and allows return-to-local only under program control.

NOTE

Return-to-local can also be accomplished by setting the RESET/STBY/ON switch first to RESET, then back to ON. This technique, however, has some potential disadvantages.

- *It defeats the purpose and advantage of local lockout, that is, the system controller will loose control of the Signal Generator.*
- *Some HP-IB conditions are reset to their default state during turn on.*

3-21. Addressing

The Signal Generator interprets the byte of information on its eight data input/output bus lines as either an address or a bus command whenever the bus is in the command entry mode, that is, when the Attention bus control line (ATN) is true and the Interface Clear bus control line (IFC) is false. Whenever the Signal Generator is being addressed (whether in local or remote operation), the front panel ADRS annunciator will light.

The Signal Generator's listen address is established by five miniature rocker switches located inside the instrument. The address selection procedure is described in Section II, Installation. The decimal equivalent of the listen address can be displayed in the MODULATION Display by pressing the HP-IB ADRS key. Refer to Table 3-5 for a list of the valid decimal (listen address) values and their equivalent ASCII characters.

3-22. Data Messages

The Signal Generator communicates on the interface bus with Data messages. Each Data message consists of one or more bytes of information sent over the Signal Generator's eight data input/output bus lines DIO1 through DIO8 during the data entry mode. The data entry mode is established when the Attention bus control line (ATN) is false. Data messages include the program codes listed in Tables 3-8 and 3-9. These program codes contain the necessary information to program virtually all of the instrument functions available in local operation. The only exceptions are DISPLAY, DISPLAY in conjunction with SEQ, Backspace, COARSE TUNE, FINE TUNE, and display HP-IB ADRS.

Table 3-5. Valid Decimal Values vs. Equivalent ASCII Characters

EQUIVALENT DECIMAL VALUE (LISTEN)	EQUIVALENT ASCII CHARACTER (LISTEN)
00	SP
01	!
02	"
03	#
04	$
05	%
06	&
07	'
08	(
09	)
10	*
11	+
12	,
13	-
14	.
15	/
16	0
17	1
18	2
19	3
20	4
21	5
22	6
23	7
24	8
25	9
26	:
27	;
28	<
29	=
30	>

Indicates Factory-set address.

3-23. Receiving the Data Message

The Signal Generator must be in remote operation and addressed to listen before it can respond to Data messages. The instrument will remain addressed to listen until it receives an Abort message or a universal unlisten command from the controller.

The paragraph entitled Switching Characteristics shows how the Signal Generator responds to Data Messages. Timing considerations and other characteristics pertinent to operation are included.

Data Message Input Format. Data messages contain the controller's talk address, the Signal Gen-

Receiving the Data Message (Cont'd) erator's listen address, a string of program codes, and an End of String message (EOS). The string of program codes follows the same protocol as a front panel keystroke sequence in local operation. The EOS message can be a Line Feed (LF), a bus END message (EOI and ATN bus control lines both set true), or an internally produced EOS.

The following paragraphs explain other key elements of the program code strings. Figure 3-10 provides some examples of Data messages.

Keyboard-to-Program Code Correlation. There is a program code that corresponds to nearly every front panel key. The exceptions are DISPLAY, DISPLAY in conjunction with SEQ, Backspace, COARSE TUNE, FINE TUNE, and display HP-IB ADRS. In addition, the program code HZ is available for carrier frequency entries, RP is available to reset the reverse power protection circuitry after the source of reverse power has been removed, and R0 and R1 are available to programmatically place the instrument in the STBY and ON states, respectively.

Value-Selectable Parameters. Carrier parameters are set using a Function-Data-Units sequence of program codes, while modulation parameters are set using a Source-Function-Data-Units sequence of program codes. Single-value parameters; such as, INT 400 Hz, INT 1 kHz, and so forth, are set with a single program code sequence.

Data. The term "Data" in each program sequence refers to the numeric value and not to the entire Data message. Data can be any number of arbitrary length in fixed point notation. Digits that exceed the maximum data length for the particular function will be truncated. This maximum limit includes any embedded decimal point. In the case of the Amplitude function, this maximum limit also includes the minus sign. The minus sign is only applicable during Amplitude Data entries. Table 3-6 summarizes these input data restrictions.

Table 3-6. Input Data Restrictions

Function	Maximum Data Length	Decimal Point Allowed	Minus Sign Allowed
Frequency	9 Digits	Yes	No
Amplitude	9 Digits (1)	Yes	Yes
AM	2 Digits	Yes	No
FM	2 Digits	Yes	No
Increment Set	Same as for selected function	Yes	No

NOTES:

1. In the Amplitude function, leading zeros are not counted.
2. Unused or unidentifiable characters are ignored.
3. Either upper or lower case letters can be used in Data messages.
4. Only the following ASCII characters are recognized by the Signal Generator:

A—Z a—z 0—9 LF — . %

All other characters, including spaces, are ignored.

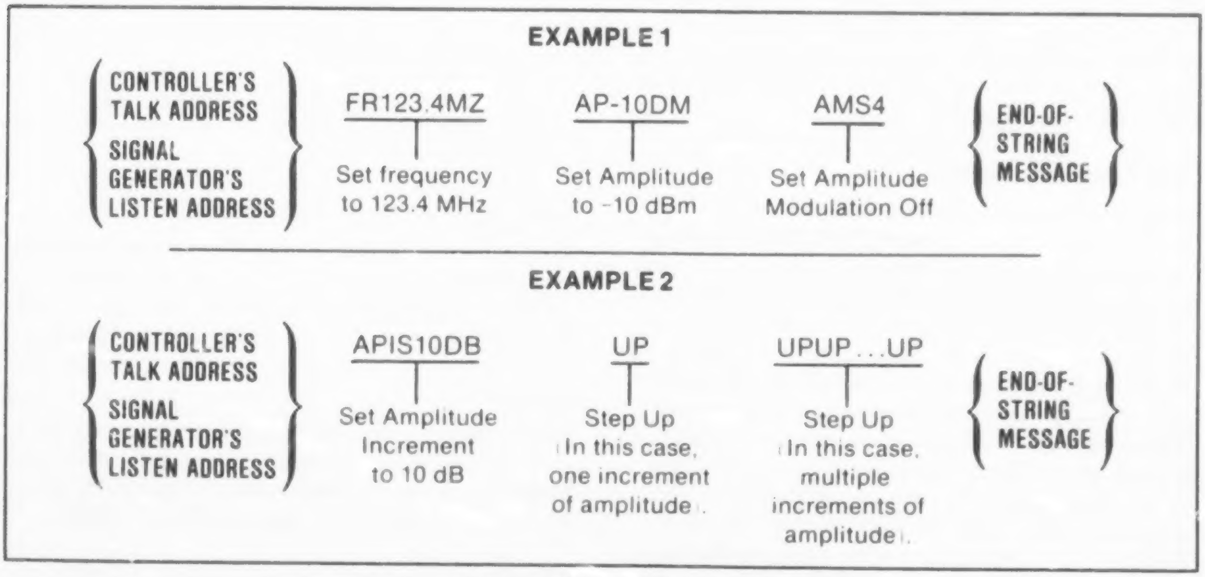

EXAMPLE 1
CONTROLLER'S TALK ADDRESS
SIGNAL GENERATOR'S LISTEN ADDRESS
FR123.4MZ
Set frequency to 123.4 MHz
AP-10DM
Set Amplitude to -10 dBm
AMS4
Set Amplitude Modulation Off
END-OF-STRING MESSAGE
EXAMPLE 2
CONTROLLER'S TALK ADDRESS
SIGNAL GENERATOR'S LISTEN ADDRESS
APIS10DB
Set Amplitude Increment to 10 dB
UP
Step Up (In this case, one increment of amplitude).
UPUP...UP
Step Up (In this case, multiple increments of amplitude).
END-OF-STRING MESSAGE

Figure 3-10. Data Message Examples

Receiving the Data Message (Cont'd)

A complete list of ASCII characters with conversions to binary, octal, decimal, and hexadecimal is provided in Table 3-10.

3-24. Sending the Data Message

The Signal Generator does not have the capability to talk; therefore, it cannot send Data messages.

3-25. Receiving the Trigger Message

The Signal Generator does not have the capability to respond to the trigger message.

3-26. Receiving the Clear Message

The Signal Generator will respond to a Clear message by setting each function parameter to the value listed in Table 3-7. The Signal Generator will respond equally to the Selected Device Clear (SDC) bus command when addressed to listen, and to the Device Clear (DCL) bus command whether addressed or not.

Table 3-7. Response to Clear Message

Parameter	Value
Carrier Frequency	100.0000 MHz
Output Amplitude	−127.0 dBm
AM Depth	0%
FM Peak Deviation Frequency	0.0 kHz
Carrier Frequency Increment	10.0000 MHz
Output Amplitude Increment	10.0 dB
AM Depth Increment	1%
FM Peak Deviation Frequency Increment	1.0 kHz
Coarse and Fine Tune Pointer	10.0000 MHz
Sequence Counter	0
All 10 Internal Storage Registers	Remain unchanged.

3-27. Receiving the Remote Message

The Remote message is comprised of two parts. First, the Remote Enable bus control line (REN) is held true, then the device listen address is sent by the controller. These two actions combine to place the Signal Generator into remote operation. Therefore, the instrument is enabled to go into remote operation when the controller begins the Remote message, but it does not actually make the transition until it is addressed to listen for the first time. All instrument settings remain unchanged when the transition from local-to-remote operation occurs.

The front panel RMT and ADRS annunciators will both light once the Signal Generator has received the Remote message and is addressed to listen.

3-28. Receiving the Local Message

The Local message is the means by which the controller sends the Go to Local (GTL) bus command. If addressed to listen, the Signal Generator will return to local operation (full front panel control) when it receives the Local message. If the instrument is in local lockout when the Local message is received, full front panel control will be returned, but local lockout will remain in effect. Unless the Signal Generator receives the Clear Lockout/Set Local message, it will return to local lockout the next time it receives a Remote message. All instrument settings remain unchanged when the transition from remote-to-local operation occurs.

The front panel RMT annunciator will be turned off when the Signal Generator switches to local operation. However, the front panel ADRS annunciator will remain lit if the Signal Generator is still being addressed to listen (whether in remote or local operation).

The front panel LOCAL key can also be used to return the Signal Generator to local operation. However, pressing the LOCAL key (when the instrument is not in local lockout) might interrupt a Data message being sent to the Signal Generator. This would leave the Signal Generator in a state unknown to the controller. This situation is undesirable and can be avoided by sending the Local Lockout message to disable the LOCAL key.

3-29. Receiving the Local Lockout Message

The Local Lockout message is the means by which the controller sends the Local Lockout (LLO) bus command. If the Signal Generator is in remote operation, it will respond to the Local Lockout message by disabling the front panel LOCAL key. Local lockout prevents the loss of data or system control due to someone accidentally pressing any of the front panel keys. If the Signal Generator is in local operation when it is enabled to remote operation (that is, REN is set true) and it receives the Local Lockout message, it will switch to remote with local lockout operation the first time it is addressed to listen. Once in local lockout, the Signal Generator can only be returned to local operation by the controller or by unplugging or resetting the instrument.

3-30. Receiving the Clear Lockout/Set Local Message

The Clear Lockout/Set Local message is the means by which the controller sets the Remote Enable bus control line (REN) false. The Signal Generator will return to local operation (full front panel control) when it receives the Clear Lockout/Set Local message. All instrument settings remain unchanged when the transition from remote with lockout to local operation occurs.

The front panel RMT annunciator will be turned off when the Signal Generator switches to local operation.

3-31. Receiving the Pass Control Message

The Signal Generator does not respond to the Pass Control message because it does not have a control capability.

3-32. Sending the Require Service Message

The Signal Generator does not have the capability to require service by setting the Service Request bus control line (SRQ) true.

3-33. Sending the Status Byte Message

The Signal Generator does not have the capability to respond to a Serial Poll Enable (SPE) bus command; therefore, it cannot send the Status Byte message.

3-34. Sending the Status Bit Message

The Signal Generator does not have the capability to respond to a Parallel Poll Enable (PPE) bus command; therefore, it cannot send the Status Bit message.

3-35. Receiving the Abort Message

The Abort message is the means by which the controller sets the Interface Clear bus control line (IFC) true. When the Abort message is received, the Signal Generator becomes unaddressed and stops listening.

3-36. Switching Characteristics

The Signal Generator's switching characteristics are an important consideration in applications involving a computer controller. For most functions, the Signal Generator has the ability to accept new Data Messages before the hardware can settle to the required output. If the timing requirements are not taken into account in the controller's program, it will be impossible in many situations to make meaningful measurements on a device driven by the Signal Generator.

Switching times for frequency, modulation and amplitude have several characteristics in com-

Table 3-8. HP-IB Program Codes (Alphabetical Order)

Program Code[1]	Parameter	Comments
AM	Amplitude Modulation	Function Entry
AP	Amplitude (carrier)	Function Entry
DB	dB	Units Entry
DF	dBf	Units Entry
DM	dBm	Units Entry
DN	Step Down (↓)	Function Feature
EM	EMF	Units Entry
FM	Frequency Modulation	Function Entry
FR	Frequency (carrier)	Function Entry
HZ	Hz	Units Entry
IS	Increment Set	Function Qualifier
KZ	kHz	Units Entry
MV	mV	Units Entry
MZ	MHz	Units Entry
PC	Percent[2]	Units Entry
RC	Recall	Feature
RP	Reverse Power Protection Reset[3]	Feature
R0	Standby[4]	Feature
R1	On[4]	Feature
SQ	Sequence	Feature
ST	Store	Feature
S1	External Modulation Source	Source Qualifier
S2	Internal 400 Hz Modulation Source	Source Qualifier
S3	Internal 1 kHz Modulation Source	Source Qualifier
S4	Modulation Source Off	Source Qualifier
UP	Step Up (↑)	Function Feature
UV	μV	Units Entry
VL	Volts	Units Entry
0—9	Numerals 0 — 9	Data Entries
–	Minus Sign	Data Entry
.	Decimal Point	Data Entry
%	Percent[2]	Units Entry

[1] Program codes can be either upper or lower case.

[2] Either PC or % can be used.

[3] The source of reverse power must be removed.

[4] The RESET/STBY/ON switch must be set to the ON position.

Switching Characteristics (Cont'd)

mon. In each case a finite amount of time passes from the command (manual or computer generated) until the required output occurs. Software execution time is required for the microprocessor and related digital circuits to process the data. This begins with a valid final terminator (keystroke or data entry) and ends with the execution in the hardware. The software time may vary considerably depending on the function. Examples are internal instructions to more than one hardware location, (may be serial, parallel or both) and differing amounts of control data and calculations.

Hardware execution time will also vary considerably. This depends on the number of circuits affected, the length of time each takes to change and whether the changes occur one at a time or concurrently.

Frequency Switching. The Signal Generator will typically be within 100 Hz of the final frequency within 2 seconds after receiving the valid units data (terminator). Figure 3-11 shows the sequence of events and the typical error frequency relative to time. Area I shows the software execution time. Areas II through IV make up the hardware execution time.

At times certain events in the frequency switching cycle may be bypassed. For example, small frequency changes will often eliminate event II, the fast slew rate mode or event IV, the FM calibration mode. However, the frequency change that allows these events to be bypassed depends on an involved algorithm that is a function of frequency band and the state of the successive approximation register of the Low Frequency Loop. Therefore, it is best to assume that the entire sequence of

Table 3-9. HP-IB Program Codes (Functional Order)

Parameter	Program Code[1]
FREQUENCY	
Frequency (carrier)	FR
AMPLITUDE	
Amplitude (carrier)	AP
MODULATION	
Amplitude Modulation	AM
Frequency Modulation	FM
External Modulation Source	S1
Internal 400 Hz Modulation Source	S2
Internal 1 kHz Modulation Source	S3
Modulation Source Off	S4
DATA	
Numerals 0 — 9	0 — 9
Minus Sign	–
Decimal Point	.
UNITS	
dB	DB
dBf	DF

Parameter	Program Code[1]
UNITS (Cont'd)	
dBm	DM
EMF	EM
Volts	VL
mV	MV
μV	UV
Hz	HZ
kHz	KZ
MHz	MZ
Percent[2]	PC
Percent[2]	%
OTHER	
Step Up (↑)	UP
Step Down (↓)	DN
Increment Set	IS
Standby[3]	R0
On[3]	R1
Store	ST
Recall	RC
Sequence	SQ
Reverse Power Protection Reset (4)	RP

[1] Program codes can be either upper or lower case.

[2] Either PC or % can be used.

[3] The RESET/STBY/ON switch must be in the ON position.

[4] The source of reverse power must be removed.

Table 3-10. Commonly Used Code Conversions

ASCII	Binary	Octal	Decimal	Hexa-decimal
NUL	00 000 000	000	0	00
SOH	00 000 001	001	1	01
STX	00 000 010	002	2	02
ETX	00 000 011	003	3	03
EOT	00 000 100	004	4	04
ENQ	00 000 101	005	5	05
ACK	00 000 110	006	6	06
BEL	00 000 111	007	7	07
BS	00 001 000	010	8	08
HT	00 001 001	011	9	09
LF	00 001 010	012	10	0A
VT	00 001 011	013	11	0B
FF	00 001 100	014	12	0C
CR	00 001 101	015	13	0D
SO	00 001 110	016	14	0E
SI	00 001 111	017	15	0F
DLE	00 010 000	020	16	10
DC1	00 010 001	021	17	11
DC2	00 010 010	022	18	12
DC3	00 010 011	023	19	13
DC4	00 010 100	024	20	14
NAK	00 010 101	025	21	15
SYN	00 010 110	026	22	16
ETB	00 010 111	027	23	17
CAN	00 011 000	030	24	18
EM	00 011 001	031	25	19
SUB	00 011 010	032	26	1A
ESC	00 011 011	033	27	1B
FS	00 011 100	034	28	1C
GS	00 011 101	035	29	1D
RS	00 011 110	036	30	1E
US	00 011 111	037	31	1F
SP	00 100 000	040	32	20
!	00 100 001	041	33	21
"	00 100 010	042	34	22
#	00 100 011	043	35	23
$	00 100 100	044	36	24
%	00 100 101	045	37	25
&	00 100 110	046	38	26
'	00 100 111	047	39	27
(	00 101 000	050	40	28
)	00 101 001	051	41	29
*	00 101 010	052	42	2A
+	00 101 011	053	43	2B
,	00 101 100	054	44	2C
—	00 101 101	055	45	2D
.	00 101 110	056	46	2E
/	00 101 111	057	47	2F
0	00 110 000	060	48	30
1	00 110 001	061	49	31
2	00 110 010	062	50	32
3	00 110 011	063	51	33
4	00 110 100	064	52	34
5	00 110 101	065	53	35
6	00 110 110	066	54	36
7	00 110 111	067	55	37
8	00 111 000	070	56	38
9	00 111 001	071	57	39
:	00 111 010	072	58	3A
;	00 111 011	073	59	3B
<	00 111 100	074	60	3C
=	00 111 101	075	61	3D
>	00 111 110	076	62	3E
?	00 111 111	077	63	3F

ASCII	Binary	Octal	Decimal	Hexa-decimal
@	01 000 000	100	64	40
A	01 000 001	101	65	41
B	01 000 010	102	66	42
C	01 000 011	103	67	43
D	01 000 100	104	68	44
E	01 000 101	105	69	45
F	01 000 110	106	70	46
G	01 000 111	107	71	47
H	01 001 000	110	72	48
I	01 001 001	111	73	49
J	01 001 010	112	74	4A
K	01 001 011	113	75	4B
L	01 001 100	114	76	4C
M	01 001 101	115	77	4D
N	01 001 110	116	78	4E
O	01 001 111	117	79	4F
P	01 010 000	120	80	50
Q	01 010 001	121	81	51
R	01 010 010	122	82	52
S	01 010 011	123	83	53
T	01 010 100	124	84	54
U	01 010 101	125	85	55
V	01 010 110	126	86	56
W	01 010 111	127	87	57
X	01 011 000	130	88	58
Y	01 011 001	131	89	59
Z	01 011 010	132	90	5A
[	01 011 011	133	91	5B
\	01 011 100	134	92	5C
]	01 011 101	135	93	5D
^	01 011 110	136	94	5E
_	01 011 111	137	95	5F
`	01 100 000	140	96	60
a	01 100 001	141	97	61
b	01 100 010	142	98	62
c	01 100 011	143	99	63
d	01 100 100	144	100	64
e	01 100 101	145	101	65
f	01 100 110	146	102	66
g	01 100 111	147	103	67
h	01 101 000	150	104	68
i	01 101 001	151	105	69
j	01 101 010	152	106	6A
k	01 101 011	153	107	6B
l	01 101 100	154	108	6C
m	01 101 101	155	109	6D
n	01 101 110	156	110	6E
o	01 101 111	157	111	6F
p	01 110 000	160	112	70
q	01 110 001	161	113	71
r	01 110 010	162	114	72
s	01 110 011	163	115	73
t	01 110 100	164	116	74
u	01 110 101	165	117	75
v	01 110 110	166	118	76
w	01 110 111	167	119	77
x	01 111 000	170	120	78
y	01 111 001	171	121	79
z	01 111 010	172	122	7A
{	01 111 011	173	123	7B
|	01 111 100	174	124	7C
}	01 111 101	175	125	7D
~	01 111 110	176	126	7E
DEL	01 111 111	177	127	7F

Switching Characteristics (Cont'd)

events shown in Figure 3-11 occurs every time a frequency change is made.

To minimize the effects of frequency hysteresis (especially near the frequency band edges), switch to the desired frequency from the same direction each time, that is, from either above or below the desired frequency. Ideally, the frequency change should be made from the same preset frequency. The main band frequency hysteresis is 100 kHz at the main band edges, that is, 123.5, 247 and 494 MHz.

During a frequency change, all modulation is turned off if the FM mode has been enabled. This applies to FM only or mixed modulation such as FM from two sources or simultaneous AM and FM. After the frequency change and FM calibration is completed, the modulation is turned on.

Amplitude Switching. During an RF amplitude change, the final level is always approached from a lower level. This means that a critical amplitude level will never be exceeded in the course of normal Signal Generator operation.

Software correction of amplitude with respect to frequency may cause the amplitude to be uncalibrated while a frequency change occurs. The software correction is implemented after the final frequency is reached.

Software execution time for an amplitude change varies considerably. The basic unit for amplitude in the Signal Generator is dBm. An input in other units requires calculations. This tends to increase the software execution time considerably. For example, an input in dBm generally will take about 160 ms from the terminator to the end of software execution. A change (increment or decrement) in dB will take a little less time, typically 130 ms. Examples of a change with calculations involved are: a preset level in mV with a change in dB, 200 ms; a level and change in mV, 340 ms; a level in dBm and a change in mV, 460 ms.

A 10 dB change without modulation (narrowband Automatic Level Control—ALC) may take up to 110 ms in the vernier hardware circuits. With modulation (wideband ALC) the switching time is typically 1 to 25 ms. The step attenuator switching time is on the order of 12 ms.

Total time requirements for simple amplitude inputs or changes, that is, minimal software and hardware execution time is 150 ms. A more complex change may take up to 560 ms.

Modulation Switching. There are applications where it is necessary to turn modulation on or off or to change to another modulation level. It takes about 400 ms for the modulation accuracy (AM or FM) to be within tolerance from the time the modulation (audio oscillator) is initially turned on. An FM deviation change typically occurs 60 ms after the final terminator (Units key) triggers the change. Turning the FM off will take about 20 ms. Amplitude modulation normally takes about 120 ms to turn off or to change to a new depth. Software execution time in the modulation mode is insignificant.

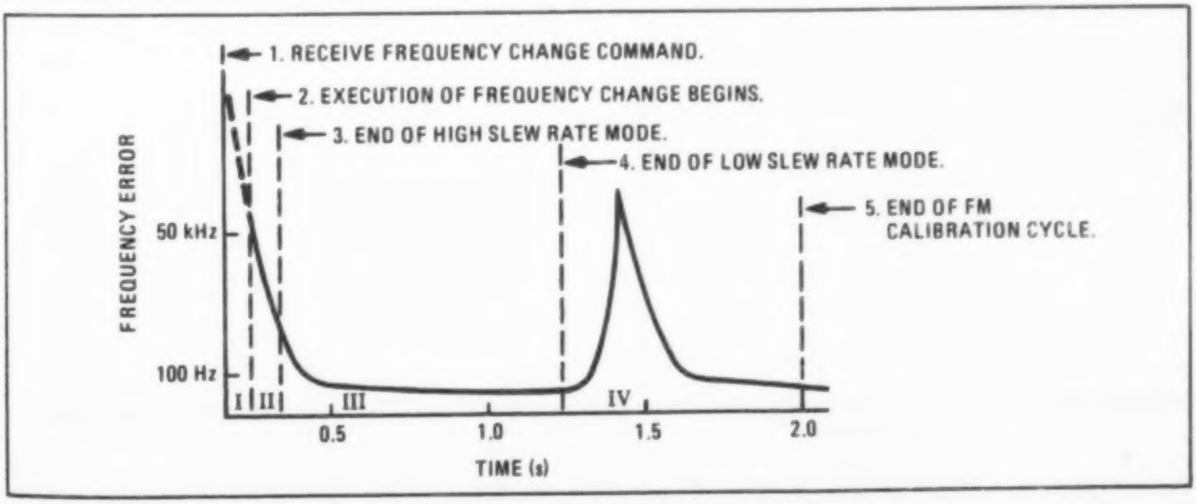


Figure 3-11. Frequency Switching Characteristics

Amplitude

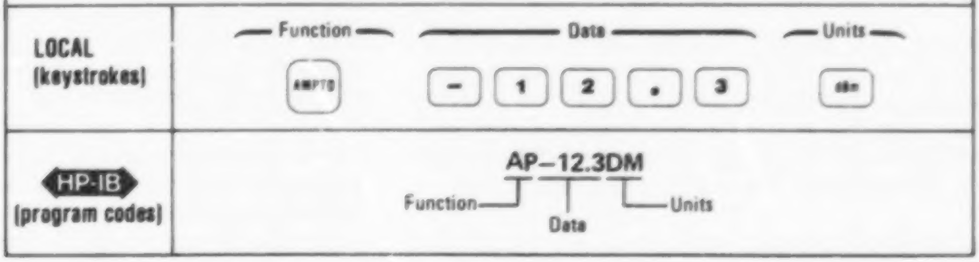
Description This instruction details how to set the output amplitude.

Operating Characteristics:
Range: +13 dBm to −127 dBm (+1.00V to +0.100 μV)
Resolution: 0.1 dB

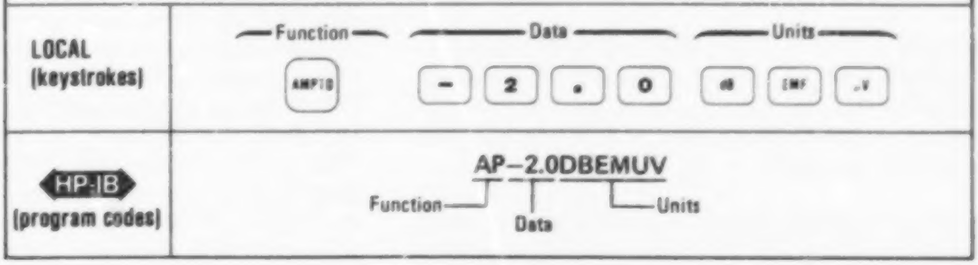
Keystroke Sequence Press and release the AMPTD Function key, the desired Data keys, and a valid Units key or combination of valid Units keys.

Examples

Set the output amplitude to −12.3 dBm.


LOCAL
(keystrokes)
Function
Data
Units
AMPTD
−
1
2
.
3
dBm
HP-IB
(program codes)
AP−12.3DM
Function
Data
Units

Set the output amplitude to −2.0 dB EMF μV.


LOCAL
(keystrokes)
Function
Data
Units
AMPTD
−
2
.
0
dB
EMF
μV
HP-IB
(program codes)
AP−2.0DBEMUV
Function
Data
Units

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
AMPTD	AP
dBm	DM
dBf	DF
dB	DB
EMF	EM
V	VL
mV	MV
μV	UV

Indications The selected output amplitude (with sign and units) will be displayed in the AMPLITUDE Display.

Comments Digits selected beyond the specified resolution of the AMPLITUDE Display will be ignored.

Amplitude (Cont'd)

Comments (Cont'd)

Leading zeros will be blanked.

Calibrated level is from −127 dBm to +13 dBm with overrange to the maximum power of the instrument.

Minus sign may be entered at any time before the final terminator.

Amplitude Data entries that would cause the peak envelope power of the instrument to exceed +17 dBm are rejected.

Amplitude function will remain selected until:

a. One of the three remaining functions is selected.

b. One of the STORE-RECALL-DISPLAY keys is pressed.

c. The instrument is reset or unplugged.

Fourteen valid units entries are possible. They are as follows:

dBm
dBf
dB V
dB mV
dB μV
dB EMF V
dB AMF mV
dB EMF μV
V
mV
μV
EMF V
EMF mV
EMF μV

Related Instructions

Amplitude Conversion
Amplitude, Up/Down

Amplitude Conversion

Description This instruction details how to change the AMPLITUDE Display from power units in dBm to any one of thirteen other valid unit configurations. This feature does not affect the actual output amplitude of the Signal Generator.

Keystroke Sequence Press any valid Units key or combination of valid Units keys with the amplitude function selected.

Example

The AMPLITUDE Display shows 10.0 dBm. Change the display to units of dB μV. (The resulting display will be 117.0 dB μV).

LOCAL (keystrokes)	—dBm——→ dB μV— dB μV Prefix Terminator Final Terminator
HP-IB (program codes)	—dBm——→ dB μV— DBUV Prefix Terminator Final Terminator

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
dBm[1]	DM[1]
dBf[1]	DF[1]
dB[2,3]	DB[2,3]
EMF[2]	EM[2]
V[1]	VL[1]
mV[1]	MV[1]
μV[1]	UV[1]

[1] Final Terminator.

[2] Prefix Terminator.

[3] Final Terminator for Increment Set Mode.

Indications The AMPLITUDE Display will change to reflect the newly selected units and the corresponding annunciator(s) will light.

Comments The amplitude function must be selected before the conversion entry or entries are made.

Logarithmic Data entries (dBm or dBf) will be displayed in the AMPLITUDE Display with 0.1 dB resolution.

The dBm or dBf Units terminator overrides a dB or EMF terminator.

If a dB or EMF Units terminator is selected, the AMPLITUDE Display will be blanked, the corresponding annunciator will light, and the Signal Generator will wait for a final terminator to be entered.

Amplitude Conversion (Cont'd)

Comments (Cont'd)

Linear Data entries (V, mV, or µV) will be displayed in the three most significant digits of the AMPLITUDE Display and the linear terminator will be autoranged (or adjusted) to comply with this condition.

Conversion formulas used are as follows:

$\text{dBm} = \text{dBm}$
$\text{dBf} = \text{dBm} + 120.0$
$\text{dB V} = \text{dBm} - 13.0$
$\text{dB mV} = \text{dBm} + 47.0$
$\text{dB}\ \mu\text{V} = \text{dBm} + 107.0$
$\text{dB EMF V} = \text{dBm} - 7.0$
$\text{dB EMF mV} = \text{dBm} + 53.0$
$\text{dB EMF}\ \mu\text{V} = \text{dBm} + 113.0$
$\text{V} = 10^{(\text{dBm} - 13.0)/20}$
$\text{mV} = 10^{(\text{dBm} + 47.0)/20}$
$\mu\text{V} = 10^{(\text{dBm} + 107.0)/20}$
$\text{EMF V} = 10^{(\text{dBm} - 7.0)/20}$
$\text{EMF mV} = 10^{(\text{dBm} + 53.0)/20}$
$\text{EMF}\ \mu\text{V} \quad 10^{(\text{dBm} + 113.0)/20}$

Related Instructions

Amplitude
Amplitude, Up/Down

Amplitude, Up/Down

Description This instruction details how to change the output amplitude by the value stored in the internal output amplitude increment register.

Keystroke Sequence Press and release the step up or step down keys associated with the output amplitude function.

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
AMPTD ▲ ▼	AP UP DN

NOTE

During remote operation, repeated UP or DN codes can be sent over the bus once the frequency function has been selected.

Indications The output amplitude shown in the AMPLITUDE Display and the output of the Signal Generator will change by the value stored in the internal output amplitude increment register.

Comments Step up and step down keys associated with the output amplitude function are used to change the output amplitude by the value stored in the internal output amplitude increment register.

Places the instrument in the Amplitude Data entry mode and clears any previously selected function.

Continues to change the output amplitude by the value stored in the internal output amplitude increment register if either key remains pressed.

Initialized value and limits of the output amplitude increment are as follows:

Initialized Value	Minimum Value	Maximum Value
10.0 dB	0.1 dB	≤144.0 dB
	0.001 μV	≤1.57V
	0.001 EMF μV	≤3.15 EMF V

Related Instructions Increment Value Change
Increment Value Display

Display

Description This instruction details how to selectively display the stored contents of an internal storage register.

Keystroke Sequence Press and release the DISPLAY key, then press and hold the Data key (a single digit register number 0—9).

Example

Display the stored contents from register 2.	
LOCAL (keystrokes)	— Display Contents of Register 2 — DISPLAY 2
HP-IB (program codes)	This feature is not accessible via HP-IB.

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
DISPLAY	None

Indications The stored contents from the selected register will be displayed as long as the Data key remains pressed.

Comments Ten internal registers are available (0—9). Each is capable of storing complete front panel setups (exclusive of increment settings).

Does not affect the actual output of the Signal Generator.

Does not change the contents of the internal sequence counter.

Does not affect the current increment settings.

Clears any previously selected function.

Feature is not accessible via HP-IB.

All displays are restored to reflect the actual Signal Generator output when the Data key is released.

Related Instructions

Display Sequence
Recall
Sequence
Store

Display Sequence

Description This instruction details how to display the contents of the internal sequence counter.

Keystroke Sequence Press and release the DISPLAY key, then press and hold the SEQ key.

Example

Display the contents of the internal sequence counter.	
LOCAL (keystrokes)	— Display Sequence Counter Contents — DISPLAY SEQ
HP-IB (program codes)	This feature is not accessible via HP-IB.

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
DISLPAY	None
SEQ	None

Indications The stored contents from the sequence counter will be displayed in the least significant digit of the AMPLITUDE Display as long as the SEQ key remains pressed.

Comments Does not affect the actual output of the Signal Generator.

Does not change the contents of the internal sequence counter.

Clears any previously selected function.

Feature is not accessible via HP-IB.

The AMPLITUDE Display is restored to reflect the actual Signal Generator output when the SEQ key is released.

Related Instructions Display
Sequence

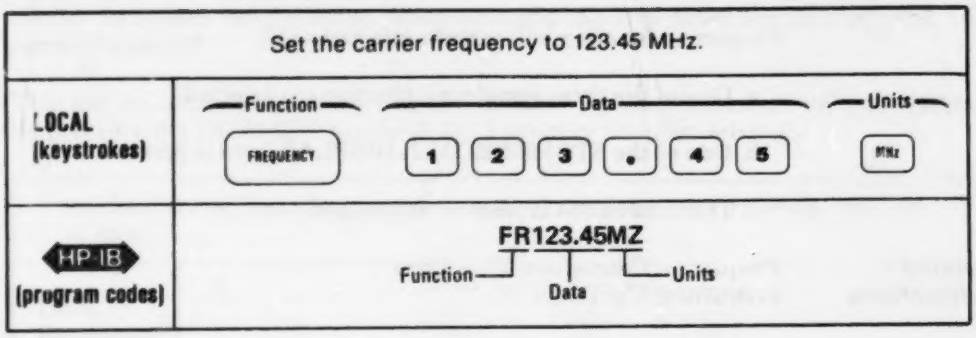
Frequency

Description This instruction details how to set the carrier frequency.

Operating Characteristics:
Range: 100 kHz to 990 MHz (990.0000 MHz)
Resolutions: 100 Hz and 250 Hz, depending on the carrier frequency selected.

Keystroke Sequence Press and release the FREQUENCY Function key, the desired Data keys, and a valid Units key.

Example



Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
FREQUENCY	FR
MHz	MZ
kHz	KZ
No key	HZ

Indications The selected carrier frequency will be displayed in megahertz in the FREQUENCY Display.

Comments Least significant (eighth) digit will be blanked when the selected carrier frequency is a multiple of 100 Hz.

In cases where the selected carrier frequency is a multiple of 250 Hz, the least significant digit will be a 5.

Digits selected beyond the specified resolution of the FREQUENCY Display will be truncated.

Leading zeros will be blanked.

Carrier frequencies below 100 kHz will result in an uncalibrated output amplitude.

The MODULATION Display will flash if a change in carrier frequency would cause the FM peak deviation frequency allowed for that frequency band to be exceeded. Entering a carrier frequency that would set the instrument in the correct band for the selected deviation frequency will clear the error condition, or pressing one of the following keys will automatically adjust the FM peak deviation frequency to the maximum frequency possible for that frequency band.

Frequency (Cont'd)

Comments (Cont'd)

Band	Carrier Frequency (MHz)
1	0.1 — 123.5
2	123.5 — 247
3	247 — 494
4	494 — 990

FM ▲ ▼

The carrier frequency increment is rejected if it is not a multiple of 100 Hz or 250 Hz.

Frequency function will remain selected until:

a. One of the three remaining functions is selected.

b. One of the STORE-RECALL-DISPLAY keys is pressed.

c. The instrument is reset or unplugged.

Related Instructions

Frequency, Coarse and Fine Tune
Frequency, Up/Down

Frequency, Coarse and Fine Tune

Description This instruction details how to quickly tune the carrier frequency in decade steps using the step up and step down keys associated with the carrier frequency function.

Keystroke Sequence This feature is enabled by pressing either the COARSE TUNE or FINE TUNE key.

Pressing either key will increase (COARSE TUNE) or decrease (FINE TUNE) the carrier frequency tuning value by a factor of 10.

Pressing the step up key will then increase the carrier frequency by the newly selected carrier frequency tuning value, while pressing the step down key will decrease the carrier ferquency.

This feature is disabled and the original carrier frequency increment value is enabled by pressing the INCR SET key (with the frequency function selected).

Example

Enable a carrier frequency tuning value of 10 kHz (assuming a starting value of 10 MHz).	
LOCAL (keystrokes)	Decrease Tuning Value FINE TUNE ÷10 FINE TUNE ÷10 FINE TUNE ÷10
HP-IB (program codes)	This feature is not accessible via HP-IB.

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
FREQUENCY	None
COARSE TUNE	None
FINE TUNE	None
⬆	None
⬇	None
INCR SET	None

Indications Whenever the COARSE TUNE or FINE TUNE key is pressed and held, the frequency digit that corresponds to the carrier frequency tuning value will flash.

When the COARSE TUNE key is pressed again, the next digit to the left will flash to indicate the new tuning value.

When the FINE TUNE key is pressed again, the next digit to the right will flash to indicate the new tuning value.

Comments Feature only applies to the carrier frequency function.

Feature is not accessible via HP-IB.

Frequency, Coarse and Fine Tune (Cont'd)

Comments (Cont'd)

COARSE TUNE and FINE TUNE keys are always available to change the carrier frequency tuning value by a factor of 10.

Places the instrument into the frequency Data entry mode and clears any previously selected function, once either the step up or step down key is pressed.

Enables the last valid carrier frequency increment value when the INCR SET key is pressed.

Related Instructions

Frequency
Frequency, Up/Down
Increment Value Change

HP-IB

Frequency, Up/Down

Description This instruction details how to change the carrier frequency by the value stored in the internal carrier frequency increment register.

Keystroke Sequence Press and release the step up or step down keys associated with the carrier frequency function.

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
FREQUENCY	FR
▲	UP
▼	DN

NOTE

During remote operation, repeated UP or DN codes can be sent over the bus once the frequency function has been selected.

Indications The carrier frequency shown in the FREQUENCY Display and the output of the Signal Generator will change by the value stored in the internal carrier frequency increment register.

Comments Step up and step down keys associated with the carrier frequency function are used to change the carrier frequency by the value stored in the internal carrier frequency increment register.

Places the instrument in the Frequency Data entry mode and clears any previously selected function.

Continues to change the carrier frequency by the value stored in the internal carrier frequency increment register if either key remains pressed.

The MODULATION Display will flash if a change in carrier frequency would cause the FM peak deviation frequency allowed for that frequency band to be exceeded. Entering a carrier frequency that would set the instrument in the correct band for the selected deviation frequency will clear the error condition, or pressing one of the following keys will automatically adjust the FM peak deviation frequency to the maximum frequency possible for that frequency band.

Band	Carrier Frequency (MHz)
1	0.1—123.5
2	123.5—247
3	247—494
4	494—990

FM ▲ ▼

Initialized value and limits of the carrier frequency increment are as follows:

Initialized Value	Minimum Value	Maximum Value
10.0000 MHz	0.1 kHz	≤989.99 MHz

Related Instructions

Frequency, Coarse and Fine Tune
Increment Value Change
Increment Value Display

HP-IB

HP-IB Address Display

Description This instruction details how to display the internally-set, decimal HP-IB address.

Keystroke Sequence Press and hold the HP-IB ADRS key.

Example

Display the internally-set, decimal HP-IB address.	
LOCAL (keystrokes)	—Display HP-IB Address— HP-IB ADRS
HP-IB (program codes)	This feature is not accessible via HP-IB.

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
HP-IB ADRS	None

Indications The internally-set, decimal HP-IB address will be displayed in the MODULATION Display as long as the HP-IB ADRS key remains pressed.

Comments HP-IB addresses greater than 30 (decimal) are interpreted as 30.

HP-IB address is factory-set to 07 decimal. (In binary, this is 00111, the equivalent ASCII character is an apostrophe).

HP-IB address is updated only when the instrument is powered up or reset.

To change the HP-IB address, refer to paragraph 2-8, HP-IB Address Selection.

Feature is not accessible via HP-IB.

The MODULATION Display is restored to reflect the actual Signal Generator output when the HP-IB ADRS key is released.

HP-IB Address Display (Cont'd)

Comments (Cont'd)

Allowable HP-IB Address Codes

ADDRESS SWITCH					EQUIVALENT ASCII CHARACTER (LISTEN)	EQUIVALENT DECIMAL VALUE (LISTEN)
A5	A4	A3	A2	A1		
0	0	0	0	0	SP	00
0	0	0	0	1	!	01
0	0	0	1	0	“	02
0	0	0	1	1	#	03
0	0	1	0	0	$	04
0	0	1	0	1	%	05
0	0	1	1	0	&	06
0	0	1	1	1	'	07
0	1	0	0	0	(	08
0	1	0	0	1	)	09
0	1	0	1	0	*	10
0	1	0	1	1	+	11
0	1	1	0	0	,	12
0	1	1	0	1	–	13
0	1	1	1	0	.	14
0	1	1	1	1	/	15
1	0	0	0	0	0	16
1	0	0	0	1	1	17
1	0	0	1	0	2	18
1	0	0	1	1	3	19
1	0	1	0	0	4	20
1	0	1	0	1	5	21
1	0	1	1	0	6	22
1	0	1	1	1	7	23
1	1	0	0	0	8	24
1	1	0	0	1	9	25
1	1	0	1	0	:	26
1	1	0	1	1	;	27
1	1	1	0	0	<	28
1	1	1	0	1	=	29
1	1	1	1	0	>	30

▨ Indicates factory-set address.

Related Instructions None

HP-IB

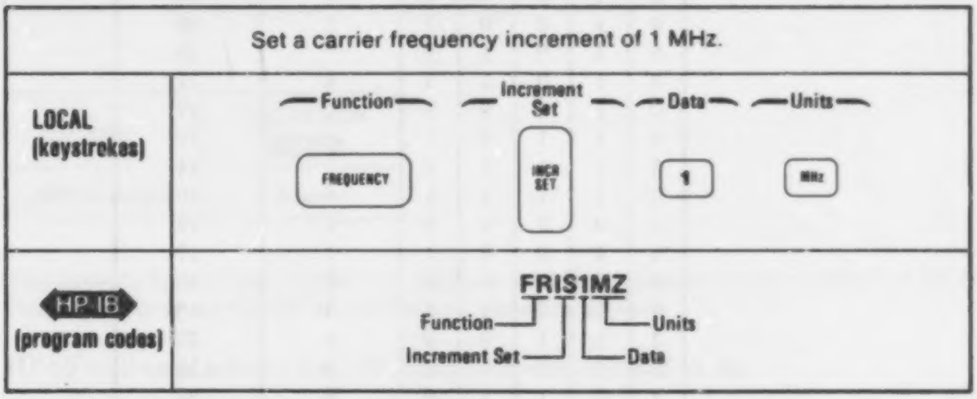
Increment Value Change

Description This instruction details how to change the value of the stored increments which are controlled by the step up and step down keys associated with each of the four main functions. Increment values for the carrier frequency, output amplitude, AM depth, and FM peak deviation frequency can be stored. The initialized value of each stored increment is listed as follows:

Carrier Frequency	10.0000 MHz
Output Amplitude	10.0 dB
AM Depth	1%
FM Peak Deviation Frequency	1.0 kHz

Keystroke Sequence Press and release a Function key, the INCR SET key, the desired Data keys, and a valid Units key.

Example


Set a carrier frequency increment of 1 MHz.

LOCAL (keystrokes)
Function
Increment Set
Data
Units
FREQUENCY
INCR SET
1
MHz
HP-IB (program codes)
FRIS1MZ
Function
Increment Set
Data
Units

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB	Keys	Program Codes HP-IB
INCR SET	IS	%	PC or %
FREQUENCY	FR	dBm	DM
AMPTD	AP	dBf	DF
AM	AM	dB	DB
FM	FM	EMF	EM
MHz	MZ	V	VL
kHz	KZ	mV	MV
No Key	HZ	μV	UV

Indications The value of the increment will appear in the display associated with the selected function as the data is entered.

Comments The frequency increment is rejected if it is not a multiple of 100 Hz or 250 Hz.

FM peak deviation frequency increments must be selected in units of kHz only.

Increment Value Change (Cont'd)

Comments (Cont'd)

The minimum allowable increment value for each of the four main functions is listed as follows:

Carrier Frequency	0.1 kHz
Output Amplitude	0.1 dB
	0.01 µV
	0.001 EMF µV
AM Depth	1%
FM Peak Deviation Frequency	0.1 kHz

The maximum allowable increment value for each of the four main functions is listed as follows:

Carrier Frequency	≤989.99 MHz
Output Amplitude	≤144.0 dB
	≤1.57V
	≤3.15 EMFV
AM Depth	≤99%
FM Peak Deviation Frequency	≤99 kHz

All displays will be restored to reflect the actual Signal Generator output as soon as a valid increment terminator is selected.

Related Instructions

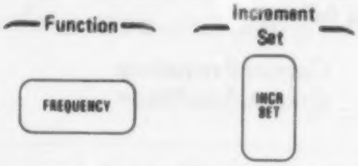
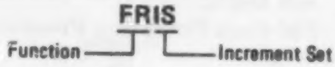
Amplitude, Up/Down
Frequency, Coarse and Fine Tune
Frequency, Up/Down
Modulation, AM Up/Down
Modulation, FM Up/Down
Increment Value Display

Increment Value Display

Description This instruction details how to display the stored value of the increments which are controlled by the step up and step down keys associated with each of the four main functions. Increment values for the carrier frequency, output amplitude, AM depth, and FM peak deviation frequency can be displayed.

Keystroke Sequence Press and release a Function key, then press and hold the INCR SET key.

Example

Display the stored carrier frequency increment.	
LOCAL (keystrokes)	
HP-IB (program codes)	

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
INCR SET	IS
FREQUENCY	FR
AMPTD	AP
AM	AM
FM	FM

Indications The stored value of the increment will be displayed in the display associated with the selected function as long as the INCR SET key remains pressed.

Comments The initialized value of each stored increment is listed as follows:

Carrier Frequency	10.0000 MHz
Output Amplitude	10.0 dB
AM Depth	1%
FM Peak Deviation Frequency	1.0 kHz

The display will be restored to reflect the actual Signal Generator output when the INCR SET key is released.

Related Instructions Increment Value Change

Modulation, AM

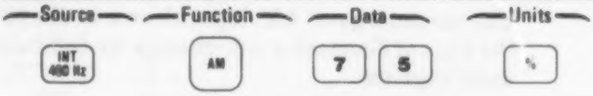
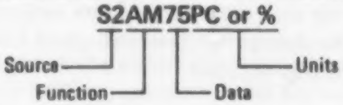
Description This instruction details how to select amplitude modulation using the internal modulation source.

Operating Characteristics:

Depth: 0 — 99% to +7 dBm
0 — 30% to +10 dBm
Resolution: 1%
Rate (internal): 400 Hz and 1 kHz, ±3%

Keystroke Sequence Press and release an Internal Source key, the AM Function key, the desired Data keys, and a valid Units key.

Example

Select AM with a depth of 75% using the internal 400 Hz source.	
LOCAL (keystrokes)	
HP-IB (program codes)	

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
INT 400 Hz	S2
INT 1 kHz	S3
AM	AM
%	PC or %

Indications Selected AM depth will be displayed in the MODULATION Display and the source annunciators (INT AM, 400 Hz, and %) will light.

Comments Digits selected beyond the specified resolution for AM depth will be truncated.

Leading zeros will be blanked.

AM depth Data entries that would cause the peak envelope power of the instrument to exceed +17 dBm are rejected.

AM function will remain selected until:

a. One of the three remaining functions is selected.

b. One of the STORE-RECALL-DISPLAY keys is pressed.

c. The instrument is reset or unplugged.

d. The External Source key may be selected in place of the Internal Source key.

Related Instructions

Modulation, AM Up/Down
Modulation, External Source
Modulation, Mixed
Modulation, Off

Modulation, AM Up/Down

Description

This instruction details how to change the percentage of AM depth by the value stored in the internal AM depth increment register.

Keystroke Sequence

Press and release the step up or step down keys associated with the amplitude modulation function.

Keys and Program Codes HP IB

Keys	Program Codes HP IB
AM	AM
▲	UP
▼	DN

NOTE

During remote operation, repeated UP or DN codes can be sent over the bus once the AM function has been selected.

Indications

The percentage of AM depth shown in the MODULATION Display and the output of the Signal Generator will change by the value stored in the internal AM depth increment register.

Comments

Step up and step down keys associated with the amplitude modulation function are used to change the percentage of AM depth by the value stored in the internal AM depth increment register.

Places the instrument in the AM Data entry mode and clears any previously selected function.

Selects default modulation source (internal 1 kHz) if no other source is selected.

Continues to change the percentage of AM depth by the value stored in the internal AM depth increment register if either key remains pressed.

Will automatically stop incrementing when the maximum percentage of AM depth permitted for a selected output amplitude is reached.

Initialized value and limits of the AM depth increment are as follows:

Initialized Value	Minimum Value	Maximum Value
1%	1%	≤99%

Related Instructions

Increment Value Change
Increment Value Display

Modulation, External Source

Description

This instruction details how to apply an external modulation signal via the front panel MOD INPUT/OUTPUT connector.

Operating Characteristics:

Rate (for AM or FM): 25 Hz to 25 kHz; 1 dB bandwidth; ac coupled
Input Impedance: 600 ohms (resistive)
Input Level: 1 Vpk (0.707 Vrms)

Keystroke Sequence

Press and release the EXT key to enable the front panel MOD INPUT/OUTPUT connector, then set the signal level of the external modulation source to 1 Vpk (0.707 Vrms) for calibrated internal control of the AM depth or FM peak deviation frequency.

Keys and Program Codes

HP-IB

Keys	Program Codes HP-IB
EXT	S1
AM	AM
%	PC or %
FM	FM
kHz	KZ

Indications

The HI EXT annunciator will light if the external modulation signal is greater than 1.02 Vpk (0.721 Vrms) and the LO EXT annunciator will light if the signal is less than 0.98 Vpk (0.693 Vrms).

NOTE

If greater accuracy is required, use a calibrated voltmeter to measure the external modulation signal.

Comments

In addition to being able to accept an external modulation signal, the MOD INPUT/OUTPUT connector provides access to the internally generated 400 Hz or 1 kHz signal whenever either is selected and the external modulation source is not selected. Its signal level is 1 Vpk (0.707 Vrms) and it cannot be adjusted by the operator.

Related Instructions

Modulation, AM
Modulation, FM
Modulation, Mixed
Modulation, Off

Modulation, FM

Description

This instruction details how to select frequency modulation using the internal modulation source.

Operating Characteristics:

Peak Deviation:

Carrier Frequency (MHz)	Maximum Peak Deviation	
	Rates ≥60 Hz	Rates <60 Hz
0.1 — 123.5	99 kHz	1600 x Rate
123.5 — 247	25 kHz	400 x Rate
247 — 494	50 kHz	800 x Rate
494 — 990	99 kHz	1600 x Rate

Resolution: 0.1 kHz for peak deviations <10 kHz
1 kHz for peak deviations ≥10 kHz

Rate (internal): 400 Hz or 1 kHz, ±3%

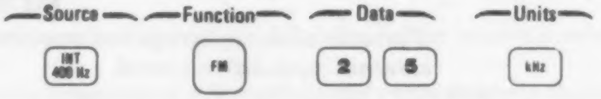
Keystroke Sequence

Press and release an Internal Source key, the FM Function key, the desired Data keys, and a valid Units key.

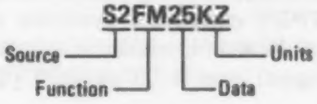
Example

Select FM with a peak deviation frequency of 25 kHz using the internal 400 Hz source.

LOCAL (keystrokes)



HP-IB (program codes)



Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
INT 400 Hz	S2
INT 1 kHz	S3
FM	FM
kHz	KZ

Indications

Selected FM peak deviation frequency will be displayed in the MODULATION Display and the source annunciators (INT FM, 400 Hz, and 1 kHz) will light.

Comments

Digits selected beyond the specified resolution for FM peak deviation will be truncated.

Leading zeros will be blanked.

Modulation, FM (Cont'd)

Comments (Cont'd)

FM peak deviation Data entries that would be out of range for the selected carrier frequency are rejected.

The MODULATION Display will flash if a change in carrier frequency would cause the FM peak deviation frequency allowed for that frequency band to be exceeded. Entering a carrier frequency that would set the instrument in the correct band for the selected deviation frequency will clear the error condition, or pressing one of the following keys will automatically adjust the FM peak deviation frequency to the maximum frequency possible for that frequency band.

Band	Carrier Frequency MHz
1	0.1 — 123.5
2	123.5 — 247
3	247 — 494
4	494 — 990

FM ▲ ▼

FM function will remain selected until:

a. One of the three remaining functions is selected.

b. One of the STORE-RECALL-DISPLAY keys is pressed.

c. The instrument is reset or unplugged.

d. The External Source key may be selected in place of the Internal Source key.

Related Instructions

Modulation, FM Up/Down
Modulation, External Source
Modulation, Mixed
Modulation, Off

Modulation, FM Up/Down

Description

This instruction details how to change the FM peak deviation frequency by the value stored in the internal FM peak deviation frequency increment register.

Keystroke Sequence

Press and release the step up or step down keys associated with the frequency modulation function.

Keys and Program Codes

HP-IB

Keys	Program Codes HP-IB
FM	FM
▲	UP
▼	DN

NOTE

During remote operation, repeated UP or DN codes can be sent over the bus once the FM function has been selected.

Indications

The FM peak deviation frequency shown in the MODULATION Display and the output of the Signal Generator will change by the value stored in the internal FM peak deviation frequency increment register.

Comments

Step up and step down keys associated with the frequency modulation function are used to change the FM peak deviation frequency by the value stored in the internal FM peak deviation frequency increment register.

Places the instrument in the FM Data entry mode and clears any previously selected function.

Selects default modulation source (internal 1 kHz) if no other source is selected.

Continues to change the FM peak deviation frequency by the value stored in the internal FM peak deviation frequency increment register if either key remains pressed.

Will automatically stop incrementing when the maximum FM peak deviation frequency permitted for a selected carrier frequency is reached.

If an out of range condition exists (MODULATION Display flashing), pressing either the step up or step down (or FM) key will automatically select the maximum FM peak deviation frequency permitted for the currently selected carrier frequency.

Initialized value and limits of the FM peak deviation frequency are as follows:

Initialized Value	Minimum Value	Maximum Value
1.0 kHz	0.1 kHz	≤99 kHz

Related Instructions

Increment Value Change
Increment Value Display

Modulation, Mixed

Description

These instructions detail the selection of mixed modulation. Modulation can be selected in one of four ways

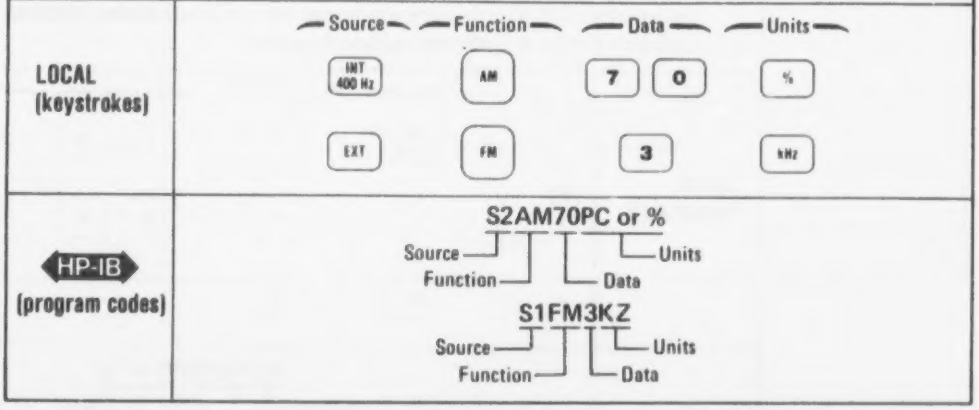
1. Simultaneous AM and FM may be selected using common or separate modulation sources (rate).
2. Simultaneous AM or FM at two rates may be selected by using internal and external modulation sources. Only one AM depth or one FM deviation can be selected.
3. Three simultaneous modulation signals, AM and FM using a common source (rate) and either AM or FM from a separate source, may be selected.
4. Four simultaneous modulation signals, two AM and two FM, may be selected. Each AM/FM pair must have a common modulation source (rate). Only one AM depth and one FM deviation can be selected.

Keystroke Sequence 1

To select simultaneous AM and FM, press and release the Source key to provide the desired AM rate, the AM Function key, the desired Data keys and the % Units key. Then press and release the Source key to provide the desired FM rate, the FM Function key, the desired Data keys and the kHz Units key. (The Source key need not be pressed for FM if the AM and FM rate is the same.)

Example 1

Simultaneously select AM with a depth of 70% and FM with a peak deviation frequency of 3 kHz using the internal 400 Hz source, and an external 1 kHz source respectively.



S2AM70PC or %

S1FM3KZ

Keystroke Sequence 2

To select simultaneous AM or FM, press and release the desired Source key, the desired Function key, the desired Data keys and a valid Units key. Then press and release the other Source key and the same Function key that was selected previously.

Modulation, Mixed (Cont'd)

Example 2

Select FM with a peak deviation frequency of 5 kHz using both an internal 1 kHz modulation source and an external 150 Hz modulation source.				
	Source	Function	Data	Units
LOCAL (keystrokes)	INT 1 kHz	FM	5	kHz
	EXT	FM		
HP-IB (program codes)	S3FM5KZ Source Function Units Data S1FM Source Function			

Keystroke Sequence 3 To select three simultaneous modulation signals, AM and FM using a common source (rate) and AM or FM from a separate source, press and release the Source key to provide the common AM and FM rate. Then press a Function key, the desired Data keys and the valid Units key. Press the other Function key, the desired Data keys and the valid Units key. Press and release the other Source key, the appropriate Function key, the desired Data keys and the valid Units key.

Example 3

Simultaneously select AM with a depth of 90% and FM with a peak deviation frequency of 25 kHz using the internal 400 Hz source, and AM with a depth of 90% using an external 6 kHz modulation source.				
	Source	Function	Data	Units
LOCAL (keystrokes)	INT 400 Hz	AM	9 0	%
		FM	2 5	kHz
	EXT	AM		
HP-IB (program codes)	S2AM90PC or % Source Function Units Data FM25KZ Function Data Units S1AM Source Function			

Modulation, Mixed (Cont'd)

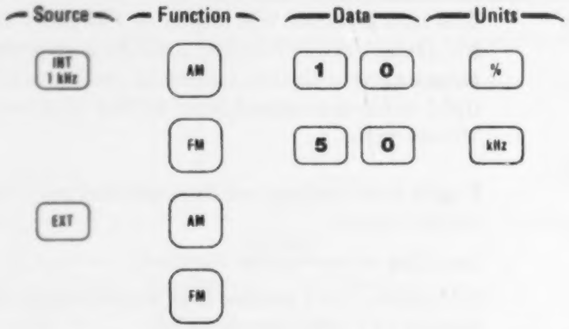
Keystroke Sequence 4

To select four simultaneous modulation signals, press and release the appropriate Source key, a Function key, the desired Data keys and the valid Units key. Press and release the other Function key, the desired Data keys and valid Units key. Press and release the other Source key, and then both Function keys.

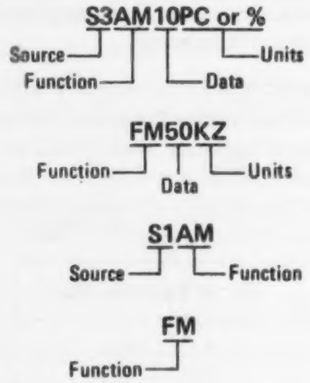
Example 4

Simultaneously select AM with a depth of 10% and FM with a peak deviation of 50 kHz using the internal 1 kHz modulation source. AM and FM with the same depth and deviation as selected previously are also selected using an external 5 kHz source.

LOCAL (keystrokes)


Source
Function
Data
Units
INT 1 kHz
AM
1
0
%
FM
5
0
kHz
EXT
AM
FM

HP-IB (program codes)


S3AM10PC or %
Source
Function
Data
Units
FM50KZ
Function
Data
Units
S1AM
Source
Function
FM
Function

Modulation, Mixed (Cont'd)

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
AM	AM
FM	FM
EXT	S1
INT 400 Hz	S2
INT 1 kHz	S3

Indications

The last selected AM depth or FM peak deviation frequency will be displayed in the MODULATION Display and the source annunciators will light. In the case where an external modulation source is used, the HI EXT and LO EXT annunciators will also light until the signal level of the external source has been adjusted to 1 Vpk (0.707 Vrms) ±5%.

Comments

Digits selected beyond the specified resolution for AM depth or FM peak deviation will be truncated.

Leading zeros will be blanked.

AM depth Data entries that would cause the peak envelope power of the instrument to exceed +17 dBm are rejected.

FM peak deviation Data entries that would be out of range for the selected carrier frequency are rejected.

The MODULATION Display will flash if a change in carrier frequency would cause the FM peak deviation frequency allowed for that frequency band to be exceeded. Entering a carrier frequency that would set the instrument in the correct band for the selected deviation frequency will clear the error condition, or pressing one of the following keys will automatically adjust the FM peak deviation frequency to the maximum frequency possible for that frequency band.

Band	Carrier Frequency MHz
1	0.1 — 123.5
2	123.5 — 247
3	247 — 494
4	494 — 990

FM ▲ ▼

AM or FM function will remain selected until:

a. One of the three remaining functions is selected.

b. One of the STORE-RECALL-DISPLAY keys is pressed.

c. The instrument is reset or unplugged.

Setting the level of the external modulation source is described under Modulation, External Source.

Related Instructions

Modulation, AM
Modulation, AM Up/Down
Modulation, External Source
Modulation, FM
Modulation, FM Up/Down
Modulation, OFF

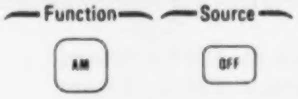
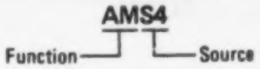
Modulation, OFF

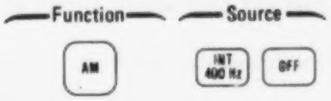
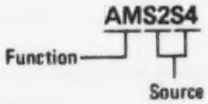
Description This instruction details how to selectively turn off the AM or FM function. In addition, it details how to selectively turn off a modulation source.

Keystroke Sequences To turn off a modulation function (AM or FM), press and release the associated Function key, then the OFF key.

To turn off a modulation source, press and release the associated Function key, Source key, then the OFF key.

Examples

Selectively turn off AM modulation function with only one modulation source in use.	
LOCAL (keystrokes)	 Function Source AM OFF
HP-IB (program codes)	 AMS4 Function Source

Selectively turn off internal 400 Hz source.	
LOCAL (keystrokes)	 Function Source AM INT 400 Hz OFF
HP-IB (program codes)	 AMS2S4 Function Source

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
AM	AM
FM	FM
EXT	S1
INT 400 Hz	S2
INT 1 kHz	S3
OFF	S4

Indications The current MODULATION Display will be blanked or the modulation source (including its annunciator) will be turned off when the OFF key is pressed.

Modulation, OFF (Cont'd)

Comments

Currently selected modulation function (AM or FM) will be turned off when the OFF key is pressed provided only one source (internal 400 Hz or 1 kHz or external) has been selected for use.

If more than one source has been selected, then a Source key (INT 400 Hz, INT 1 kHz, or EXT) has to be pressed before the OFF key is pressed. In this case, the currently selected modulation function will remain selected and only the chosen source (including its annunciator) will be turned off.

If both modulation functions are simultaneously selected and share the same source, then only the currently selected modulation function will be turned off when the OFF key is pressed and the MODULATION Display will be restored to show the modulation parameters of the remaining function.

Related Instructions

Modulation, AM Up/Down
Modulation, FM Up/Down
Modulation, External Source
Modulation, Mixed

Recall

Description This instruction details how to selectively recall the stored contents from an internal storage register.

Keystrcke Sequence Press and release the RECALL key, then a Data key (a single digit register number 0—9).

Example

Recall the stored contents from register 2.	
LOCAL (keystrokes)	Recall Contents from Register 2 RECALL 2
HP-IB (program codes)	RC2 Recall Contents from Register 2

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
RECALL	RC

Indications The stored contents from the selected register will be recalled and the output of the Signal Generator will be changed so that it agrees with the recalled parameter values.

Comments Ten internal registers are available (0—9). Each is capable of storing complete front panel setups (exclusive of increment settings).

Clears any previously selected function.

Updates the contents of the internal sequence counter so that it agrees with the numerical location of the recalled register.

Does not affect the current increment settings.

Related Instructions

Display
Store
Sequence

Sequence

Description

This instruction details how to sequentially recall the stored contents from each of the internal storage registers.

Keystroke Sequence

Press and release the SEQ key.

Example

Sequentially recall the stored contents from each of the internal storage registers.	
LOCAL (keystrokes)	Recall Contents from Next Sequential Storage Register SEQ
HP-IB (program codes)	SQ Recall Contents from Next Sequential Storage Register

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
SEQ	SQ

Indications

The stored contents from each internal storage register will be recalled and the output of the Signal Generator will be changed so that it agrees with the recalled parameter values.

Comments

Ten internal registers are available (0—9). Each is capable of storing complete front panel setups (exclusive of increment settings).

Does not clear any previously selected function.

Updates the contents of the internal sequence counter so that it agrees with the numerical location of the recalled register.

Does not affect the current increment settings.

Remote sequence operation is permitted through an external switch closure connected at the rear panel SEQ connector J5.

Related Instructions

Display
Display Sequence
Recall
Store

Store

Description This instruction details how to store complete front panel setups (exclusive of increment settings) for either selectable or sequential recall or display at a later time.

Keystroke Sequence Press and release the STORE key, then a Data key (a single digit register number 0—9).

Example

Store the current front panel settings in register 2.	
LOCAL (keystrokes)	Store Settings in Register 2 STORE 2
HP-IB (program codes)	ST2 Store Settings in Register 2

Keys and Program Codes HP-IB

Keys	Program Codes HP-IB
STORE	ST

Indications No visible front panel change.

Comments Ten internal registers are available (0—9). Each is capable of storing complete front panel setups (exclusive of increment settings).

Clears any previously selected function.

Initialized conditions of the Signal Generator are stored in each of the ten internal storage registers when the instrument is powered up or reset.

Related Instructions

Display
Recall
Sequence

SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

The procedures in this section test the instrument's electrical performance using the specifications of Table 1-1 as the performance standards. All tests can be performed without access to the interior of the instrument. A simpler operational test is included in Section III under Operator's Checks.

NOTES

If the performance tests are to be considered valid, the following conditions must be met:

a. The Signal Generator must have a 30-minute warmup.

b. The line voltage must be within 90—125 Vac or 198—252 Vac; 48—66 Hz. The voltage selector card must be in the proper position. Refer to Figure 2-1.

c. The ambient temperature must be 0 to 55°C for the Level Accuracy and Flatness Test.

4-2. EQUIPMENT REQUIRED

Equipment required for the performance tests is listed in Table 1-3, Recommended Test Equipment. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model(s).

4-3. PERFORMANCE TEST RECORD

Results of the performance tests may be tabulated on Table 4-2 which is the Performance Test Record. The Performance Test Record located at the end of this section lists all of the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs or adjustments.

4-4. CALIBRATION CYCLE

This instrument requires periodic verification of performance. Depending on the use and environmental conditions, the instrument should be checked using the following performance tests at least once each year.

4-5. ABBREVIATED PERFORMANCE TESTING

In most cases, it is not necessary to perform all of the tests in this section. Table 4-1 shows which tests are recommended for various situations. The Operator's Checks in Section III should be the first step in all testing situations.

4-6. TEST PROCEDURES

It is assumed that the person performing the following tests understands how to operate the specified test equipment. Equipment settings, other than those for the Signal Generator, are stated in general terms. For example, a test might require that a spectrum analyzer's resolution bandwidth be set to 100 Hz; however, the time per division setting would not be specified and the operator would set that control so that the analyzer operates correctly.

It is also assumed that the person performing the tests will supply whatever cables, connectors, and adapters are necessary.

Table 4-1. Abbreviated Performance Tests

Testing Situations		Basic Functional Checks Section III	HP-IB Functional Checks Section III	Spectral Purity Para. 4-7	High Level Accuracy & Flatness Para. 4-8	Low Level Accuracy Para. 4-9	Modulation Para. 4-10	Output Leakage Para. 4-11
Incoming Inspection or Overall Performance Verification		x	x	x	x	x	x	x
After Complete Adjustment		x		x	x	x	x	x
After Repairs to an Individual Assembly								
Assembly	Reference Service Sheet No.							
A1	18	x						
A2	18 thru 21	x						
A3	8	x		x				
A3	9	x		x				
A3	10	x		x			FM	
A3	11	x		x			FM	
A3	12	x		x			FM	
A3	13	x		x				
A4	1	x		x				
A4	2	x		x				
A5	1	x						
A6	4	x		x	x		AM	
A6	5	x		x	x			
A6	7	x						
A7	4, 5, and 14	x						
A8	3	x		x				
A9	7	x		x	x	x		x
A10	6	x			x	x	x	
A10	7	x						
A10	12	x					FM	
A10	22	x					x	
A11	14 thru 17	x	x		x		x	
A13	17		x					
A14	14 and 22	x						
A15	22	x						
A16	22	x						
FL1	3	x		x				

4-7. SPECTRAL PURITY TESTS

SPECIFICATION:

Electrical Characteristics	Performance Limit	Conditions
SPURIOUS SIGNALS:		
Harmonics	<-30 dBc	≤+7 dBm output levels
Non-harmonics	<-60 dBc	>5 kHz from carrier in CW mode
Sub-harmonics	None	
RESIDUAL MODULATION CW MODE:		
AM (0.05 to 15 kHz Post Detection Noise Bandwidth	<-70 dBc	0.1 to 990 MHz
FM (0.3 to 3 kHz Post Detection Noise Bandwidth)	<15 Hz rms	0.1 to 123.5 MHz
	<3 Hz rms	123.5 to 247 MHz
	<6 Hz rms	247 to 494 MHz
	<15 Hz rms	494 to 990 MHz
FM (0.05 to 15 kHz Post Detection Noise Bandwidth	<30 Hz rms	0.1 to 123.5 MHz
	<8 Hz rms	123.5 to 247 MHz
	<16 Hz rms	247 to 494 MHz
	<30 Hz rms	494 to 990 MHz

DESCRIPTION: Spurious signals are checked using a spectrum analyzer. Residual AM and FM Modulation are checked using a modulation analyzer.

EQUIPMENT:

Spectrum Analyzer	HP 8558B
Modulation Analyzer	HP 8901A
Digital Multimeter	HP 3465A
AM/FM Test Source (required for modulation analyzer verification of residual AM)	HP 11715A
Cable (UG-210/U type N connectors)	HP 11500B
Cable (UG-88C/U BNC and dual banana plug connectors)	HP 11001A

PROCEDURE: *Spurious Signals*

1. Set the spectrum analyzer as follows:

Frequency Span/Div	200 kHz
Resolution Bandwidth	3 kHz
Optimum Input	+10 dBm
Reference Level	+10 dBm

4-7. SPECTRAL PURITY TESTS (Cont'd)

2. Set the Signal Generator as follows:

Frequency	100 kHz
Frequency Increment	100 kHz
Amplitude	+10 dBm
Modulation	Off

3. Connect the RF OUTPUT of the Signal Generator to the input of the spectrum analyzer as shown in Figure 4-1. Verify that all harmonics are <-30 dBc, all non-harmonics 5 kHz from the carrier are <-60 dBc, and that there are no sub-harmonics as the frequency is incremented from 100 kHz to 990 MHz.

NOTES

Adjust the Frequency Span/Div and Resolution Bandwidth controls as required.

Change the frequency increment from 100 kHz to 10 MHz at 10 MHz, if desired.

Spurious Signals	Results	
	Actual	Max.
Harmonics	______	<-30 dBc
Non-Harmonics (5 kHz from carrier)	______	<-60 dBc
Sub-Harmonics	______	None

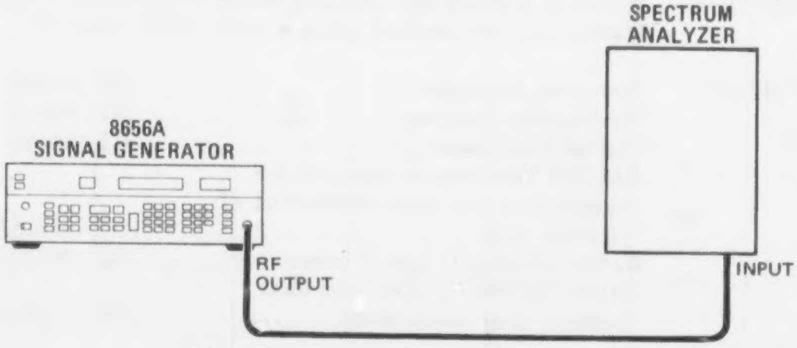


Figure 4-1. Spurious Signals Test Setup

Residual AM

NOTE

The residual AM specification of the Signal Generator is not equivalent to the published specification of the HP 8901A Modulation Analyzer. To make a valid residual AM measurement, the residual AM of the modulation analyzer should be at least 3 dB better than the specification being tested. In order to verify that the residual AM of the modulation analyzer is adequate to measure the Signal Generator's

4-7. SPECTRAL PURITY TESTS (Cont'd)

NOTE (cont'd)

residual AM specification, the residual AM of the modulation analyzer must be verified to ensure the validity of the measurement. If the Signal Generator's residual AM is measured frequently, it is not necessary to verify the residual AM of the modulation analyzer each time; however, it is recommended that it be verified monthly to ensure an accurate measurement.

4. Verify the residual AM of the modulation analyzer as follows:

   a. Connect the modulation output of the modulation analyzer to the input of the digital multimeter and the AM output of the AM/FM test source to the input of the modulation analyzer as shown in Figure 4-2. Nothing should be connected to the audio input of the AM/FM test source.

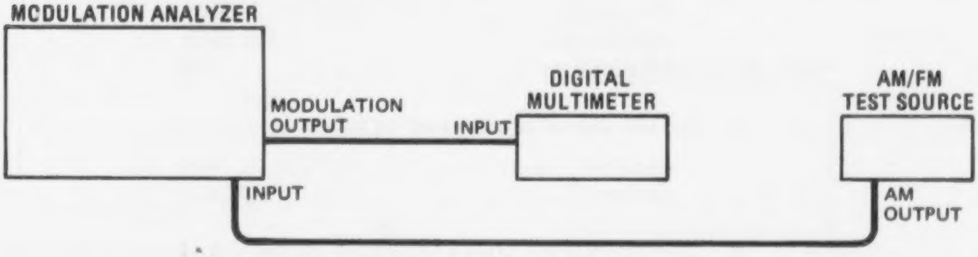


Figure 4-2. Modulation Analyzer Residual AM Verification Test Setup

   b. Set the modulation analyzer as follows:

      Measurement .... Frequency

   c. Set the AM/FM test source as follows:

      Test Mode .... FM

   d. Tune the carrier frequency on the AM/FM test source for a modulation analyzer reading of 12.5 ±0.1 MHz.

   e. Set the digital multimeter as follows:

      Function .... Vac
      Range .... 200 mV

   f. Set the modulation analyzer as follows:

      Measurement .... AM
      HP Filter .... 50 Hz
      LP Filter .... 15 kHz

   g. The digital multimeter should indicate 2.2 mV or less.

4-7. SPECTRAL PURITY TESTS (Cont'd)

NOTE

To make a valid residual AM measurement, the residual AM of the modulation analyzer should be at least 3 dB better than the specification being tested or <-73 dBc (0.022%). With an output sensitivity of 10%/V, the corresponding output level is 2.2 mV.

5. Set the modulation analyzer as follows:

   Measurement .... AM
   Detector .... Peak+
   HP Filter .... 50 Hz
   LP Filter .... 15 kHz
   FM De-Emphasis .... Off

6. Set the Signal Generator as follows:

   Frequency .... Any
   Amplitude .... 0.0 dBm
   Modulation .... Off

7. Set the digital multimeter as follows:

   Function .... Vac
   Range .... 200 mV

8. Connect the RF OUTPUT of the Signal Generator to the input of the modulation analyzer and the output of the modulation analyzer to the input of the digital multimeter as shown in Figure 4-3.

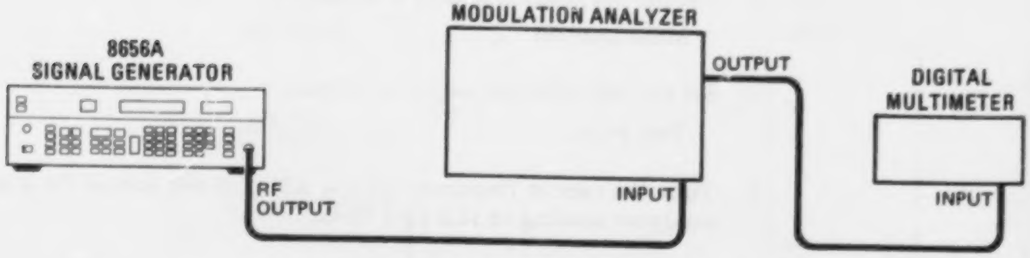


Figure 4-3. Residual AM Test Setup

9. The digital multimeter should indicate <3.16 mVrms.

Actual	Max.
______	<3.16 mVrms

4-7. SPECTRAL PURITY TESTS (Cont'd)

Residual FM

10. Set the modulation analyzer as follows:

    Measurement .... FM
    Detector ....AVG
    FM De-Emphasis .... Off
    Automatic Operation ....Selected

11. Set the Signal Generator as follows:

    Frequency .... Any
    Amplitude ....0.0 dBm
    Modulation .... Off

12. Connect the RF OUTPUT of the Signal Generator to the input of the modulation analyzer as shown in Figure 4-4.

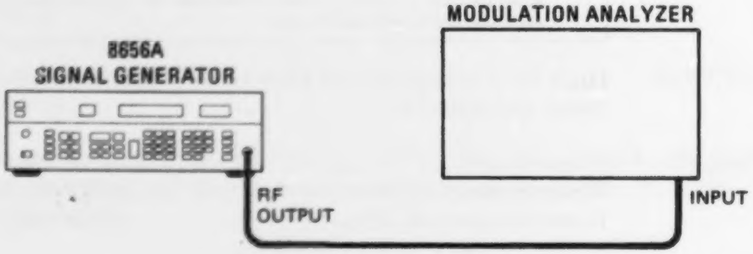


Figure 4-4. Residual FM Test Setup

13. Set the Signal Generator frequency and select the modulation analyzer high-pass and low-pass filters as indicated in the following table. Verify that the measured results do not exceed the limits specified.

Signal Generator Frequency	Modulation Analyzer Filter		Results (Hz rms)	
	High-Pass (Hz)	Low-Pass (kHz)	Actual	Max.
0.1 to 123.5 MHz	300	3	______	<15
123.5 to 247 MHz	300	3	______	<3
247 to 494 MHz	300	3	______	<6
494 to 990 MHz	300	3	______	<15
0.1 to 123.5 MHz	50	15	______	<30
123.5 to 247 MHz	50	15	______	<8
247 to 494 MHz	50	15	______	<16
494 to 990 MHz	50	15	______	<30

4-8. HIGH LEVEL ACCURACY AND FLATNESS TESTS

SPECIFICATION:

Electrical Characteristics	Performance Limit	Conditions
OUTPUT:		
Level Range	+13 dBm to −127 dBm	Into 50 ohms
Resolution	0.1 dB	
Absolute Level Accuracy[1]	≤±1.5 dB	Output levels of +13 dBm to −127 dBm; frequencies from 100 kHz to 990 MHz
Level Flatness	≤±1.0 dB	Output level setting of 0.0 dBm; frequencies from 100 kHz to 990 MHz

[1] Absolute level accuracy includes allowances for detector linearity, temperature, flatness, attenuator accuracy, and measurement error.

DESCRIPTION: High level accuracy (+13 dBm to −67 dBm) and flatness are verified using a power meter and sensors.

EQUIPMENT:

Power Meter	HP 436A
Power Sensor (−25 dBm)	HP 8482A
Power Sensor (−60 dBm)	HP 8484A

PROCEDURE: *Level Flatness*

1. Connect the −25 dBm power sensor to the power meter. Zero and adjust the power sensor to the power meter.
2. Connect the power sensor to the Signal Generator as shown in Figure 4-5.

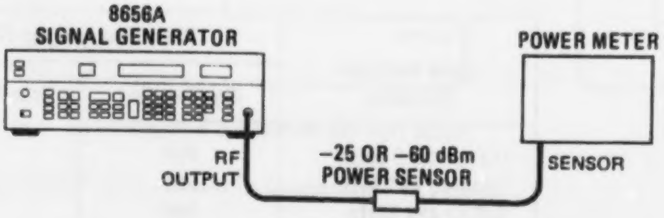


Figure 4-5. High Level Accuracy and Flatness Test Setup

3. Set the Signal Generator as follows:

Frequency	100 kHz
Frequency Increment	100 kHz
Amplitude	0.0 dBm
Modulation	Off

4-8. HIGH LEVEL ACCURACY AND FLATNESS TESTS (Cont'd)

4. Set power meter mode to dB (Ref).

5. Step the Signal Generator through the frequency range of 100 kHz to 990 MHz (use 10 MHz steps above 10 MHz) and record the highest and lowest readings.

________ Highest reading ________ Frequency
________ Lowest reading ________ Frequency

The amplitude variation should not exceed 2.0 dB. Record the maximum variation (highest reading — lowest reading).

________ ≤±1.0 dB

Absolute Level Accuracy

6. Set the Signal Generator as follows:

Frequency .... 10 MHz
Amplitude .... +13 dBm
Amplitude Increment.............. 5 dBm
Modulation .... Off

7. Power meter reading must be +13 ±1.5 dBm. Step the amplitude down to -22 dBm. At each step, the power meter reading must be within ±1.5 dBm of the selected amplitude.

________ +13 ±1.5 dBm
________ +8 ±1.5 dBm
________ +3 ±1.5 dBm
________ -2 ±1.5 dBm
________ -7 ±1.5 dBm
________ -12 ±1.5 dBm
________ -17 ±1.5 dBm
________ -22 ±1.5 dBm

8. Replace the -25 dBm power sensor with the -60 dBm power sensor.

NOTE

Let the system warm up, then zero the power meter and adjust the power meter to the power sensor.

9. Connect the -60 dBm power sensor to the RF OUTPUT of the Signal Generator as shown in Figure 4-5.

4-8. HIGH LEVEL ACCURACY AND FLATNESS TESTS (Cont'd)

10. **Step the amplitude down to –67 dBm. At each step, the power meter reading must be within ±1.5 dB of the selected amplitude.**

__________ –27 ±1.5 dBm
__________ –32 ±1.5 dBm
__________ –37 ±1.5 dBm
__________ –42 ±1.5 dBm
__________ –47 ±1.5 dBm
__________ –52 ±1.5 dBm
__________ –57 ±1.5 dBm
__________ –62 ±1.5 dBm
__________ –67 ±1.5 dBm

11. **Repeat steps 7 through 10 for frequencies greater than 10 MHz.**

4-9. LOW LEVEL ACCURACY TESTS

SPECIFICATION:

Electrical Characteristics	Performance Limit	Conditions
OUTPUT:		
Level Range	+13 dBm to −127 dBm	Into 50 ohms
Resolution	0.1 dB	
Absolute Level Accuracy[1]	≤±1.5 dB	Output levels of +13 dBm to −127 dBm; frequencies from 100 kHz to 990 MHz

[1] Absolute level accuracy includes allowances for detector linearity, temperature, flatness, attenuator accuracy, and measurement error.

DESCRIPTION: Low level accuracy (below −67 dBm) is verified by inserting a calibrated attenuator (pad) in series with the Signal Generator output to establish a reference on a spectrum analyzer. The attenuator is then removed and the Signal Generator level is set 60 dBm lower. The Signal Generator output is then compared to the reference level on the spectrum analyzer and the actual level is calculated.

EQUIPMENT:

Power Meter	HP 436A
Power Sensor (−25 dBm)	HP 8482A
Power Sensor (−60 dBm)	HP 8484A
Spectrum Analyzer	HP 8568A
Wideband Amplifier (26 dB)	HP 8477D Option 010
Fixed 60 dB Attenuator	HP 8491A Option H56
Cables (UG-210/U type N connectors)	HP 11500B

PROCEDURE:

1. Set the Signal Generator RESET/STBY/ON switch to STBY to zero the power meter.

2. Connect the power sensor to the power meter and to the RF OUTPUT of the Signal Generator as shown in Figure 4-6. Zero the power meter and adjust the power sensor to the power meter.

NOTE

Use the −25 dBm sensor if the level being measured is greater than −20 dBm. For lower levels, use the −60 dBm sensor.

3. Set the Signal Generator as follows:

Frequency	10 MHz
Amplitude	0.0 dBm
Modulation	Off
RESET/STBY/ON	ON

4-9. LOW LEVEL ACCURACY TESTS (Cont'd)

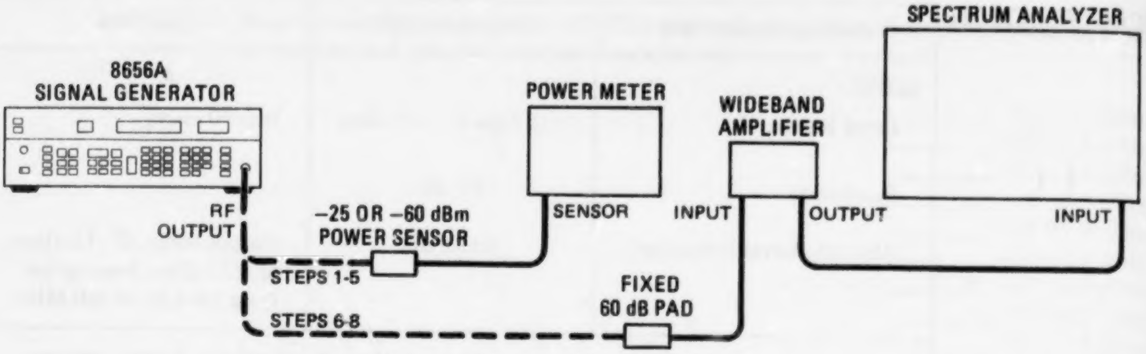

SPECTRUM ANALYZER
8656A
SIGNAL GENERATOR
POWER METER
WIDEBAND
AMPLIFIER
RF
OUTPUT
-25 OR -60 dBm
POWER SENSOR
SENSOR
INPUT
OUTPUT
INPUT
STEPS 1-5
STEPS 6-8
FIXED
60 dB PAD

Figure 4-6. Low Level Accuracy Test Setup

4. Set the spectrum analyzer as follows:

Center Frequency	10 MHz
Reference Level	-60 dBm
Frequency Span/Div	1 MHz
Resolution Bandwidth	100 kHz
Video Average	25 times

5. Set the Signal Generator amplitude to 60 dBm above the power level being verified. For example, if it is desired to verify a power level of -80 dBm, set the amplitude to -20 dBm. Measure the output with the power meter and record the reading.

________ dBm

6. Connect the 60 dB pad to the RF OUTPUT of the Signal Generator and connect the signal through the wideband amplifier as shown in Figure 4-6. View the signal on the spectrum analyzer and set the reference level of the spectrum analyzer one division above the signal in the 2 dB log amplitude mode. Use well shielded RF cables or leakage will affect the accuracy of the results.

7. Decrease the Signal Generator amplitude by 60 dBm and remove the pad. View the signal on the spectrum analyzer and determine the difference from the signal viewed in step 5. The actual output level is calculated as follows:

________ power meter reading in step 5.
− ________ exact value of pad.
+ ________ difference observed in step 7.
= ________ actual output level

8. Repeat steps 5 through 7 for output amplitudes to -127 dBm.

9. Repeat steps 1 through 8 for frequencies of 100 MHz, 201 MHz, 801 MHz, 901 MHz, and 990 MHz. These are the frequencies for which the pad is calibrated.

4-10. MODULATION TESTS

SPECIFICATION:

Electrical Characteristics	Performance Limit	Conditions
AMPLITUDE MODULATION:		
Depth[1]	0 to 99%	Output levels of +7 dBm and below; frequencies from 100 kHz to 990 MHz.
	0 to 30%	Output levels of +10 dBm and below; frequencies from 100 kHz to 990 MHz.
Resolution	1%	
Incidental Phase Modulation	<0.3 radian peak	30% AM depth and internal rates
Indicator Accuracy[1]	±2%, (±4% of reading)	Depths 90% and internal rates
AM Rates:		
Internal	400 and 1 kHz, ±3%	
External	25 Hz to 25 kHz	1 dB bandwidth, ac coupled
AM Distortion (internal rates)	<1.5%	0 to 30% AM
	<3%	31 to 70% AM
	<5%	71 to 90% AM
FREQUENCY MODULATION		
Maximum Peak Deviation (Δfpk)[2]:		
Rates ≥60 Hz	99 kHz	0.1 to 123.5 MHz (fc)
	25 kHz	123.5 to 247 MHz (fc)
	50 kHz	247 to 494 MHz (fc)
	99 kHz	494 to 990 MHz (fc)
Rates <60 Hz	1600 x Rate	0.1 to 123.5 MHz (fc)
	400 x Rate	123.5 to 247 MHz (fc)
	800 x Rate	247 to 494 MHz (fc)
	1600 x Rate	494 to 990 MHz (fc)
		(FM not specified for fc — Δfpk <100 kHz)
Resolution	0.1 kHz	Deviations <10 kHz
	1 kHz	Deviations ≥10 kHz

[1] AM depth is further limited by the Indicator Accuracy specification.

[2] FM deviation is further limited by the Indicator Accuracy specification.

4-10. MODULATION TESTS (Cont'd)

SPECIFICATION:
(Cont'd)

Electrical Characteristics	Performance Limit	Conditions
FREQUENCY MODULATION (Cont'd):		
Incidental AM	<0.1%	<20 kHz peak deviation, internal rates and carrier frequency ≥500 kHz.
Indicator Accuracy[2]	±5% of reading	At internal rates. Add ±5% if 250 Hz frequency increments are used.
FM Distortion (Total Harmonic Distortion)	<0.5%	100 Hz to 99 kHz peak deviations and internal rates.
FM Rates:		
Internal	400 Hz and 1 kHz, ±3%	
External	25 Hz to 25 kHz	1 dB bandwidth, ac coupled

[2] FM deviation is further limited by the Indicator Accuracy specification.

DESCRIPTION: All modulation specifications are verified by measuring the specified parameters on a modulation analyzer. Distortion is verified by measuring the demodulated output from the modulation analyzer on a distortion analyzer.

EQUIPMENT:

Modulation Analyzer	HP 8901A
Distortion Analyzer	HP 339A
AM/FM Test Source (required for modulation analyzer verification of incidental AM)	HP 11715A
Test Oscillator	HP 651B
Cable (UG-210/U type N connectors)	HP 11500B
Cable (UG-88C/U BNC and dual banana plug connectors)	HP 11001A

PROCEDURE: *AM Indicator Accuracy*

1. Connect the RF OUTPUT of the Signal Generator to the input of the modulation analyzer as shown in Figure 4-7.
2. Connect the modulation output of the modulation analyzer to the input of the distortion analyzer as shown in Figure 4-7.

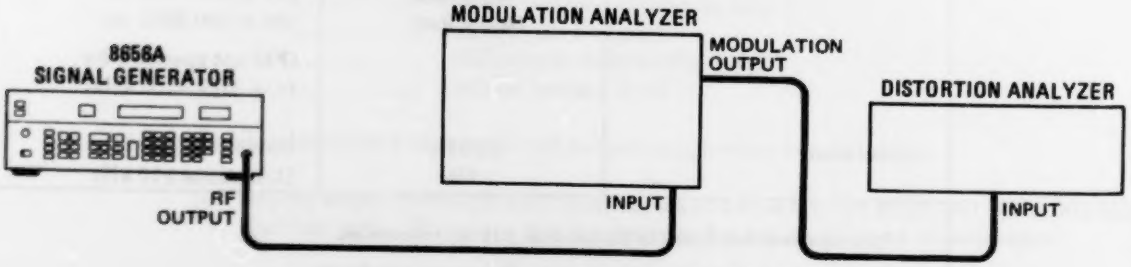


Figure 4-7. Modulation Test Setup

4-10. MODULATION TESTS (Cont'd)

3. Set the modulation analyzer as follows:

Measurement	AM
Detector	Peak+
HP Filter	300 Hz
LP Filter	15 kHz
FM De-Emphasis	Off
Automatic Operation	Selected

4. Set the Signal Generator as follows:

Frequency	100 MHz
Amplitude	+7 dBm
Modulation	1 kHz (Int.) AM 50%

5. Set the AM depth to the values listed in the following table and verify that the measured results are within the limits specified.

AM Depth for 100 MHz	Results		
	Min.	Actual	Max.
10%	7.6%	________	12.4%
30%	26.8%	________	33.2%
70%	65.2%	________	74.8%
90%	84.4%	________	95.6%

6. Repeat step 5 with the Signal Generator set to frequencies of 240 MHz, 400 MHz, and 990 MHz.

AM Depth for 240 MHz	Results		
	Min.	Actual	Max.
10%	7.6%	________	12.4%
30%	26.8%	________	33.2%
70%	65.2%	________	74.8%
90%	84.4%	________	95.6%

AM Depth for 400 MHz	Results		
	Min.	Actual	Max.
10%	7.6%	________	12.4%
30%	26.8%	________	33.2%
70%	65.2%	________	74.8%
90%	84.4%	________	95.6%

4-10. MODULATION TESTS (Cont'd)

AM Depth for 990 MHz	Results		
	Min.	Actual	Max.
10%	7.6%	______	12.4%
30%	26.8%	______	33.2%
70%	65.2%	______	74.8%
90%	84.4%	______	95.6%

7. Select the modulation analyzer's 50 Hz HP filter. Verify the AM accuracy with the Signal Generator frequency at 100 MHz and internal 400 Hz AM modulation.

AM Depth for 100 MHz	Results		
	Min.	Actual	Max.
10%	7.6%	______	12.4%
30%	26.8%	______	33.2%
70%	65.2%	______	74.8%
90%	84.4%	______	95.6%

Incidental Phase Modulation

8. Set the modulation analyzer as follows:

Measurement	Phase Modulation
HP Filter	300 Hz
LP Filter	15 kHz
Detector	Peak+

9. Set the Signal Generator as follows:

Frequency	100 kHz
Frequency Increment	100 kHz
Amplitude	+7 dBm
Modulation	1 kHz (Int.) AM 30%

10. Step the Signal Generator through the frequency range of 100 kHz to 990 MHz (use 10 MHz steps above 10 MHz) and record the highest reading. The highest reading should not exceed the limit specified.

Signal Generator Frequency		Result	
Min.	Max.	Actual	Max.
100 kHz	990 MHz	______	<0.3 radian peak

4-10. MODULATION TESTS (Cont'd)

AM Distortion

11. Set the modulation analyzer as follows:

Measurement	AM
HP Filter	300 Hz
LP Filter	15 kHz
Detector	Peak+

12. Set the distortion analzyer as follows:

Function	Distortion
Analyzer Input Select	Distortion
Frequency	1 kHz

13. Set the Signal Generator as follows:

Frequency	10 MHz
Amplitude	+7 dBm
Modulation	1 kHz (Int.) AM 50%

14. **Set the AM depth to the values listed in the following table and verify that the measured results do not exceed the limits specified.**

AM Depth for 100 MHz	Results	
	Actual	Max.
30%	______	<1.5%
70%	______	<3.0%
90%	______	<5.0%

15. **Repeat step 13 with the Signal Generator set to frequencies of 240 MHz, 400 MHz, and 990 MHz.**

AM Depth for 240 MHz	Results	
	Actual	Max.
30%	______	<1.5%
70%	______	<3.0%
90%	______	<5.0%

AM Depth for 400 MHz	Results	
	Actual	Max.
30%	______	<1.5%
70%	______	<3.0%
90%	______	<5.0%

AM Depth for 990 MHz	Results	
	Actual	Max.
30%	______	<1.5%
70%	______	<3.0%
90%	______	<5.0%

4-10. MODULATION TESTS (Cont'd)

FM Indicator Accuracy

16. Set the modulation analyzer as follows:

Measurement .... FM
Detector .... Peak+
HP Filter .... 300 Hz
LP Filter .... 3 kHz

17. Set the Signal Generator as follows:

Frequency .... 100 MHz
Amplitude .... +7 dBm
Modulation .... 1 kHz (Int.) FM 5 kHz

18. Set the FM deviation to the values listed in the following table and verify that the measured results are within the limits specified.

FM Deviation for 100 MHz	Results		
	Min.	Actual	Max.
5.0 kHz	4.75 kHz	______	5.25 kHz
30.0 kHz	28.50 kHz	______	31.50 kHz
70.0 kHz	66.50 kHz	______	73.50 kHz
99.0 kHz	94.05 kHz	______	103.95 kHz

Incidental AM

NOTE

The incidental AM specification of the Signal Generator is not equivalent to the published specification of the HP 8901A Modulation Analyzer. To make a valid incidental AM measurement, the incidental AM of the modulation analyzer must be four times better than the specification being tested. In order to verify that the incidental AM of the modulation analyzer is adequate to measure the Signal Generator's incidental AM specification, the incidental AM of the modulation analyzer must be verified to ensure the validity of the measurement. If the Signal Generator's incidental AM is measured frequently, it is not necessary to verify the incidental AM of the modulation analyzer each time; however, it is recommended that it be verified monthly to ensure an accurate measurement.

19. Verify the incidental AM of the modulation analyzer as follows:

a. Connect the FM ÷4 output of the AM/FM test source to the input of the modulation analyzer and the 50Ω output of the test oscillator to the audio input of the AM/FM test source, as shown in Figure 4-8.

b. Set the modulation analyzer as follows:

Measurement .... Frequency

4-10. MODULATION TESTS (Cont'd)

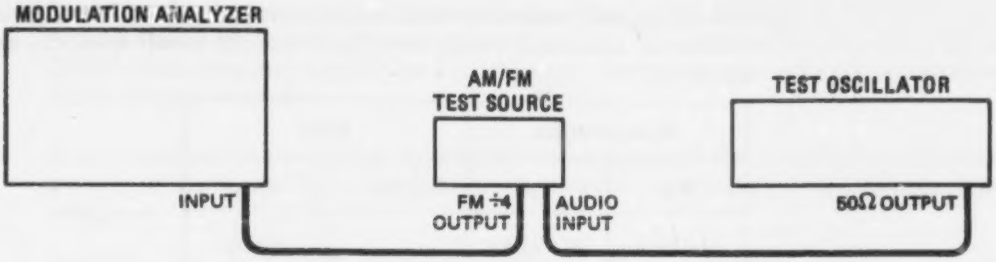


Figure 4-8. Modulation Analyzer Incidental AM Verification Test Setup

c. Set the AM/FM test source as follows:

Test Mode .... FM

d. Tune the carrier frequency on the AM/FM test source for a modulation analyzer reading of 100 ±0.1 MHz.

e. Set the test oscillator as follows:

Frequency .... 1 kHz
Output Attenuator .... −10 dBm
Amplitude Course .... Fully ccw

f. Set the modulation analyzer as follows:

Measurement .... FM
Detector .... Peak+
HP Filter .... 300 Hz
LP Filter .... 3 kHz

g. Increase the output of the test oscillator by rotating the Amplitude Coarse control clockwise until the modulation analyzer indicates 20.0 ±0.1 kHz peak deviation.

h. Set the modulation analyzer as follows:

Measurement .... AM

i. The modulation must be <0.02% AM to test the incidental AM of the Signal Generator.

20. Set the modulation analyzer as follows:

Measurement .... AM
Detector .... Peak+
HP Filter .... 300 Hz
LP Filter .... 3 kHz

21. Set the Signal Generator as follows:

Amplitude .... +7 dBm
Modulation .... 1 kHz (Int.) FM 20 kHz

22. Connect the equipment as shown in Figure 4-7, Modulation Test Setup.

4-10. MODULATION TESTS (Cont'd)

23. Set the Signal Generator frequency to a value within the range specified in the following table and verify that the measured result does not exceed the limit specified.

Signal Generator		Result	
Min.	Max.	Actual	Max.
500 kHz	990 MHz	________	<0.1%

FM Distortion

24. Set the modulation analyzer as follows:

Measurement .... FM
Detector .... Peak+
HP Filter .... 300 Hz
LP Filter .... 3 kHz

25. Set the distortion analyzer as follows:

Function .... Distortion
Analyzer Input Select .... Distortion
Frequency .... 1 kHz

26. Set the Signal Generator as follows:

Frequency .... 100.0 MHz
Amplitude .... +7 dBm
Modulation .... 1 kHz (Int.) FM

27. Connect the equipment as shown in Figure 4-7, Modulation Test Setup.

28. Verify that the measured Total Harmonic Distortion does not exceed 0.5%.

29. Set the Signal Generator FM deviation to a value within the range specified in the following table and verify that the measured result does not exceed the limit specified.

FM Deviation		Result	
Min.	Max.	Actual	Max.
100 Hz	99 kHz	________	<0.5%

NOTE

At peak deviations less than 3 kHz, residual FM and other types of FM distortion become a greater portion of the distortion reading. If the distortion falls within tolerance at or above 3 kHz, it may be safely assumed that the Signal Generator meets the test requirements.

4-11. OUTPUT LEAKAGE TESTS

SPECIFICATION: **Leakage:** Leakage limits are within those specified in MIL STD 461A, VDE 0871, and CISPR Publication 11. Furthermore, less than 1.0 μV is induced in a two-turn, 2.5 cm (1-inch) diameter loop held 2.5 cm (1 inch) away from the front surface and measured into a 50-ohm receiver.

DESCRIPTION Output leakage is verified by holding a loop antenna 2.5 cm (1 inch) from the front surface of the Signal Generator and measuring the resulting signal with a spectrum analyzer.

The loop antenna is suspended in a molding so that when the molding is in contact with a surface, the loop antenna is one inch from the surface.

NOTE

The use of a screen room may be necessary to reduce external radiated interference.

EQUIPMENT

One-Inch Loop Antenna	HP 08640-60501
26 dB Amplifier	HP 8447D
Spectrum Analyzer	HP 8558A
50-ohm Termination (3 required)	HP 11593A

PROCEDURE:

1. Connect equipment as shown in Figure 4-9.

NOTE

To avoid disturbing the antenna's field and causing measurement error, grasp the antenna at the end that has the BNC connector.

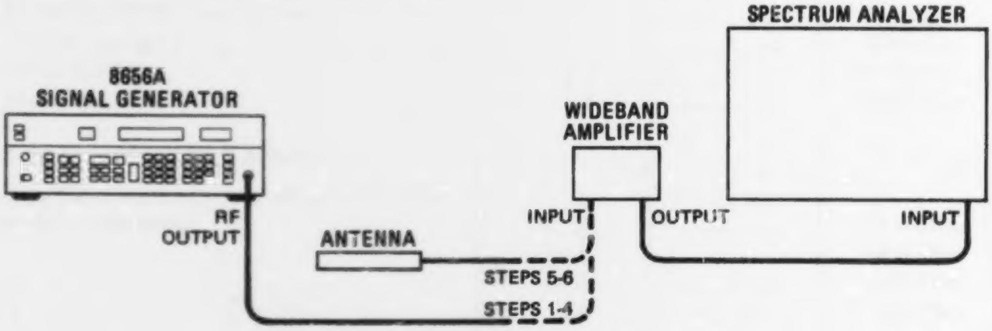


Figure 4-9. Output Leakage Test Setup

2. Set the Signal Generator as follows:

Frequency	100 MHz
Amplitude	−107 dBm
Modulation	Off
RESET/STBY/ON	ON

4-11. OUTPUT LEAKAGE TESTS (Cont'd)

3. Set the spectrum analyzer as follows:

Center Frequency	100 MHz
Input Attenuation	-40 dB
Reference Level	-20 dBm
Frequency Span/Div	20 MHz
Resolution Bandwidth	10 kHz

4. View the signal on the spectrum analyzer and adjust the reference level controls of the spectrum analyzer to set the -107 dBm signal from the Signal Generator to a reference graticule line on the spectrum analyzer display. Set the video filter to further separate the signal from the noise. Disconnect the Signal Generator from the spectrum analyzer and connect 50-ohm terminations to the Signal Generator RF OUTPUT connector.

5. Connect the one-inch loop antenna to the analyzer through the 26 dB amplifier as shown in Figure 4-9. Hold the end of the loop antenna cylinder in contact with the front surfaces of the Signal Generator. All signals and noise should be below the reference graticule line (i.e., below -107 dBm).

__________ <-107 dBm (<1.0 μV) at 100 MHz

6. Repeat step 5 for frequencies of 300, 500, 700, 900, and 990 MHz.

__________ <-107 dBm (<1.0 μV) at 300 MHz
__________ <-107 dBm (<1.0 μV) at 500 MHz
__________ <-107 dBm (<1.0 μV) at 700 MHz
__________ <-107 dBm (<1.0 μV) at 900 MHz
__________ <-107 dBm (<1.0 μV) at 990 MHz

Table 4-2. Performance Test Record (1 of 4)

Hewlett-Packard Company
Model 8656A
Signal Generator
Serial Number ______________________

Tested by ______________________

Date ______________________

Para. No.	Test	Results		
		Min.	**Actual**	**Max.**
4-7.	**SPURIOUS SIGNALS:**			
	Harmonics		________	-30 dBc
	Non-Harmonics (>5 kHz from carrier)		________	-60 dBc
	Sub-Harmonics		________	None
	RESIDUAL MODULATION CW MODE:			
	AM (0.05 to 15 kHz Post Detection Noise Bandwidth)			
	0.1 to 990 MHz		________	3.16 mVrms (-70 dBc)
	FM (0.3 to 3 kHz Post Detection Noise Bandwidth)			
	0.1 to 123.5 MHz		________	15 Hz rms
	123.5 to 247 MHz		________	3 Hz rms
	247 to 494 MHz		________	6 Hz rms
	494 to 990 MHz		________	15 Hz rms
	FM (0.05 to 15 kHz Post Detection Noise Bandwidth)			
	0.1 to 123.5 MHz		________	30 Hz rms
	123.5 to 247 MHz		________	8 Hz rms
	247 to 494 MHz		________	16 Hz rms
	494 to 990 MHz		________	30 Hz rms
4-8.	**HIGH LEVEL ACCURACY AND FLATNESS**			
	Absolute Level Accuracy (+13 dBm to -67 dBm; 100 kHz to 990 MHz)	+11.5	________	+14.5 dBm
		+6.5	________	+9.5 dBm
		+1.5	________	+4.5 dBm
		-3.5	________	-0.5 dBm
		-8.5	________	-5.5 dBm
		-13.5	________	-10.5 dBm
		-18.5	________	-15.5 dBm
		-23.5	________	-20.5 dBm
		-28.5	________	-25.5 dBm
		-33.5	________	-30.5 dBm
		-38.5	________	-35.5 dBm
		-43.5	________	-40.5 dBm
		-48.5	________	-45.5 dBm
		-53.5	________	-50.5 dBm

Table 4-2. Performance Test Record (2 of 4)

Para. No.	Test	Results		
		Min.	Actual	Max.
4-8.	**HIGH LEVEL ACCURACY AND FLATNESS:**			
Cont'd	Absolute Level Accuracy (+13 to −67 dBm; 100 kHz to 990 MHz)	−58.5	______	−55.5 dBm
		−63.5	______	−60.5 dBm
		−68.5	______	−65.5 dBm
	Level Flatness (0.0 dBm)	−1.0	______	+1.0 dB
4-9.	**LOW LEVEL ACCURACY**			
	Absolute Level Accuracy (−67 dBm to −127 dBm; 100 kHz to 990 MHz)			
	−67 dBm to −127 dBm 10 MHz	−1.5	______	+1.5 dB
	100 MHz	−1.5	______	+1.5 dB
	201 MHz	−1.5	______	+1.5 dB
	801 MHz	−1.5	______	+1.5 dB
	901 MHz	−1.5	______	+1.5 dB
4-10.	**AMPLITUDE MODULATION**			
	Indicator Accuracy			
	(Internal 1 kHz source)			
	100 MHz 10%	7.6	______	12.4%
	30%	26.8	______	33.2%
	70%	65.2	______	74.8%
	90%	84.4	______	95.6%
	240 MHz 10%	7.6	______	12.4%
	30%	26.8	______	33.2%
	70%	65.2	______	74.8%
	90%	84.4	______	95.6%
	400 MHz 10%	7.6	______	12.4%
	30%	26.8	______	33.2%
	70%	65.2	______	74.8%
	90%	84.4	______	95.6%
	990 MHz 10%	7.6	______	12.4%
	30%	26.8	______	33.2%
	70%	65.2	______	74.8%
	90%	84.4	______	95.6%
	(Internal 400 Hz source)			
	100 MHz 10%	7.6	______	12.4%
	30%	26.8	______	33.2%
	70%	65.2	______	74.8%
	90%	84.4	______	95.6%
	Incidental Phase Modulation (30% AM Internal Rates) 100 kHz to 990 MHz		______	0.3 radian peak

Table 4-2. Performance Test Record (3 of 4)

Para. No.	Test	Results		
		Min.	Actual	Max.
4-10. Cont'd)	**AMPLITUDE MODULATION:**			
	AM Distortion			
	(Internal 1 kHz Source)			
	100 MHz 30%		______	1.5%
	70%		______	3.0%
	90%		______	5.0%
	240 MHz 30%		______	1.5%
	70%		______	3.0%
	90%		______	5.0%
	400 MHz 30%		______	1.5%
	70%		______	3.0%
	90%		______	5.0%
	990 MHz 30%		______	1.5%
	70%		______	3.0%
	90%		______	5.0%
	FREQUENCY MODULATION			
	Indicator, Accuracy			
	(Internal 1 kHz Source)			
	100 MHz 5.0 kHz	4.75 kHz	______	5.25 kHz
	30.0 kHz	28.50 kHz	______	31.50 kHz
	70.0 kHz	66.50 kHz	______	73.50 kHz
	99.0 kHz	94.05 kHz	______	103.95 kHz
	Incidental AM			
	(<20 kHz Peak Deviation, Internal Rates and Carrier Frequency 500 kHz to 990 MHz).		______	0.1%
	FM Distortion			
	(Internal 1 kHz Source)			
	100 Hz to 99 kHz Deviation		______	0.5%

Table 4-2. Performance Test Record (4 of 4)

Para. No.	Test	Results		
		Min.	Actual	Max.
4-11.	**OUTPUT LEAKAGE** Leakage (Two-turn 2.5 cm diameter loop held 2.5 cm away from front surface)		______	−107 dBm (1.0 μV) at 100 mHz
			______	−107 dBm (1.0 μV) at 300 mHz
			______	−107 dBm (1.0 μV) at 500 mHz
			______	−107 dBm (1.0 μV) at 700 mHz
			______	−107 dBm (1.0 μV) at 900 mHz
			______	−107 dBm (1.0 μV) at 990 mHz

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

This section contains adjustments and checks that assure peak performance of the Signal Generator. The instrument should be readjusted after repair or failure to pass a performance test. Allow a 30-minute warm-up prior to performing the adjustments. Removal of the instrument top and bottom covers is required for most adjustments. Included in this section are test setups and illustrations that show the location of each assembly. Removal and disassembly procedures are given in Section VIII. To determine which performance tests and adjustments to perform after a repair, refer to paragraph 5-5, Post-Repair Adjustments.

5-2. SAFETY CONSIDERATIONS

Refer to the Safety Considerations page found at the beginning of this manual for a summary of the safety information.

5-3. EQUIPMENT REQUIRED

Most adjustment procedures contain a list of required test equipment. The test equipment is also identified by callouts in the test setup diagrams, where included. If substitutions must be made for the specified test equipment, refer to the Recommended Test Equipment table in Section I of this manual for the minimum specifications. It is important that the test equipment meet the critical specifications listed in the table if the Signal Generator is to meet its performance requirements.

5-4. FACTORY-SELECTED COMPONENTS

Factory-selected components are identified on the schematics and parts lists by an asterisk (*) which follows the reference designator. The nominal value or range of the components is shown. Manual change sheets will provide updated information pertaining to selected components. Table 5-1 lists

Table 5-1. Factory Selected Components

Reference Designator	Service Sheet	Range of Values	Basis of Selection
A4R6,10	1	110Ω to 287Ω	Attenuator pad selected for − 8 dBm input to mixer A4U1.
A4R7	1	17.8Ω to 61.9Ω	Measure power level at RF Test Point A4TP3 with A4R6 and A4R7 disconnected. Select pad values for −8 dBm to mixer. Level must be checked whenever the A3, A4, A8, or FL1 assemblies are replaced. **R6, 10 R7 Attenuation (db)** 110 61.9 9 121 51.1 8 133 46.4 7 147 38.3 6 178 31.6 5 215 23.7 4 287 17.8 3
A4C22	1	0 or 1 pF	Removed to eliminate spurs at 690 to 740 MHz.
A6R4	4	75Ω to 147Ω	Selected to bias U1 so noise and harmonics are as low as possible in both the divide-by-2 and divide-by-4 bands. Refer to Specifications and Supplemental Characteristics tables in Section I.

FACTORY-SELECTED COMPONENTS (Cont'd)

the reference designator, the basis used for selecting a particular value, the nominal value range, and the service sheet where the component part is shown.

5-5. POST-REPAIR ADJUSTMENTS

Table 5-2 lists the adjustments related to repairs or replacement of any of the assemblies.

5-6. RELATED ADJUSTMENTS

The procedures in this section can be done in any order; however, it is suggested that the power supply voltage, reference voltage, and audio oscillator adjustments be performed first. Changes in these adjustments can affect other adjustments, especially level and modulation accuracies.

WARNING

Maintenance described herein is performed with power supplied to the instrument, and protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed.

Table 5-2. Post-Repair Adjustments

Assembly Repaired or Replaced	Reference Service Sheet No.	Related Adjustments (Paragraph)
A1	18	None
A2	18 thru 21	None
A3	8	5-16
A3	9	None
A3	10	5-23
A3	11	None
A3	12	5-22
A3	13	5-14, 5-15
A4	1	5-12
A4	2	5-11, 5-13
A5	1	None
A6	4 and 6	5-19, 5-21
A6	5	5-20
A7	14 thru 17	None
A8	1 and 3	5-17, 5-18
A9	7	5-24
A10	6	5-8, 5-9, 5-10, 5-19 and 5-21
A10	12	5-12
A10	22	5-7
A11 thru A15	13 thru 17, and 22	None
A16	22	5-25

5-7. POWER SUPPLY VOLTAGE ADJUSTMENT

REFERENCE: Service Sheets 8 and 22.

DESCRIPTION: The +5.4 Vdc power supply is adjusted for +5.25 Vdc ±0.02 Vdc at Test Point A3TP10 using a digital multimeter.

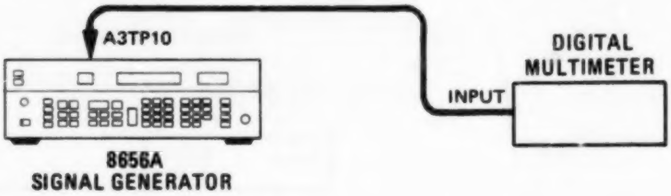


Figure 5-1. +5.4 Vdc Power Supply Adjustment Setup

EQUIPMENT: Digital Multimeter .... HP 3465A

PROCEDURE:

1. Set the digital multimeter as follows:

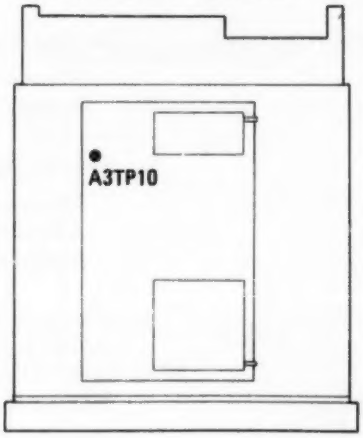
Function	Vdc
Range	20V

2. Set the Signal Generator as follows:

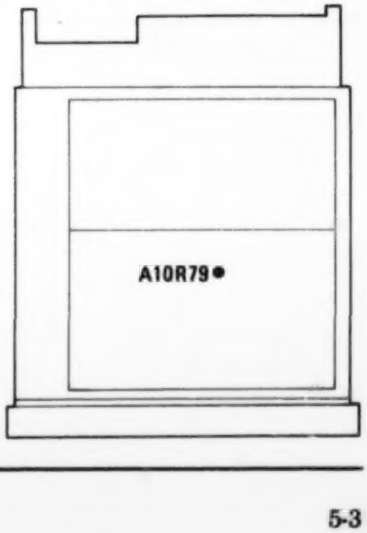
Frequency	140 MHz
Amplitude	−10 dBm
Modulation	AM 50%

3. Connect the digital multimeter to Test Point A3TP10 (+5V). Adjust A10R79 (+5.4V ADJ) for a reading of +5.25 Vdc ±0.02 Vdc on the digital multimeter.

Top Internal View, Level 1



Bottom Internal View, Level 4



5-8. REFERENCE VOLTAGE ADJUSTMENT

REFERENCE: Service Sheet 6.

DESCRIPTION: The +2 Vdc reference is adjusted for +2.000 Vdc ±0.004 Vdc at Test Point A10J6 pin 4 using a digital multimeter.

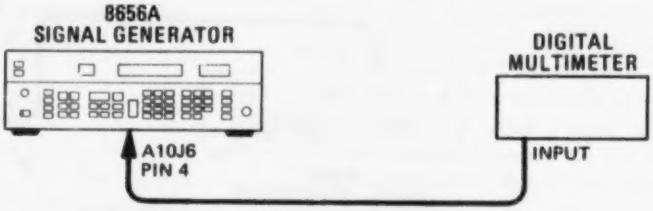

8656A
SIGNAL GENERATOR
DIGITAL
MULTIMETER
A10J6
PIN 4
INPUT

Figure 5-2. +2 Vdc Reference Adjustment Setup

EQUIPMENT: Digital Multimeter .... HP 3465A

PROCEDURE:

1. Set the digital multimeter as follows:

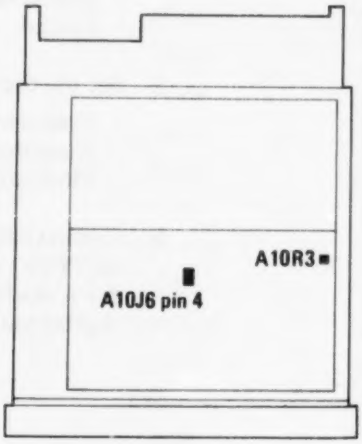
   Function ....Vdc
   Range 20V

2. Set the Signal Generator as follows:

   Frequency .... 140 MHz
   Amplitude .... −10 dBm
   Modulation ....AM 50%

3. Connect the digital multimeter to Test Point A10J6 pin 4 (+2V (R)) and adjust A10R3 (+2V REF ADJ) for a reading of 2.000 Vdc ±0.004 Vdc on the digital multimeter.

Bottom Internal View, Level 4


A10R3
A10J6 pin 4

5-9. AUDIO OSCILLATOR LEVEL ADJUSTMENT

REFERENCE: Service Sheet 6.

DESCRIPTION: The internal 1 kHz modulation source is adjusted to 0.707 Vrms ±0.007 Vrms at Test Point A10J6 pin 6. Then, the internal 400 Hz modulation source is checked to ensure that it is within the same limits.

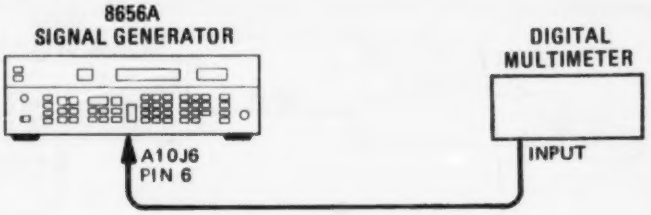


Figure 5-3. Audio Oscillator Level Adjustment Setup

EQUIPMENT: Digital Multimeter ....HP 3465A

PROCEDURE:

1. Set the digital multimeter as follows:

   Function .... Vac
   Range 2V

2. Set the Signal Generator as follows:

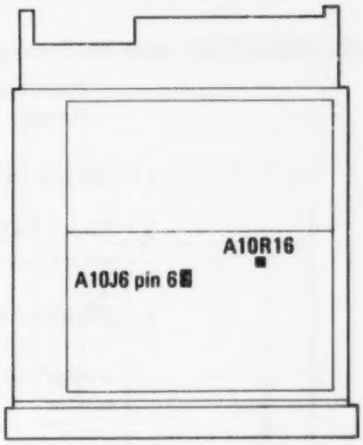
   Frequency .... Any
   Amplitude .... Any
   Modulation ....1 kHz AM

3. Connect the digital multimeter to Test Point A10J6 pin 6.

4. Adjust A10R16 (OSC ADJ) for a 0.707 Vrms ±0.007 Vrms reading on the digital multimeter.

5. Select the internal 400 Hz modulation source. Check that the 400 Hz oscillator level is within 0.707 Vrms ±0.007 Vrms. If it is not, repeat step 4 until both readings are within the specified limits.

Bottom Internal View, Level 4



5-10. AM OFFSET ADJUSTMENT

REFERENCE: Service Sheet 6.

DESCRIPTION: The dc offset of the AM Offset Buffer is adjusted for 0.000 Vdc ±0.001 Vdc at Test Point A10J6 pin 12 with the reference inputs to the Level DAC and AM% DAC grounded and the digital input to each programmaticaly set to zero.

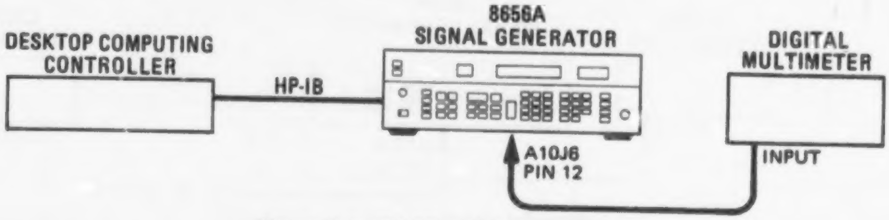
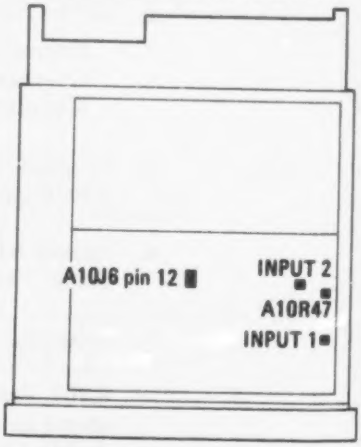


Figure 5-4. AM Offset Adjustment Setup

EQUIPMENT:

Digital Multimeter	HP 3465A
Desktop Computing Controller	HP 9825A
General I/O & Extended I/O ROM	HP 98213A
HP-IB Interface	HP 98034A

Bottom Internal View, Level 4



PROCEDURE:

1. Set the digital multimeter as follows:

Function	Vdc
Range	200 mV

2. Set the Signal Generator modulation off.
3. Short INPUT 1 and INPUT 2 Test Points to ground.
4. Connect the Desktop Computing Controller using the HP-IB Interface to the HP-IB connector on the rear panel of the Signal Generator.
5. Connect the digital multimeter to A10J6 pin 12.
6. Program the Desktop Computing Controller to set the digital inputs to the Level DAC and AM% DAC to zero as follows:
   [Controller talk and Signal Generator listen] "variable name"
   rem 7; wrt 707, "D0"

NOTE

To determine the HP-IB address of the Signal Generator, press the HP-IB ADRS key and read the internally-set, decimal address in the MODULATION Display. The factory set address is 07.

7. Adjust A10R47 (OFFSET ADJ) for 0.000 Vdc ±0.001 Vdc.
8. Remove the two shorts installed in step 3.

ADJUSTMENTS

5-11. 715 MHz SIDEBAND ADJUSTMENT

REFERENCE: Service Sheet 2.

DESCRIPTION: The 715 MHz Sideband adjustment is made so that both inputs to the Sideband Comparator are equal with the Signal Generator frequency set to 715 MHz. The dc voltage between Test Points A4TP10 and A4TP11 (which are the inputs to the Sideband Comparator) is adjusted to be less than 0.007 Vdc as the frequency is returned to 715 MHz from both 690 and 740 MHz in 5 MHz steps.

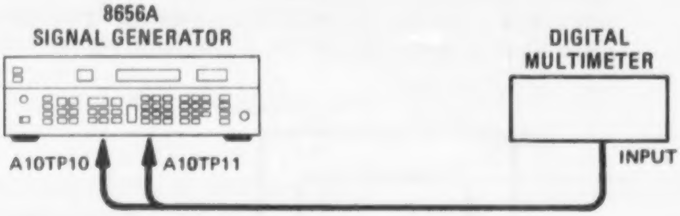


Figure 5-5. 715 MHz Sideband Adjustment Setup

EQUIPMENT: Digital Multimeter ....HP 3465A

PROCEDURE:

1. Set the digital multimeter as follows:
   Function ....Vdc
   Range .... 200 mV

2. Set the Signal Generator as follows:
   Frequency .... 715 MHz
   Frequency Increment .... 50 MHz
   Amplitude .... Any
   Modulation .... Off

   CAUTION

   DO NOT CONNECT TP13 to TP16 when the test points are not grounded.

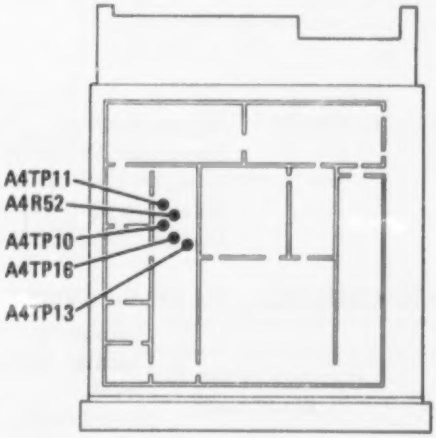
3. Connect the digital multimeter input between Test Points A4TP10 and A4TP11. Short Test Points A4TP13 and A4TP16 to ground.

4. Increment the frequency up to 765 and back to 715 MHz.

5. Adjust A4R52 (715 MHz ADJ) for 0 Vdc ±0.007 Vdc.

6. Remove the two shorts installed in step 3.

Top Internal View, Level 2



5-12. NOTCH FILTER ADJUSTMENTS

REFERENCE: Service Sheet 1.

DESCRIPTION: Each one of the Notch Filters is adjusted using a signal source set to 50, 100, 150, 200, 250, and 300 MHz. The 50 to 250 MHz Notch Filters are de-selected one at a time to pass that frequency. With each filter de-selected and its output centered on a spectrum analyzer display, the Notch Filter is then re-selected and adjusted for a minimum signal output on the spectrum analyzer.

The two 300 MHz Notch Filters are in the circuit all of the time. A 300 MHz signal source is applied to the input of each filter and its output is connected to a spectrum analyzer. Each filter is then adjusted for a minimum signal output.

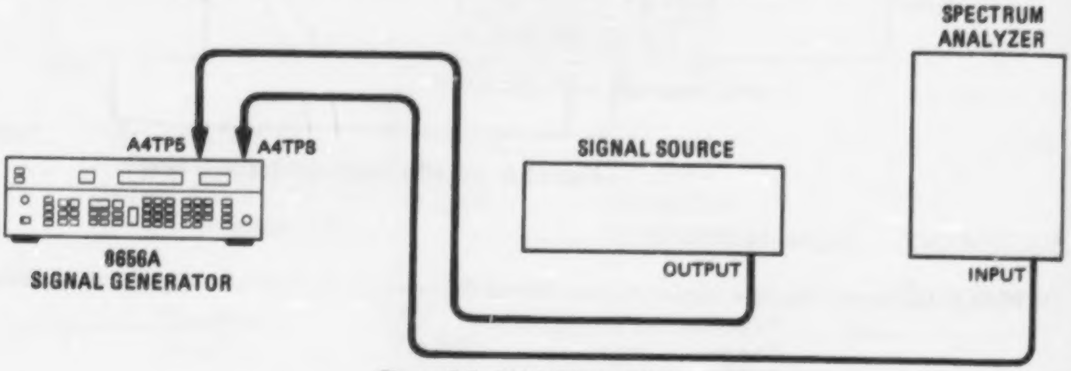


Figure 5-6. Notch Filters Adjustment Setup

EQUIPMENT:

Signal Source	HP 8640B
Spectrum Analyzer	HP 8558B
Adapter Probes (2)	HP 1250-1598
Adapters (2) N(m) to BNC(f)	HP 1250-0780
Cables (2) BNC(m) to SMC(f)	HP 08662-60080

PROCEDURE:

1. Set the signal source as follows:

Frequency	250.000 MHz
Counter Mode	Expand X10
Level	−20 dBm
Modulation	Off

2. Set the spectrum analyzer as follows:

Optimum Input	−10 dBm
Reference Level	0 dBm
Frequency Span/Div	500 kHz
Resolution Bandwidth	30 kHz

3. Set the Signal Generator as follows:

Frequency	950 MHz
Frequency Increment	50 MHz
Amplitude	Any
Modulation	Off

5-12. NOTCH FILTER ADJUSTMENTS (Cont'd)

PROCEDURE: (Cont'd)

4. Connect the signal source to the Signal Generator at RF Test Point A4TP5 using an adapter (HP part no. 1250-1598).

5. Connect the spectrum analyzer to the Signal Generator at RF Test Point A4TP8 using an adapter (HP part no. 1250-1598).

6. Adjust the spectrum analyzer to center the 250 MHz signal on the spectrum analyzer display.

7. Step the frequency down 50 MHz to 900 MHz.

8. Adjust A4C53 (250 MHz IF ADJ) for a minimum signal output on the spectrum analyzer display.

9. Tune the signal source to 200.000 MHz and center the 200 MHz signal on the spectrum analyzer display.

10. Step the frequency down 50 MHz to 850 MHz.

11. Adjust A4L36 (200 MHz IF ADJ) for a minimum signal output on the spectrum analyzer display.

12. Tune the signal source to 150.000 MHz and center the 150 MHz signal on the spectrum analyzer display.

13. Step the frequency down 50 MHz to 800 MHz.

14. Adjust A4L37 (150 MHz IF ADJ) for a minimum signal output on the spectrum analyzer display.

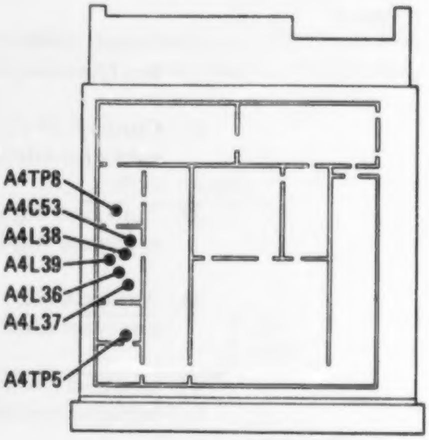
15. Tune the signal source to 100.000 MHz and center the 100 MHz signal on the spectrum analyzer display.

16. Step the frequency down 50 MHz to 750 MHz.

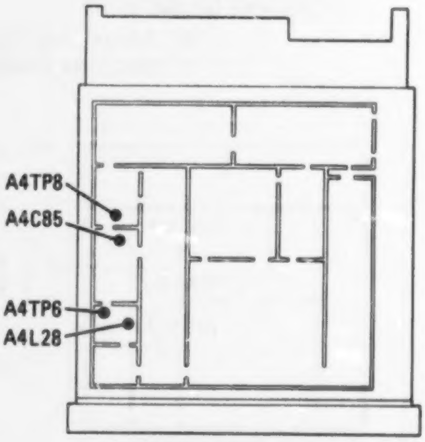
17. Adjust A4L38 (100 MHz IF ADJ) for a minimum signal output on the spectrum analyzer display.

18. Tune the signal source to 50.000 MHz and center the 50 MHz signal on the spectrum analyzer display.

Top Internal Views, Level 2



50 to 250 MHz IF Adjustments
(Steps 4—20)



300 MHz IF Adjustments
(Steps 21—26)

5-12. NOTCH FILTER ADJUSTMENTS (Cont'd)

PROCEDURE: (Cont'd)

19. Step the frequency up 50 MHz to 800 MHz.
20. Adjust A4L39 (50 MHz IF ADJ) for a minimum signal output on the spectrum analyzer display.
21. Connect the spectrum analyzer to the Signal Generator at RF Test Point A4TP6 using an adapter (HP part no. 1250-1598).
22. Tune the signal source to 300.000 MHz and center the 300 MHz signal on the spectrum analyzer display.
23. Adjust A4L28 (300 MHz IN IF ADJ) for a minimum signal output on the spectrum analyzer display.
24. Connect the spectrum analyzer to the Signal Generator at RF Test Point A4TP8 using an adapter (HP part no. 1250-1598).
25. Connect the signal source to the Signal Generator at RF Test Point A4TP6 using an adapter (HP part no. 1250-1598) and bypass A4L28 by placing a jumper across it.
26. Adjust A4C85 (300 MHz IF ADJ) for a minimum signal output on the spectrum analyzer display. Remove the jumper across A4L28.

5-13. HIGH FREQUENCY LOOP OFFSET ADJUSTMENT

REFERENCE: Service Sheet 2.

DESCRIPTION: The tune voltage ramp from the Loop Amplifier is disconnected from the High Frequency Oscillator Assembly—A5 and then it is adjusted for a symmetrical ramp using an oscilloscope.

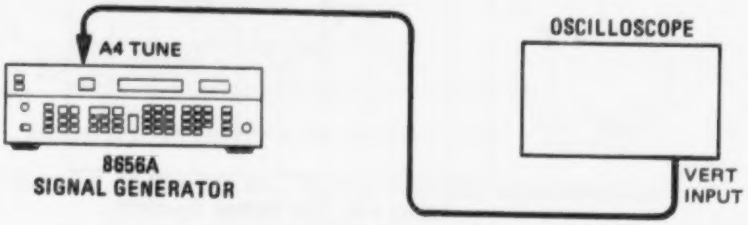


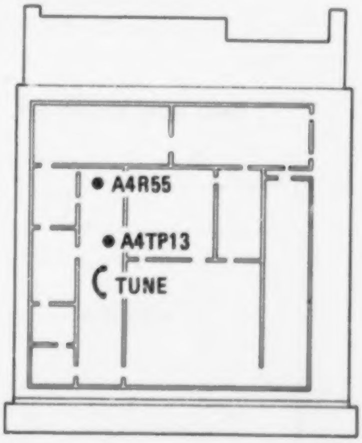
Figure 5-7. High Frequency Loop Offset Adjustment Setup

EQUIPMENT: Oscilloscope .... HP 1222A

PROCEDURE:

1. Set the oscilloscope as follows:
   - Vertical Gain 5V/div
   - Sweep Speed .... 10 ms/div
2. Set the Signal Generator as follows:
   - Frequency .... 140 MHz
   - Amplitude .... -10 dBm
   - Modulation .... 1 kHz (Int.) AM 50%
3. Disconnect the TUNE voltage wire (white-black-orange) from the High Frequency Oscillator Assembly—A5.
4. Connect oscilloscope to TUNE voltage wire (white-black-orange).
5. Short Test Point A4TP13 to ground.

Top Internal View, Level 2



6. Adjust A4R55 (OFFSET ADJ) for the most symmetrical ramp as analyzed on the oscilloscope (equal rise and fall times) as shown in Figure 5-8.
7. Remove the oscilloscope and reconnect the TUNE voltage wire to the High Frequency Oscillator Assembly—A5.
8. Remove the short installed in step 5.

5-13. HIGH FREQUENCY LOOP OFFSET ADJUSTMENT (Cont'd)

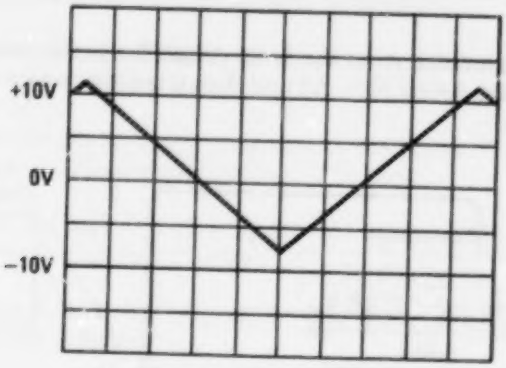


Figure 5-8. Tune Voltage Waveform

5-14. 50 MHz REFERENCE OSCILLATOR FREQUENCY ADJUSTMENT

REFERENCE: Service Sheet 13.

DESCRIPTION: The internal 50 MHz Reference Oscillator frequency is adjusted to 50.0000 MHz ±100 Hz at A3J5 using a frequency counter.

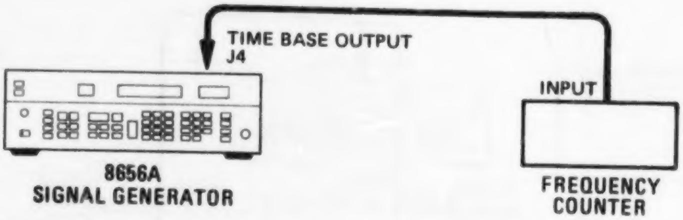


Figure 5-9. 50 MHz Reference Oscillator Frequency Adjustment Setup

QUIPMENT:

Frequency Counter	HP 5328A
Adapter N(m) to BNC(f)	HP 1250-0780
Cable BNC(m)	HP 10503A

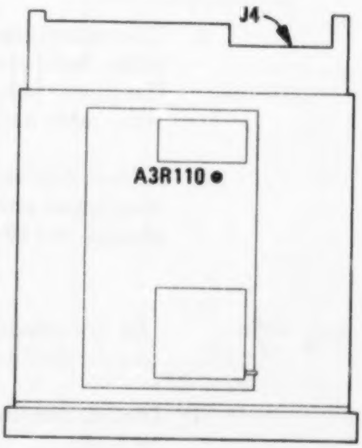
NOTE

If the Signal Generator has Option 001 installed disconnect coaxial cable A16W2 from the rear panel TIME BASE INPUT connector J3.

ROCEDURE:

1. Disconnect coaxial cable W5 from A3J5 (50 MHz Reference Oscillator output). Connect the frequency counter to A3J5 using the appropriate cable and adapters.
2. Adjust A3R110 (TB ADJ) for a frequency counter reading of 10.0000 MHz ±20 Hz.
3. Reconnect A16W2 to J3 if the Signal Generator has Option 001 installed.

Top Internal View, Level 1



5-15. 50 MHz REFERENCE OSCILLATOR LEVEL ADJUSTMENT

REFERENCE: Service Sheet 13.

DESCRIPTION: The output power level of the 50 MHz Reference Oscillator is adjusted for maximum power at A3J5 using a power meter.

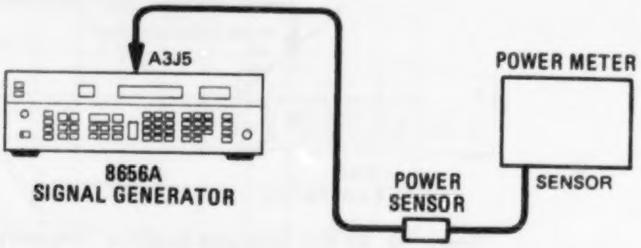


Figure 5-10. 50 MHz Reference Oscillator Level Adjustment Setup

EQUIPMENT:

Power Meter	HP 436A
Power Sensor	HP 8482A
Cable BNC(m) to SMC(f)	HP 08662-60080
Adapter N(f) to BNC(f)	HP 1250-0077
Adapter BNC(f) to BNC(f)	HP 1250-0080

PROCEDURE:

1. Set the power meter with the power meter sensor connected as follows:

   Mode .... dBm

2. Disconnect coaxial cable W5 from A3J5 (50 MHz Reference Oscillator output). Connect the power sensor to A3J5 using the appropriate cable and adapters.

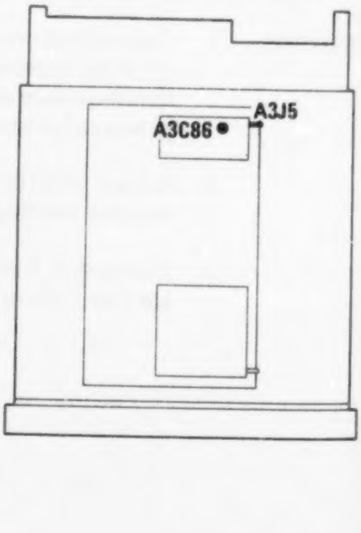
3. Adjust A3C86 (50 MHZ LEVEL ADJ) for a maximum power meter reading. The reading should be +16 dBm or greater.

NOTE

Do not remove the 50 MHz Section covers for this adjustment.

4. Disconnect the power meter and reconnect W5 to A3J5.

Top Internal View, Level 1



5-16. 60 TO 110 MHz OSCILLATOR FLATNESS ADJUSTMENT

REFERENCE: Service Sheet 8.

DESCRIPTION: The 60 to 110 MHz Low Frequency Oscillator is adjusted so that its output is ≤0.3 dB at 100 and 110 MHz at A3J4 using a power meter.

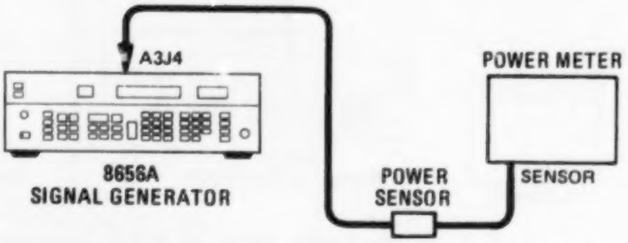


Figure 5-11. 60 to 110 MHz Oscillator Flatness Adjustment Setup

EQUIPMENT:

Power Meter	HP 436A
Power Sensor	HP 8482A
Adapter N(f) to BNC(m)	HP 1250-0077
Adapter BNC(f) to BNC(f)	HP 1250-0080
Cable BNC(m) to SMC(f)	HP 08662-60080

PROCEDURE:

1. Set the power meter with the power sensor connnected as follows:

   Mode .... dBm

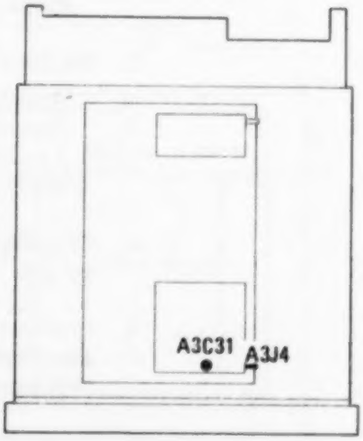
2. Set the Signal Generator as follows:

   Frequency .... 40 MHz
   Frequency Increment............. 10 MHz
   Amplitude .... Any
   Modulation .... Off

3. Disconnect coaxial cable W3 from A3J4 (60 to 110 MHz Oscillator output). Connect the power sensor to A3J4 using the appropriate cable and adapters.

4. Allow the reading on power meter to stabilize, then set the mode to dB (ref).

Top Internal View, Level 1



5. Adjust A3C31 (60 — 110 MHz FLATNESS ADJ) for a power meter difference of ≤1.3 dB as the frequency is stepped between 40 and 90 MHz in 10 MHz steps. The 60 to 110 MHz oscillator frequency will vary from 60 to 110 MHz.

6. Disconnect the power meter and reconnect W3 to A3J4.

5-17. 690 TO 740 MHz IF COMPENSATION ADJUSTMENT

REFERENCE: Service Sheets 1 and 3

DESCRIPTION: The power levels of the IF frequencies 690 to 740 MHz are measured at RF Test Point A4TP3 and adjusted for flatness within ±1.5 dB using a power meter.

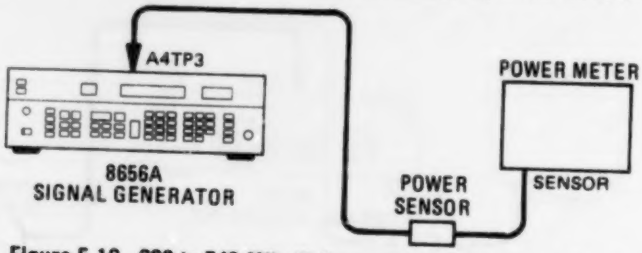


Figure 5-12. 690 to 740 MHz IF Compensation Adjustment Setup

EQUIPMENT:

Power Meter	HP 436A
Power Sensor	HP 8482A
Adapter Probe	HP 1250-1598
Adapter N(f) to BNC(m)	HP 1250-0077
Adapter BNC(f) to BNC(f)	HP 1250-0080
Cable BNC(m) to SMC(f)	HP 08662-60080

PROCEDURE:

1. Set the power meter with the power sensor connected as follows:

   Mode .... dBm

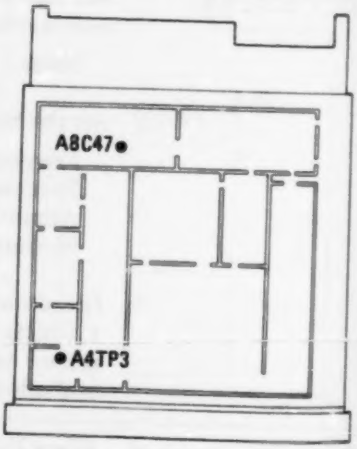
2. Set the Signal Generator as follows:

   Frequency .... 40 MHz
   Frequency Increment .... 10 MHz
   Amplitude .... Any
   Modulation .... Off

3. Zero the power meter and wait for zero LED to go out.

4. Connect the power sensor to the Signal Generator at RF Test Point A4TP3 using an adapter (HP part no. 1250-1598).

Top Internal View, Level 2



5. Step the Signal Generator frequency up in 10 MHz steps to 90 MHz recording the power meter reading at each frequency.

6. Step the Signal Generator to the frequency with the lowest reading and select the power meter dB (ref) mode.

7. Step the frequency up and down between 40 and 90 MHz and adjust A8C47 (COMP ADJ) until the maximum and minimum power meter readings are within 3 dB. The 690 to 740 MHz IF will then be flat to within ±1.5 dB.

5-18. 400 MHz BANDPASS FILTER ADJUSTMENT

REFERENCE: Service Sheet 3.

DESCRIPTION: The 400 MHz Bandpass Filter is adjusted for maximum power at RF Test Point A8TP3 using a power meter.

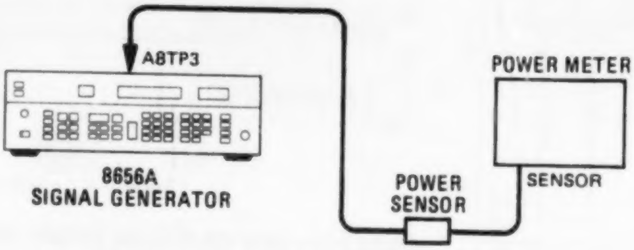


Figure 5-13. 400 MHz Bandpass Filter Adjustment Setup

EQUIPMENT:

Power Meter	HP 436A
Power Sensor	HP 8482A
Adapter Probe	HP 1250-1598
Adapter N(f) to BNC(m)	HP 1250-0077
Cable BNC(m) to SMC(f)	HP 08662-60080

PROCEDURE:

1. Set the power meter with the power sensor connected as follows:

   Mode .... dBm

2. Set the Signal Generator as follows:

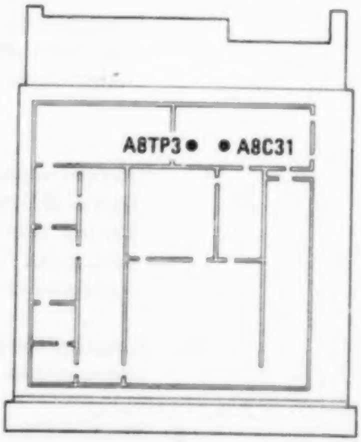
   Frequency .... Any
   Amplitude .... −10 dBm
   Modulation .... Off

3. Zero the power meter and wait for the zero LED to go out.

4. Connect the power sensor to the Signal Generator at RF Test Point A8TP3 using an adapter (HP part no. 1250-1598).

5. Adjust A8C31 (PEAK ADJ) for a maximum power meter reading.

Top Internal View, Level 2



5-19. LEVEL AND ALC LOOP DETECTOR ADJUSTMENTS

REFERENCE: Service Sheets 4 and 6.

DESCRIPTION: First, the reference level to the Level Digital to Analog Converter (DAC) is adjusted to +7.00 dBm ±0.02 dB. Then the detector bias reference level to the ALC Amplifier is adjusted to -4.00 dBm ±0.02 dB.

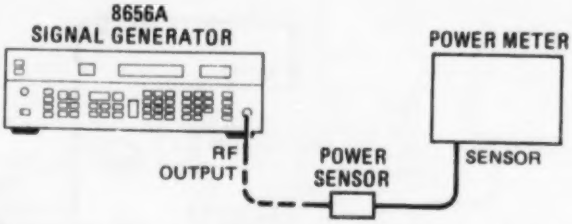


Figure 5-14. Level and ALC Loop Detector Adjustment Setup

EQUIPMENT:

Power Meter	HP 436A
Power Sensor	HP 8482A

PROCEDURE:

1. Set the power meter with power sensor connected as follows:

Mode	dBm

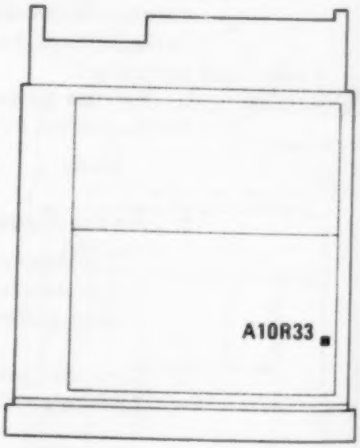
2. Set the Signal Generator as follows:

Frequency	800 MHz
Amplitude	+7 dBm
Modulation	Off
Amplitude Increment	11 dB

NOTE

Before making the adjustment, all internal RF covers must be installed and the instrument must be warmed up for a minimum of 2 hours. (The internal RF top cover is removed to permit access).

Bottom Internal View, Level 4



3. Connect the power sensor to the RF OUTPUT connector on the Signal Generator.

4. Set the Signal Generator RESET/STBY/ON switch to STBY and zero the power meter.

5. Wait for the power meter zero LED to go out, then set the RESET/STBY/ON switch to the ON position.

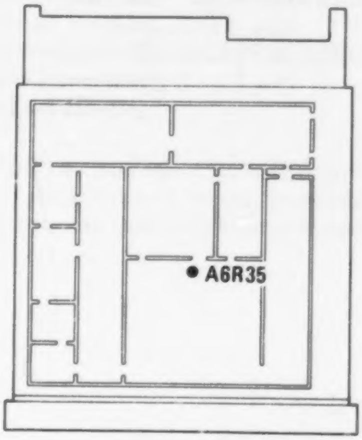
6. Adjust A10R33 (LEVEL ADJ) for a reading of +7.00 dBm ±0.02 dB on the power meter.

5-19. LEVEL AND ALC LOOP DETECTOR ADJUSTMENTS (Cont'd)

PROCEDURE: (Cont'd)

7. Step the Signal Generator amplitude down to −4 dBm.
8. Adjust A6R35 (DET ADJ) for a reading of −4.00 dBm ±0.02 dB on the power meter.
9. Repeat steps 6, 7 and 8 until both readings are within the required tolerances.

Top Internal View, Level 2



5-20. HETERODYNE BAND ACCURACY AND FLATNESS ADJUSTMENTS

REFERENCE: Service Sheet 5.

DESCRIPTION: The accuracy and flatness of the heterodyne band are adjusted for an equal power difference from 0 dBm at 10 MHz and 123 MHz and power variation not greater than ±0.5 dB for frequencies between 3 MHz and 123 MHz.

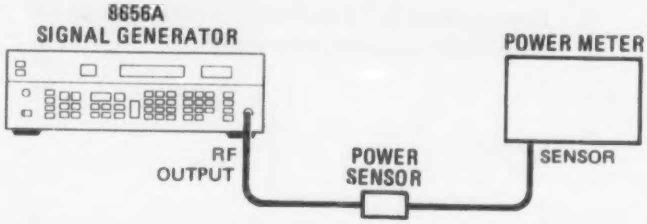


Figure 5-15. Heterodyne Band Accuracy and Flatness Adjustment Setup

EQUIPMENT:

Power Meter	HP 436A
Power Sensor	HP 8482A

PROCEDURE:

1. Set the power meter with the power sensor connected as follows:

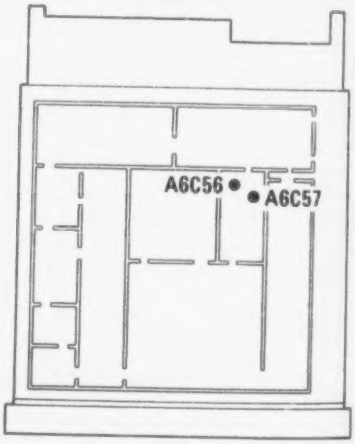
Mode	dBm

2. Set the Signal Generator as follows:

Frequency	10 MHz
Frequency Increment	5 MHz
Amplitude	0 dBm
Modulation	Off

3. Connect the power sensor to RF OUTPUT connector on the Signal Generator.
4. Set the Signal Generator RESET/STBY/ON switch to STBY and zero the power meter.
5. Wait for the power meter zero LED to go out, then set the RESET/STBY/ON switch to the ON position.

Top Internal View, Level 2



6. Adjust A6C56 (ACC ADJ) for a 0 dBm ±0.5 dB reading on the power meter.
7. Change the frequency to 123 MHz and adjust A6C57 (FLAT ADJ) for a 0 dBm ±0.5 dB reading on the power meter.

NOTES

1. If A6C57 does not have the range to adjust the amplitude at 123 MHz to 0.0 dBm ±0.5 dB, repeat step 6 adjusting A6C56 to increase or decrease the amplitude until both adjustments are within the specified limits. A6C56 is used to shift the amplitude level of the heterodyne band.

5-20. HETERODYNE BAND ACCURACY AND FLATNESS ADJUSTMENTS (Cont'd)

PROCEDURE:
(Cont'd)

NOTES (Cont'd)

2. This note applies to instruments with serial prefixes 2032A and below. If A6C56 cannot be adjusted so A6C57 (note 1) will meet the specification, change to the capacitor listed in Table 6-3 (2.5—5.5 pF) and repeat this procedure.

8. Step the frequency between 3 MHz and 123 MHz. The amplitude variation from maximum to minimum should not exceed 1 dB. If amplitude variation is greater than 1 dB repeat steps 6 and 7 to compensate the flatness so that amplitude remains within 0.0 dBm ±0.5 dB.

5-21. AM% AND ALC LOOP AM ADJUSTMENTS

REFERENCE: Service Sheets 4 and 6.

DESCRIPTION: The reference level to the AM% Digital to Analog Converter (DAC) is adjusted for an average amplitude modulation of 21.4%. The AM reference to the ALC Amplifier is adjusted for minimum distortion of the modulation.

NOTE

The AM Offset, Level, and Heterodyne Flatness adjustments must be performed before performing these adjustments. Refer to paragraphs 5-10, 5-19 and 5-20.

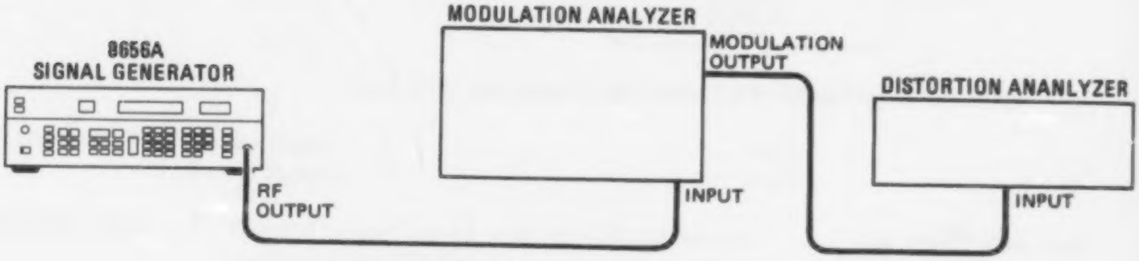


Figure 5-16. AM% and ALC Loop AM Adjustments Setup

EQUIPMENT

Modulation Analyzer	HP 8901A
Distortion Analyzer	HP 339A
AM/FM Test Source (required modulation analyzer verification of incidental AM)	HP 11715A
Test Oscillator	HP 651B
Cable (UG-210/U type N connectors)	HP 11500B
Cable (UG-88C/U BNC and dual banana plug connectors)	HP 11001A

PROCEDURE:

1. Set the modulation analyzer as follows:

Measurement	AM
Detection	AVG
HP Filter	50 Hz
LP Filter	15 kHz

2. Set the Signal Generator as follows:

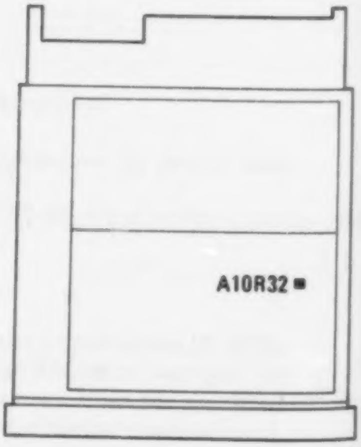
Frequency	200 MHz
Amplitude	+4 dBm
Modulation	1 kHz (Int.) AM 30%
Amplitude Increment	8 dB

3. Adjust A10R32 (AM% ADJ) for a reading of 21.40% on the modulation analyzer.

NOTE

Do not remove any of the internal RF covers for this adjustment.

Bottom Internal View, Level 4



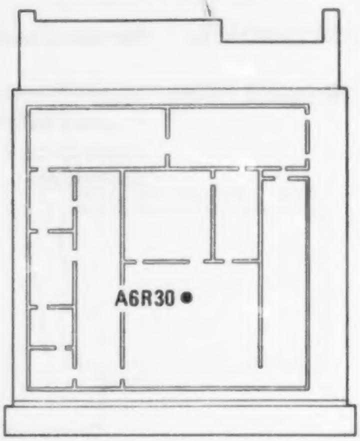
5-21. AM% AND ALC LOOP AM ADJUSTMENTS (Cont'd)

4. Set the Signal Generator as follows:

Frequency .... 123 MHz
Amplitude .... −4 dBm
Modulation .... AM 70%

5. Adjust A6R30 (AM ADJ) for a minimum reading on the Distortion Analyzer. Typically the distortion is less than 3%.

Top Internal View, Level 2



5-22. FM DEVIATION ADJUSTMENT

REFERENCE: Service Sheet 12.

DESCRIPTION: The FM deviation is adjusted with a maximum FM peak deviation frequency of 99 kHz entered into the Signal Generator. The carrier frequency is stepped down in 10 MHz steps from 990 to 940 MHz and A10R64 is adjusted for an equal error around 99 kHz deviation.

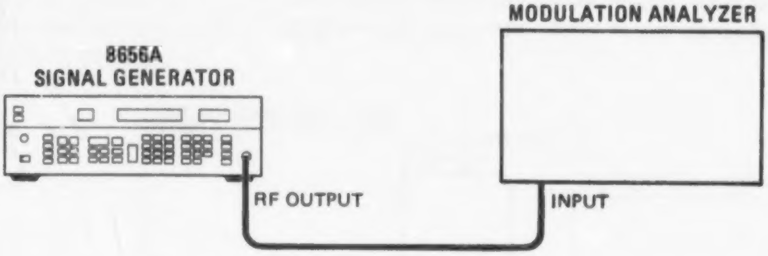


Figure 5-17. FM Deviation Adjustment Setup

EQUIPMENT:

Modulation Analyzer	HP 8901A
Cable UG-210/U (Type N)	HP 11500A

PROCEDURE:

1. Set the modulation analyzer as follows:

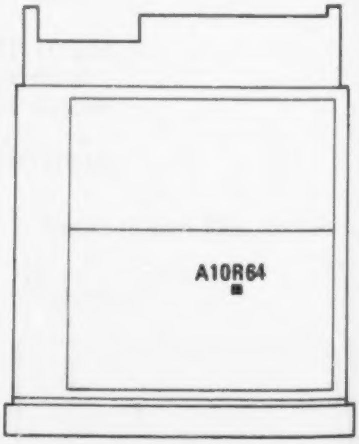
Measurement	FM
Detector	+Peak
HP Filter	300 Hz
LP Filter	3 kHz

2. Set the Signal Generator as follows:

Frequency	990 MHz
Frequency Increment	10 MHz
Amplitude	+4 dBm
Modulation	1 kHz (Int.) FM 99 kHz

3. Connect the modulation analyzer input to the RF OUTPUT connector on the Signal Generator.

Bottom Internal View, Level 4



4. Adjust A10R64 (FM ADJ) for a 99.0 kHz deviation reading on the modulation analyzer.

5. Step the frequency down from 990 to 940 MHz and record the deviation at each of the 10 MHz steps.

6. Adjust A10R64 for equal error ±2 kHz from 99 kHz at the frequencies of maximum and minimum peak kHz deviation.

5-23. FM FREQUENCY RESPONSE ADJUSTMENT

REFERENCE: Service Sheet 10.

DESCRIPTION: The FM frequency response is adjusted with a peak deviation frequency of 99 kHz as an external modulation source is tuned between 50 Hz and 1 kHz.

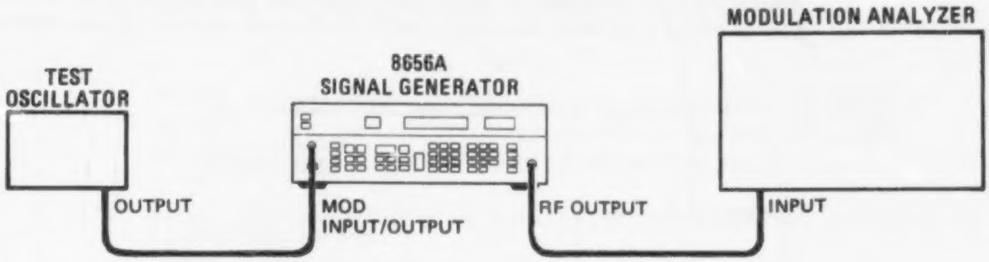


Figure 5-18. FM Frequency Response Setup

EQUIPMENT:

Test Oscillator	HP 651B
Modulation Analyzer	HP 8901A

PROCEDURE:

1. Set the Signal Generator as follows:

Frequency	90 MHz
Ampliutde	0.0 dBm
Modulation	Ext. FM 99 kHz

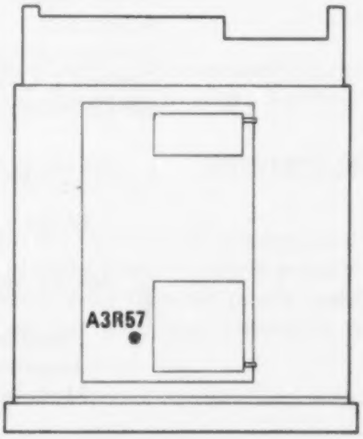
2. Set the test oscillator as follows:

Frequency	1 kHz
Amplitude Coarse	CCW

3. Set the modulation analyzer as follows:

Measurement	FM
Detector	Peak+
LP Filter	15 kHz

Top Internal View, Level 1



4. Connect the equipment as shown in Figure 5-18.
5. Rotate the test oscillator output level CW until the LO EXT LED on the front panel of the Signal Generator goes out. Both the HI EXT and LO EXT LEDs must be out.
6. Record the deviation reading on the modulation analyzer.
7. Tune the test oscillator frequency to 50 Hz.
8. Adjust A3R57 (FM ADJ) for a difference of ±1.0 kHz as the external modulation signal is tuned between 50 Hz and 1 kHz.

5-24. ATTENUATOR ADJUSTMENTS

REFERENCE: Service Sheet 7.

DESCRIPTION: Each of the five attenuator sections is actuated separately via HP-IB using a Desktop Computing Controller so that they can be individually adjusted. The wire adjustment loops form capacitors C1—3, 6 and 8. Each is adjusted in relation to the associated series resistor. A reference power level with all attenuator pads out is taken with the power meter and each attenuator pad is adjusted relative to that reference.

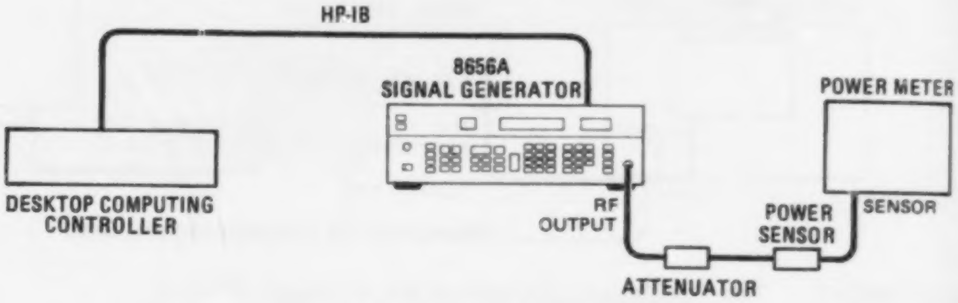


Figure 5-19. Attenuator Adjustment Setup

EQUIPMENT:

Power Meter	HP 436A
Power Sensor	HP 8484A
Attenuator	HP 8491A Option 020
Desktop Computing Controller	HP 9825A
General I/O & Extended I/O ROM	HP 98213A
HP-IB Interface	HP 98034A

PROCEDURE:

1. Set the power meter with the power sensor connected as follows:

   Mode .... dBm

2. Set the Signal Generator as follows:

   Frequency .... 990 MHz
   Amplitude .... 0 dBm
   Modulation .... Off

3. Connect the Desktop Computing Controller using the HP-IB Interface to the HP-IB connector on the rear panel of the Signal Generator.

4. Connect the power sensor to the attenuator and the attenuator to the RF OUTPUT connector on the Signal Generator.

5. Set the Signal Generator RESET/STBY/ON switch to STBY and zero the Power Meter.

6. Wait for the power meter zero LED to go out, then set the RESET/STBY/ON switch to the ON position.

5-24. ATTENUATOR ADJUSTMENTS (Cont'd)

7. Wait for the power meter reading to stabilize, then select the dB(ref) mode.

8. Program the Desktop Computer to select the desired pad. When the HP 9825A Desktop Computing Controller is used as the controller, the pad is selected by entering the statement shown in Table 5-3.

   (Controller talk and Signal Generator listen) "variable name"

NOTE

To determine the address of the Signal Generator, press the HPIB ADRS key and read the decimal equivalent of the address in the MODULATION display. The factory set address is 07.

9. Only remove the internal RF cover from the pad being adjusted. See Figure 5-20.

10. Adjust the wire loop capacitor for the power meter reading specified for the pad being adjusted. See Table 5-3.

NOTE

Cover must be tight.

11. Replace the internal RF cover and observe the power meter reading. If it has changed, remove the cover and readjust the wire loop to give the correct power meter reading with the cover in place.

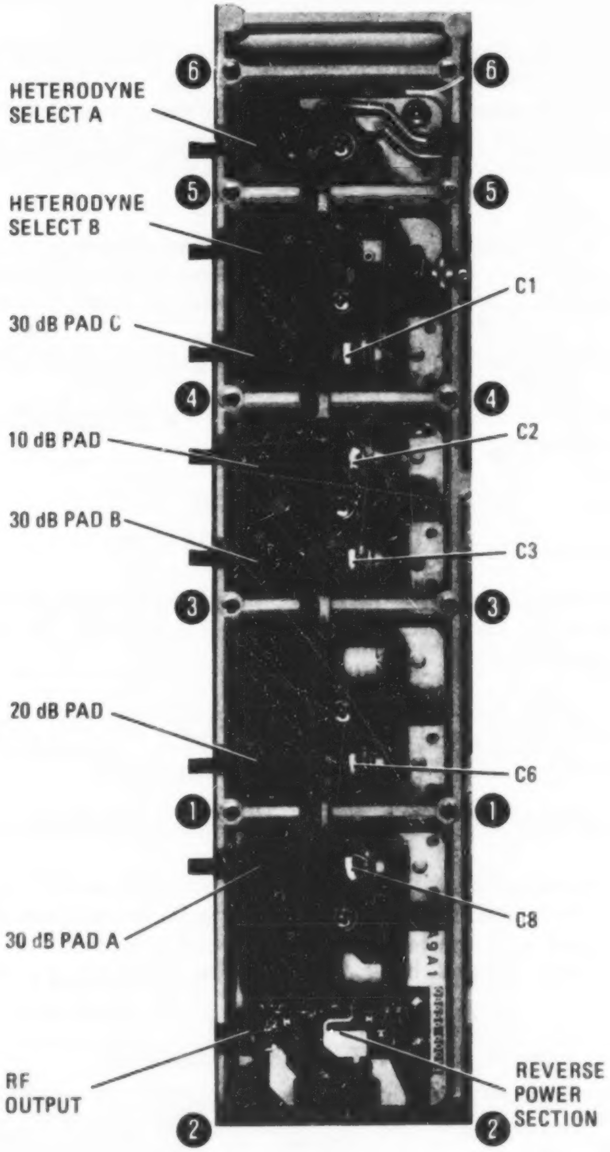
12. Place the power meter in dBm mode, select 0 dBm by entering the statement shown in Table 5-3 and repeat steps 5, 6, 7, 8, 10, and 11 until the limits in step 10 are met without further adjustment of the wire loop capacitors.

13. Repeat steps 5 through 12 to adjust the other attenuator pads.

14. After the adjustments have been completed, replace the internal RF bottom cover, then place the attenuator plate clamp into position and press down to firmly position the cover flush with the casting. Activate each pad and verify that the power meter reading is still within the specified limits. Readjust the wire loop capacitor, if necessary.

Table 5-3. Attenuator Pad Adjustment Information

Wire Loop Capacitor	Pad	Power Meter Reading	Statement to Select Pad with 9825A Controller
C2	10 dB	10 ± 0.1 dB	rem 7; wrt 707, "A4"
C6	20 dB	20 ± 0.1 dB	rem 7; wrt 707, "A2"
C8	30 dB A	30 ± 0.05 dB	rem 7; wrt 707, "A5"
C3	30 dB B	30 ± 0.05 dB	rem 7; wrt 707, "A3"
C1	30 dB C	30 ± 0.05 dB	rem 7; wrt 707, "A1"
None	None	0 ± 0.5 dB	rem 7; wrt 707, "A0"


⑥
⑥
HETERODYNE SELECT A
⑤
⑤
HETERODYNE SELECT B
C1
30 dB PAD C
④
④
10 dB PAD
C2
30 dB PAD B
C3
③
③
20 dB PAD
C6
①
①
C8
30 dB PAD A
9A1
RF OUTPUT
REVERSE POWER SECTION
②
②

NOTE:

SCREWS SECURING THE ATTENUATOR PLATE CLAMP MUST BE TIGHTENED IN THE ① TO ⑥ ORDER SHOWN'

Figure 5-20. Attenuator Adjustment Locations

⚠ 5-25. OPTION 001 10 MHz REFERENCE OSCILLATOR FREQUENCY ADJUSTMENT

REFERENCE: Service Sheet 22.

DESCRIPTION: The Option 001 10 MHz Reference Oscillator frequency is adjusted to 10.000 MHz ±10.0 Hz using a frequency counter.

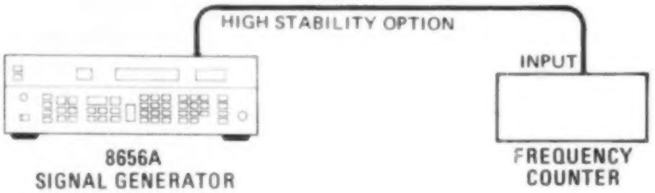


Figure 5-21. 10 MHz Reference Oscillator Frequency Adjustment Setup

EQUIPMENT: Frequency Counter .... HP 5328A

PROCEDURE:

WARNING

To avoid the possibility of hazardous electrical shock, disconnect the power cable from Main power before disconnecting the fan. Electrical power is connected to the fan whenever the power cable is connected to Mains power.

CAUTION

Use caution when removing the fan shroud from the casting. A ground wire is connected between the fan and the casting.

1. Remove the fan shroud from the rear of instrument. (Refer to Disassembly Procedures in Section VIII.)
2. Remove the COARSE and FINE screw-on adjustment covers.
3. Connect the frequency counter to the TIME BASE HIGH STABILITY OPTION connector (A16J1) on the rear panel of the Signal Generator.
4. Adjust the COARSE and FINE adjustments for a reading of 10.000 MHz ±10.0 Hz on the frequency counter.
5. Replace adjustment covers, fan shroud and series regulator cover.

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

This section contains information for ordering parts. Table 6-2 lists abbreviations used in the parts list and throughout the manual. Table 6-3 lists all replaceable parts in reference designator order. Table 6-4 contains the names and addresses that correspond to the manufacturer's code numbers.

6-2. ABBREVIATIONS

Table 6-2 lists abbreviations used in the parts list, schematics, and throughout the manual. In some cases, two forms of the abbreviation are used, one all in capitals letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower case and upper case letters.

6-3. REPLACEABLE PARTS LIST

Table 6-3 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies and their components in alphanumeric order by reference designation.

b. Chassis-mounted parts in alphanumeric order by reference designation.

c. Mechanical parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number.

b. Part number check digit (CD).

c. The total quantity (Qty) for the entire instrument except for option assemblies.

d. The description of the part.

e. A typical manufacturer of the part in a five-digit code.

f. The manufacturer's number for the part.

NOTE

The total quantity for each part is given only once, that is, at the first occurrence of the part number in the list. The total quantities for optional assemblies are totalled by assembly and not integrated into the standard list.

6-4. FACTORY SELECTED PARTS (*)

Parts marked with an asterisk (*) are factory selected parts. The value listed in the parts list is the nominal value. Refer to Sections V and VIII of this manual for information on determining what value to use for replacement.

6-5. PARTS LIST BACKDATING (†)

Parts marked with a dagger (†) are different in Signal Generators with serial number prefixes lower than the one that this manual applies to directly. Table 7-1 lists the backdating changes by serial number prefix. Table 7-2 lists components affected by each change.

6-6. PARTS LIST UPDATING (Change Sheet)

Production changes to Signal Generators made after the publication date of this manual are accompanied by a change in the serial number prefix. Changes to the parts list are recorded by serial number prefix on a MANUAL CHANGES supplement. Also, parts list errors are noted in the ERRATA portion of the MANUAL CHANGES supplement.

6-7. ILLUSTRATED PARTS BREAKDOWNS

Most mechanical parts are identified in Figures 6-1 through 6-9. These figures are located at the end of the replaceable parts table.

6-8. ORDERING INFORMATION

To order a part listed in the replaceable parts table, include the Hewlett-Packard part number (with the check digit) and the quantity required. Address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, include the instrument model number,

ORDERING INFORMATION (Cont'd)

instrument serial number, description and function of the part, and the quantity of parts required. Address the order to the nearest Hewlett-Packard office.

NOTE

> *Within the USA, it is better to order directly from the HP Parts Center in Mountain View, California. Ask your nearest HP office for information and forms for the "Direct Mail Order System".*

6-9. RECOMMENDED SPARES LIST

Stocking spare parts for an instrument is often done to ensure quick return to service after a malfunction occurs. Hewlett-Packard has prepared a "Recommended Spares" list for this instrument. The contents of the list are based on failure reports and repair data. Quantities given are for one year of parts support. A complimentary copy of the "Recommended Spares" list may be requested from your nearest Hewlett-Packard office.

When stocking parts to support more than one Signal Generator or to support a variety of Hewlett-Packard instruments, it may be more economical to work from one consolidated list rather than simply adding together stocking quantities from the individual instrument lists. Hewlett-Packard will prepare consolidated "Recommended Spares" lists for any number or combination of instruments. Contact your nearest Hewlett-Packard office for details.

Table 6-1. Reference Designations

REFERENCE DESIGNATIONS

A	assembly
AT	attenuator; isolator; termination
B	fan; motor
BT	battery
C	capacitor
CP	coupler
CR	diode; diode thyristor; varactor
DC	directional coupler
DL	delay line
DS	annunciator; signaling device (audible or visual); lamp; LED
E	miscellaneous electrical part
F	fuse
FL	filter
H	hardware
HY	circulator
J	electrical connector (stationary portion); jack
K	relay
L	coil; inductor
M	meter
MP	miscellaneous mechanical part
P	electrical connector (movable portion); plug
Q	transistor: SCR; triode thyristor
R	resistor
RT	thermistor
S	switch
T	transformer
TB	terminal board
TC	thermocouple
TP	test point
U	integrated circuit; microcircuit
V	electron tube
VR	voltage regulator; breakdown diode
W	cable; transmission path; wire
X	socket
Y	crystal unit (piezo-electric or quartz)
Z	tuned cavity; tuned circuit

Table 6-2. Abbreviations (1 of 2)

ABBREVIATIONS

A	ampere
ac	alternating current
ACCESS	accessory
ADJ	adjustment
A/D	analog-to-digital
AF	audio frequency
AFC	automatic frequency control
AGC	automatic gain control
AL	aluminum
ALC	automatic level control
AM	amplitude modulation
AMPL	amplifier
APC	automatic phase control
ASSY	assembly
AUX	auxiliary
avg	average
AWG	American wire gauge
BAL	balance
BCD	binary coded decimal
BD	board
BE CU	beryllium copper
BFO	beat frequency oscillator
BH	binder head
BKDN	breakdown
BP	bandpass
BPF	bandpass filter
BRS	brass
BWO	backward-wave oscillator
CAL	calibrate
ccw	counter-clockwise
CER	ceramic
CHAN	channel
cm	centimeter
CMO	cabinet mount only
COAX	coaxial
COEF	coefficient
COM	common
COMP	composition
COMPL	complete
CONN	connector
CP	cadmium plate
CRT	cathode-ray tube
CTL	complementary transistor logic
CW	continuous wave
cw	clockwise
cm	centimeter
D/A	digital-to-analog
dB	decibel
dBm	decibel referred to 1 mW
dc	direct current
deg	degree (temperature interval or difference)
...°	degree (plane angle)
°C	degree Celsius (centigrade)
°F	degree Fahrenheit
°K	degree Kelvin
DEPC	deposited carbon
DET	detector
diam	diameter
DIA	diameter (used in parts list)
DIFF AMPL	differential amplifier
div	division
DPDT	double-pole, double-throw
DR	drive
DSB	double sideband
DTL	diode transistor logic
DVM	digital voltmeter
ECL	emitter coupled logic
EMF	electromotive force
EDP	electronic data processing
ELECT	electrolytic
ENCAP	encapsulated
EXT	external
F	farad
FET	field-effect transistor
F/F	flip-flop
FH	flat head
FIL H	fillister head
FM	frequency modulation
FP	front panel
FREQ	frequency
FXD	fixed
g	gram
GE	germanium
GHz	gigahertz
GL	glass
CRD	ground(ed)
H	henry
h	hour
HET	heterodyne
HEX	hexagonal
HD	head
HDW	hardware
HF	high frequency
HG	mercury
HI	high
HP	Hewlett-Packard
HPF	high pass filter
HR	hour (used in parts list)
HV	high voltage
Hz	Hertz
IC	integrated circuit
ID	inside diameter
IF	intermediate frequency
IMPG	impregnated
in	inch
INCD	incandescent
INCL	include(s)
INP	input
INS	insulation
INT	internal
kg	kilogram
kHz	kilohertz
kΩ	kilohm
kV	kilovolt
lb	pound
LC	inductance-capacitance
LED	light-emitting diode
LF	low frequency
LG	long
LH	left hand
LIM	limit
LIN	linear taper (used in parts list)
lin	linear
LK WASH	lock washer
LO	low; local oscillator
LOG	logarithmic taper (used in parts list)
log	logrithm(ic)
LPF	low pass filter
LV	low voltage
m	meter (distance)
mA	milliampere
MAX	maximum
MΩ	megohm
MEG	meg (10^6) (used in parts list)
MET FLM	metal film
MET OX	metallic oxide
MF	medium frequency; microfarad (used in parts list)
MFR	manufacturer
mg	milligram
MHz	megahertz
mH	millihenry
mho	mho
MIN	minimum
min	minute (time)
...'	minute (plane angle)
MINAT	miniature
mm	millimeter

NOTE

All abbreviations in the parts list will be in upper-case.

Table 6-2. Abbreviations (2 of 2)

MOD	modulator
MOM	momentary
MOS	metal-oxide semiconductor
ms	millisecond
MTG	mounting
MTR	meter (indicating device)
mV	millivolt
mVac	millivolt, ac
mVdc	millivolt, dc
mVpk	millivolt, peak
mVp-p	millivolt, peak-to-peak
mVrms	millivolt, rms
mW	milliwatt
MUX	multiplex
MY	mylar
μA	microampere
μF	microfarad
μH	microhenry
μmho	micromho
μs	microsecond
μV	microvolt
μVac	microvolt, ac
μVdc	microvolt, dc
μVpk	microvolt, peak
μVp-p	microvolt, peak-to-peak
μVrms	microvolt, rms
μW	microwatt
nA	nanoampere
NC	no connection
N/C	normally closed
NE	neon
NEG	negative
nF	nanofarad
NI PL	nickel plate
N/O	normally open
NOM	nominal
NORM	normal
NPN	negative-positive-negative
NPO	negative-positive zero (zero temperature coefficient)
NRFR	not recommended for field replacement
NSR	not separately replaceable
ns	nanosecond
nW	nanowatt
OBD	order by description
OD	outside diameter
OH	oval head
OP AMPL	operational amplifier
OPT	option
OSC	oscillator
OX	oxide
oz	ounce
Ω	ohm
P	peak (used in parts list)
PAM	pulse-amplitude modulation
PC	printed circuit
PCM	pulse-code modulation; pulse-count modulation
PDM	pulse-duration modulation
pF	picofarad
PH BRZ	phosphor bronze
PHL	Phillips
PIN	positive-intrinsic-negative
PIV	peak inverse voltage
pk	peak
PL	phase lock
PLO	phase lock oscillator
PM	phase modulation
PNP	positive-negative-positive
P/O	part of
POLY	polystyrene
PORC	porcelain
POS	positive; position(s) (used in parts list)
POSN	position
POT	potentiometer
p-p	peak-to-peak
PP	peak-to-peak (used in parts list)
PPM	pulse-position modulation
PREAMPL	preamplifier
PRF	pulse-repetition frequency
PRR	pulse repetition rate
ps	picosecond
PT	point
PTM	pulse-time modulation
PWM	pulse-width modulation
PWV	peak working voltage
RC	resistance-capacitance
RECT	rectifier
REF	reference
REG	regulated
REPL	replaceable
RF	radio frequency
RFI	radio frequency interference
RH	round head; right hand
RLC	resistance-inductance-capacitance
RMO	rack mount only
rms	root-mean-square
RND	round
ROM	read-only memory
R&P	rack and panel
RWV	reverse working voltage
S	scattering parameter
s	second (time)
"	second (plane angle)
S-B	slow-blow (fuse) (used in parts list)
SCR	silicon controlled rectifier; screw
SE	selenium
SECT	sections
SEMICON	semiconductor
SHF	superhigh frequency
SI	silicon
SIL	silver
SL	slide
SNR	signal-to-noise ratio
SPDT	single-pole, double-throw
SPG	spring
SR	split ring
SPST	single-pole, single-throw
SSB	single sideband
SST	stainless steel
STL	steel
SQ	square
SWR	standing-wave ratio
SYNC	synchronize
T	timed (slow-blow fuse)
TA	tantalum
TC	temperature compensating
TD	time delay
TERM	terminal
TFT	thin-film transistor
TGL	toggle
THD	thread
THRU	through
TI	titanium
TOL	tolerance
TRIM	trimmer
TSTR	transistor
TTL	transistor-transistor logic
TV	television
TVI	television interference
TWT	traveling wave tube
U	micro (10^{-6}) (used in parts list)
UF	microfarad (used in parts list)
UHF	ultrahigh frequency
UNREG	unregulated
V	volt
VA	voltampere
Vac	volts, ac
VAR	variable
VCO	voltage-controlled oscillator
Vdc	volts, dc
VDCW	volts, dc, working (used in parts list)
V(F)	volts, filtered
VFO	variable-frequency oscillator
VHF	very-high frequency
Vpk	volts, peak
Vp-p	volts, peak-to-peak
Vrms	volts, rms
VSWR	voltage standing wave ratio
VTO	voltage-tuned oscillator
VTVM	vacuum-tube voltmeter
V(X)	volts, switched
W	watt
W/	with
WIV	working inverse voltage
WW	wirewound
W/O	without
YIG	yttrium-iron-garnet
Z_o	characteristic impedance

NOTE

All abbreviations in the parts list will be in upper-case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	08656-60065	7	1	KEYBOARD ASSEMBLY	28480	08656-60065
A1J1	1251-5923	0	1	CONNECTOR 14-PIN M POST TYPE	28480	1251-5923
A1S1	5060-9436	7	48	PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1805	8	1	KEY CAP, HALF 'V'	28480	5041-1805
A1S2	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1793	3	1	KEY CAP, HALF 'SEQ'	28480	5041-1793
A1S3	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1806	9	1	KEY CAP, HALF 'MV'	28480	5041-1806
A1S4	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1789	7	1	KEY CAP, HALF 'STORE'	28480	5041-1789
A1S5	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1807	0	1	KEY CAP, HALF 'UV'	28480	5041-1807
A1S6	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1790	0	1	KEY CAP, HALF 'RECALL'	28480	5041-1790
A1S7	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1792	2	1	KEY CAP, HALF 'LOCAL'	28480	5041-1792
A1S8	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1791	1	1	KEY CAP, HALF 'DISPLAY'	28480	5041-1791
A1S9	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1796	6	1	KEY CAP, HALF 'MHZ'	28480	5041-1796
A1S10	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1802	5	1	KEY CAP, HALF 'DBM'	28480	5041-1802
A1S11	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1795	5	1	KEY CAP, HALF 'KHZ'	28480	5041-1795
A1S12	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1803	6	1	KEY CAP, HALF 'DBF'	28480	5041-1803
A1S13	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1800	3	1	KEY CAP, HALF '%'	28480	5041-1800
A1S14	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1801	4	1	KEY CAP, HALF 'DB'	28480	5041-1801
A1S15	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1813	0	1	KEY CAP, HALF 'BACKSPACE'	28480	5041-1813
A1S16	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1804	7	1	KEY CAP, HALF 'EMF'	28480	5041-1804
A1S17	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1786	4	1	KEY CAP, HALF 'NUMBER 8'	28480	5041-1786
A1S18	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1784	2	2	KEY CAP, HALF 'NUMBER 9'	28480	5041-1784
A1S19	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1783	1	1	KEY CAP, HALF 'NUMBER 5'	28480	5041-1783
A1S20	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1784	2		KEY CAP, HALF 'NUMBER 6'	28480	5041-1784
A1S21	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1780	8	1	KEY CAP, HALF 'NUMBER 2'	28480	5041-1780
A1S22	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1781	9	1	KEY CAP, HALF 'NUMBER 3'	28480	5041-1781
A1S23	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1787	5	1	KEY CAP, HALF 'DECIMAL POINT'	28480	5041-1787
A1S24	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1788	6	1	KEY CAP, HALF 'MINUS'	28480	5041-1788
A1S25	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1814	9	1	KEY CAP, FULL 'AMPTD'	28480	5041-1814
A1S26	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1785	3	1	KEY CAP, HALF 'NUMBER 7'	28480	5041-1785
A1S27	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1799	9	8	KEY CAP, HALF 'INCREMENT AMPTD'	28480	5041-1799
A1S28	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1782	0	1	KEY CAP, HALF 'NUMBER 4'	28480	5041-1782
A1S29	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1799	9		KEY CAP, HALF 'DECREMENT AMPTD'	28480	5041-1799
A1S30	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1779	5	1	KEY CAP, HALF 'NUMBER 1'	28480	5041-1779
A1S31	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1815	0	1	KEY CAP,SMALL DOUBLE FULL 'INCR SET'	28480	5041-1815
A1S32	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1778	4	1	KEY CAP, HALF 'NUMBER 0'	28480	5041-1778
A1S33	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1627	2	1	KEY CAP, FULL 'FM'	28480	5041-1627
A1S34	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1630	7	1	KEY CAP, DOUBLE FULL 'FREQUENCY'	28480	5041-1630
A1S35	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1799	9		KEY CAP, HALF 'INCREMENT FM'	28480	5041-1799
A1S36	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1808	1	1	KEY CAP, HALF 'COARSE TUNE'	28480	5041-1808

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1S37	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1799	9		KEY CAP, HALF 'INCREMENT FREQ'	28480	5041-1799
A1S38	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1799	9		KEY CAP, HALF 'DECREMENT FREQ'	28480	5041-1799
A1S39	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1809	2	1	KEY CAP, HALF 'FINE TUNE'	28480	5041-1809
A1S40	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1799	9		KEY CAP, HALF 'DECREMENT FM'	28480	5041-1799
A1S41	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1794	4	1	KEY CAP, HALF 'EXT'	28480	5041-1794
A1S42	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1628	3	1	KEY CAP, FULL 'AM'	28480	5041-1628
A1S43	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1810	5	1	KEY CAP, HALF 'INT 400 HZ'	28480	5041-1810
A1S44	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1799	9		KEY CAP, HALF 'INCREMENT AM'	28480	5041-1799
A1S45	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1811	6	1	KEY CAP, HALF 'INT 1 KHZ'	28480	5041-1811
A1S46	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1812	7	1	KEY CAP, HALF 'HP-IB ADRS'	28480	5041-1812
A1S47	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1797	7	1	KEY CAP, HALF 'OFF'	28480	5041-1797
A1S48	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
	5041-1799	9		KEY CAP, HALF 'DECREMENT AM'	28480	5041-1799
A1S49	3101-2302	4	1	SWITCH, TOGGLE SPDT	28480	3101-2302
	0520-0155	0	2	SCREW-MACH 2-56 .125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2190-0890	1	2	WASHER-LK HLCL NO. 2 .088-IN-ID	28480	2190-0890
	2420-0001	5	2	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
	08656-20025	5	2	STANDOFF-SWITCH	28480	08656-20025
A2	08656-60009	9	1	DISPLAY ASSEMBLY	28480	08656-60009
A2C1	0180-0100	3	5	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A2C2	0160-3879	7	20	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C9	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C11	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C12	0160-0573	2	1	CAPACITOR-FXD 4700PF +-20% 100VDC CER	28480	0160-0573
A2C13	0160-3878	6	2	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A2DS1	1990-0486	6	19	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1	19	STANDOFF-LED	28480	1400-1008
A2DS2	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS3	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS4	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS5	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS6	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS7	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS8	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS9	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS10	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS11	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS12	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS13	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS14	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS15	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS16	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS17	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008
A2DS18	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1008	1		STANDOFF-LED	28480	1400-1008

See introduction to this section for ordering information
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2DS19	1990-0486	6		LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
	1400-1000	1		STANDOFF-LED	28480	1400-1000
A2J1	1251-5343	0	1	CONNECTOR 12-PIN M POST TYPE	28480	1251-5343
A2J2	1251-5922	9	1	CONNECTOR 14-PIN M POST TYPE	28480	1251-5922
A2MP1	08656-00008	2	4	FRONT PANEL, REAR BRACKET	28480	08656-00008
	2360-0113	2	29	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A2R1	1810-0275	1	1	NETWORK, RES 1K 10-PIN-SIP .1-PIN-SPCG	01121	210A102
A2R2	1810-0206	0	1	NETWORK, RES 10K 8-PIN-SIP .1PIN-SPCG	01121	208A103
A2R3	0757-0279	0	5	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A2R4	0698-3161	9	2	RESISTOR 38.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3832-F
A2R5	0757-0443	0	1	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
A2R6	1810-0402	6	12	NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R7	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R8	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R9	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R10	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R11	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R12	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R13	0757-0797	7	1	RESISTOR 90.9 1% .5W F TC=0+-100	28480	0757-0797
A2R14	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R15	1810-0403	7	2	NETWORK-RESISTOR R1-R15: 330 OHM+-2%	01121	316A331
A2R16	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R17	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R18	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R19	0698-3446	3	5	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A2R20	0698-3441	8	12	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A2R21	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A2R22	1810-0403	7		NETWORK-RESISTOR R1-R15: 330 OHM+-2%	01121	316A331
A2R23	1810-0402	6		NETWORK, RES 330 16-PIN-DIP .1-PIN-SPCG	01121	316B331
A2R24	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A2R25	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2TP1	0360-0077	5	9	TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2TP2	0360-0077	5		TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2TP3	0360-0077	5		TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2TP4	0360-0077	5		TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2TP5	0360-0077	5		TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2TP6	0360-0077	5		TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2TP7	1251-0600	0	53	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2TP8	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2TP9	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2TP10	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2TP11	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2TP12	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2TP13	0360-0077	5		TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2TP14	0360-0077	5		TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2TP15	0360-0077	5		TERMINAL-STUD SGL-TUR SWGFRM-MTG	28480	0360-0077
A2U1	1820-2056	1	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS378N
A2U2	1820-1858	9	2	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A2U3	1820-1560	0	2	IC SHF-RGTR CMOS D-TYPE SERIAL-IN	27014	MM74C165N
A2U4	1990-0592	5	13	DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4	14	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U5	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U6	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U7	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U8	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U9	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U10	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U11	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U12	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U13	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U14	1990-0481	3	1	DISPLAY-AN-SEG 1-CHAR .400-H RED	28480	5082-7656
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U15	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U16	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859

See introduction to this section for ordering information
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2U17	1990-0592	5		DISPLAY-NUM-SEG 1-CHAR .43-H	28480	5082-7653
	1200-0859	4		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0859
A2U18	1820-1560	8		IC SHF-RGTR CMOS D-TYPE SERIAL-IN	27014	MM74C165N
A2U19	1820-1316	4	1	IC GATE CMOS 8-INP	01928	CD4048AE
A2U20	1820-0618	7	3	IC BFR TTL NON-INV HEX	01295	SN7417N
A2U21	1820-2186	8	2	IC DRVR TTL LED DRVR 7-INP	01295	SN75497N
A2U22	1820-2186	8		IC DRVR TTL LED DRVR 7-INP	01295	SN75497N
A2U23	1820-1433	6	2	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A2U24	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A2U25	1820-1216	3	4	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A2U26	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A2U27	1820-1413	2	12	IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U28	1820-1423	4	6	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A2U29	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U30	1820-2056	1		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS378N
A2U31	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U32	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U33	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U34	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U35	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U36	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U37	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U38	1820-2056	1		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS378N
A2U39	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U40	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U41	1820-1413	2		IC DCDR CMOS BCD-TO-7-SEG 4-TO-7-LINE	01928	CD4511BE
A2U42	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A3	08656-60003	3	1	LOW FREQUENCY LOOP ASSEMBLY	28480	08656-60003
A3C1	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A3C2	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A3C3	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A3C4	0160-0575	4	24	CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C5	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C6	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C7	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C8	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3C9	0160-2055	9	25	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C10	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C11	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3C12	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3C13	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C14	0160-4082	6	3	CAPACITOR-FDTHRU 1000PF 20% 200V CER (INCLUDED MOUNTING HARDWARE)	28480	0160-4082
A3C15	0160-2437	1	1	CAPACITOR-FDTHRU 5000PF +80 -20% 200V	28480	0160-2437
A3C16	0160-4370	5	1	CAPACITOR-FXD 1000PF +-5% 200VDC CER	51642	200-200-NP0-102J
A3C17	0160-4350	1	1	CAPACITOR-FXD 68PF +-5% 200VDC CER 0+-30	28480	0160-4350
A3C18	0160-4306	3	2	CAPACITOR-FXD 33PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-330J
A3C19	0160-0434	4	2	CAPACITOR-FXD 10PF +-.1PF 500VDC CER	28480	0160-0434
A3C20	0160-0708	7	1	CAPACITOR-FXD 150PF +-10% 100VDC CER	28480	0160-0708
A3C21	0160-0375	2	4	CAPACITOR-FXD 2.2PF +-.1PF 300VDC CER	28480	0160-0375
A3C22	0160-0434	4		CAPACITOR-FXD 10PF +-.1PF 500VDC CER	28480	0160-0434
A3C23	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C24	0160-3022	2	1	CAPACITOR-FXD 16PF +-1% 500VDC CER 0+-30	28480	0160-3022
A3C25	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3C26	0160-0375	2		CAPACITOR-FXD 2.2PF +-.1PF 300VDC CER	28480	0160-0375
A3C27	0160-4521	8	1	CAPACITOR-FXD 12PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-120J
A3C28	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C29	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C30	0160-3873	1		CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A3C31	0121-0440	8		CAPACITOR-V TRMR-CER 2.5-5PF 63V PC-MTG	28480	0121-0440
A3C32	0160-2236	8	1	CAPACITOR-FXD 1PF +-.25PF 500VDC CER	28480	0160-2236
A3C33	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3C34	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3C35	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C36	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C37	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3C38	0160-0154	5	3	CAPACITOR-FXD 2200PF +-10% 200VDC POLYE	28480	0160-0154
A3C39	0160-0161	4	2	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A3C40	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C41	0160-4764	1	2	CAPACITOR-FXD 150PF +-5% 100VDC CER	28480	0160-4764
A3C42	0160-0300	3	1	CAPACITOR-FXD 2700PF +-10% 200VDC POLYE	28480	0160-0300
A3C43	0170-0040	9	2	CAPACITOR-FXD .047UF +-10% 200VDC POLYE	56289	292P47392
A3C44	0160-0154	5		CAPACITOR-FXD 2200PF +-10% 200VDC POLYE	28480	0160-0154

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3C45	0160-0194	3	1	CAPACITOR-FXD .015UF +-10% 200VDC POLYE	28480	0160-0194
A3C46	0160-0161	4		CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A3C47	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A3C48	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A3C49	0160-4231	7	1	CAPACITOR-FXD 4700PF +-5% 50VDC	28480	0160-4231
A3C50	0160-0153	4	2	CAPACITOR-FXD 1000PF +-10% 200VDC POLYE	28480	0160-0153
A3C51	0160-3072	2	5	CAPACITOR-FXD 1UF +-10% 100VDC MET-POLYE	28480	0160-3072
A3C52	0160-3072	2		CAPACITOR-FXD 1UF +-10% 100VDC MET-POLYE	28480	0160-3072
A3C53	0160-3072	2		CAPACITOR-FXD 1UF +-10% 100VDC MET-POLYE	28480	0160-3072
A3C54	0160-4929	0	1	CAPACITOR-FXD .022UF +-2% 100VDC CER	56289	SCCOG223X2100C5
A3C55	0160-3916	3	1	CAPACITOR-FXD 220PF +-2% 100VDC CER	51642	200-100-NPO-221G
A3C56	0180-2104	1	1	CAPACITOR-FXD 40UF+-20% 30VDC TA	06001	69F2143G7
A3C57	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A3C58	0180-1746	5	5	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A3C59	0160-0154	5		CAPACITOR-FXD 2200PF +-10% 200VDC POLYE	28480	0160-0154
A3C60	0180-0229	7	3	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C61	0160-2453	1	2	CAPACITOR-FXD .22UF +-10% 80VDC POLYE	28480	0160-2453
A3C62	0160-2453	1		CAPACITOR-FXD .22UF +-10% 80VDC POLYE	28480	0160-2453
A3C63	0180-0291	3	10	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A3C64	0160-2208	4	1	CAPACITOR-FXD 330PF +-5% 300VDC MICA	28480	0160-2208
A3C65	0180-2216	6	1	CAPACITOR-FXD 350UF+75-10% 16VDC AL	56289	30D357G016DH2
A3C66	0160-2307	4	1	CAPACITOR-FXD 47PF +-5% 300VDC MICA	28480	0160-2307
A3C67	0160-4653	7	1	CAPACITOR-FXD .1UF +-5% 100VDC MET-POLYP	28480	0160-4653
A3C68	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A3C69	0160-3072	2		CAPACITOR-FXD 1UF +-10% 100VDC MET-POLYE	28480	0160-3072
A3C70	0160-3661	5	1	CAPACITOR-FXD .1UF +-5% 50VDC MET-POLYC	28480	0160-3661
A3C71	0160-0153	4		CAPACITOR-FXD 1000PF +-10% 200VDC POLYE	28480	0160-0153
A3C72	0160-0162	5	1	CAPACITOR-FXD .022UF +-10% 200VDC POLYE	28480	0160-0162
A3C73	0170-0040	9		CAPACITOR-FXD .047UF +-10% 200VDC POLYE	56289	292P47392
A3C74	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C75	0180-2206	4	1	CAPACITOR-FXD 60UF+-10% 6VDC TA	56289	150D606X9006B2
A3C76	0140-0196	3	2	CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300WV1CR
A3C77	0160-2259	5	1	CAPACITOR-FXD 12PF +-5% 500VDC CER 0+-30	28480	0160-2259
A3C78	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C79	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C80	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C81	0160-3072	2		CAPACITOR-FXD 1UF +-10% 100VDC MET-POLYE	28480	0160-3072
A3C82	0160-0570	9	2	CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A3C83	0180-0094	4	2	CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
A3C84	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C85	0140-0196	3		CAPACITOR-FXD 150PF +-5% 300VDC MICA	72136	DM15F151J0300WV1CR
A3C86	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A3C87	0160-0574	3	3	CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-0574
A3C88	0140-0205	5	1	CAPACITOR-FXD 62PF +-5% 300VDC MICA	72136	DM15E620J0300WV1CR
A3C89	0160-4307	4	1	CAPACITOR-FXD 47PF +-5% 200VDC CER 0+-30	28480	0160-4307
A3C90	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C91	0180-0094	4		CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
A3C92	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C93	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C94	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C95	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A3C96	0160-4385	2	1	CAPACITOR-FXD 15PF +-5% 200VDC CER 0+-30	51642	200-200-NPO-150J
A3C97	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A3CR1	0122-0065	7	6	DIODE-VVC 29PF 3%	28480	0122-0065
A3CR2	1901-0179	7	6	DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A3CR3	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A3CR4	1901-0050	3	56	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR9	1901-0586	0	3	DIODE-GEN PRP 30V 25MA TO-72	28480	1901-0586
A3CR10	1901-0586	0		DIODE-GEN PRP 30V 25MA TO-72	28480	1901-0586
A3CR11	1901-0586	0		DIODE-GEN PRP 30V 25MA TO-72	28480	1901-0586
A3CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR14	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR15	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR16	1901-0527	9	1	DIODE-CUR RGLTR 75V DO-7	28480	1901-0527
A3CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR18	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR20	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR21	1901-0539	3	2	DIODE-SM SIG SCHOTTKY	28480	1901-0539
A3CR22	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A3CR23	1901-0535	9	4	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A3CR24	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A3CR25	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3CR26	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A3CR27	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A3CR28	1901-0376	6	3	DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A3CR29	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A3CR30	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR31	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR32	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR33	0122-0065	7		DIODE-VVC 29PF 3%	28480	0122-0065
A3CR34	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A3CR35	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3E1	9170-0847	3	1	CORE-SHIELDING BEAD	02114	56-590-65/3B PARYLENE COATED
A3E2	9170-0029	3	1	CORE-SHIELDING BEAD	28480	9170-0029
A3J1	1251-5560	9	2	CONNECTOR 8-PIN M POST TYPE	28480	1251-5560
A3J2	1200-0507	9	11	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A3J3	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A3J4	1250-1626	0	4	CONNECTOR-RF SMC M PC 50-OHM	28480	1250-1626
	3050-0079	3	2	WASHER-FL NM NO. 2 .094-IN-ID .188-IN-OD	28480	3050-0079
A3J5	1250-1626	0		CONNECTOR-RF SMC M PC 50-OHM	28480	1250-1626
	3050-0079	3		WASHER-FL NM NO. 2 .094-IN-ID .188-IN-OD	28480	3050-0079
A3L1	9100-1618	1	8	INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1618
A3L2	9100-1618	1		INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1618
A3L3	9100-1618	1		INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1618
A3L4	9140-0144	0	5	INDUCTOR RF-CH-MLD 4.7UH 10% .105DX.26LG	28480	9140-0144
A3L5				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L6				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L7				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L8				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L9				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L10				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L11				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L12				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L13				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L14				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L15	9135-0073	3	5	INDUCTOR RF-CH-MLD 51NH 5% .102DX.26LG	28480	9135-0073
A3L16	9135-0071	1	2	INDUCTOR RF-CH-MLD 62NH 5% .102DX.26LG	28480	9135-0071
A3L17	9100-3360	2	1	INDUCTOR RF-CH-MLD 680NH 5% .2DX.385LG	28480	9100-3360
A3L18	9140-0112	2	2	INDUCTOR RF-CH-MLD 4.7UH 10%	28480	9140-0112
A3L19	9100-2247	4	20	INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A3L20	9140-0112	2		INDUCTOR RF-CH-MLD 4.7UH 10%	28480	9140-0112
A3L21	9140-0144	0		INDUCTOR RF-CH-MLD 4.7UH 10% .105DX.26LG	28480	9140-0144
A3L22	9140-0141	7	4	INDUCTOR RF-CH-MLD 680NH 10% .105DX.26LG	28480	9140-0141
A3L23†				NOT ASSIGNED		
A3L24				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A3L25	9140-0141	7		INDUCTOR RF-CH-MLD 680NH 10% .105DX.26LG	28480	9140-0141
A3MP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3MP2	1400-0966	8	17	CLIP-HINGE	91506	6015-13AT
A3MP3	2190-0007	0	3	WASHER-LK HLCL NO. 8 .168-IN-ID	28480	2190-0007
A3MP4	2360-0113	2		SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A3MP5	2580-0002	4	1	NUT-HEX-DBL-CHAM 8-32-THD .085-IN-THK	00000	ORDER BY DESCRIPTION
A3MP6	3050-0063	5	2	WASHER-FL MTLC NO. 8 .172-IN-ID	28480	3050-0063
A3MP7	3050-0121	6	1	WASHER-FL MTLC NO. 6 .144-IN-ID	28480	3050-0121
A3MP8	4208-0277	9	1	FOAM, BOTTOM, 60/110MHZ SECTION	28480	4208-0277
A3MP9	9220-3065	0	1	FOAM, TOP, 60/110MHZ SECTION	28480	9220-3065
A3MP10	7120-0055	2	1	LABEL, INFO (50MHZ LEVEL)	28480	7120-0055
A3MP11	7120-0056	3	1	LABEL, INFO (60-110MHZ FLATNESS)	28480	7120-0056
A3MP12	08656-00029	7	1	BOTTOM COVER, 60/110MHZ SECTION	28480	08656-00029
A3MP13	08656-00030	0	1	TOP COVER, 60/110MHZ SECTION	28480	08656-00030
A3MP14	08656-00031	1	1	BOTTOM COVER, 50MHZ SECTION	28480	08656-00031
A3MP15	08656-00032	2	1	TOP COVER, 50MHZ SECTION	28480	08656-00032
A3MP16	08656-00041	3	2	CLIP-CAPACITOR GROUND	28480	08656-00041
A3MP17	08656-00044	6	1	SHIELD, FENCE	28480	08656-00044
A3Q1	1855-0280	2	1	TRANSISTOR J-FET N-CHAN D-MODE TO-92 SI	17856	E107
A3Q2	1855-0414	4	2	TRANSISTOR J-FET 2N4393 N-CHAN D-MODE	04713	2N4393
A3Q3	1854-0071	7	4	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A3Q4	1855-0288	0	1	TRANSISTOR J-FET 2N5556 N-CHAN D-MODE	17856	2N5556
A3Q5	1854-0610	0	1	TRANSISTOR NPN SI TO-46 FT=800MHZ	28480	1854-0610
A3Q6	1854-0345	8	2	TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	04713	2N5179
A3Q7	1854-0696	2	6	TRANSISTOR NPN SI TO-72 PD=200MW	28480	1854-0696
A3Q8	1854-0696	2		TRANSISTOR NPN SI TO-72 PD=200MW	28480	1854-0696
A3Q9	1854-0247	9	3	TRANSISTOR NPN SI TO-39 PD=1W FT=800MHZ	28480	1854-0247
A3Q10	1853-0010	0	1	TRANSISTOR PNP SI TO-72 PD=200MW FT=1GHZ	28480	1853-0010
A3Q11	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
A3Q12	1854-0345	8		TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	04713	2N5179
A3Q13	1855-0414	4		TRANSISTOR J-FET 2N4393 N-CHAN D-MODE	04713	2N4393

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R1	0698-3151	7	5	RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A3R2	0698-3444	1	12	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A3R3	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A3R4	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A3R5	0698-3431	6	1	RESISTOR 23.7 1% .125W F TC=0+-100	03888	PME55-1/8-T0-23R7-F
A3R6	0698-3156	2	14	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R7	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A3R8	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R9	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R10	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A3R11	0757-0441	8	3	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A3R12	0757-0416	7	5	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3R13	0757-0180	2	2	RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A3R14	0757-0405	4	5	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
A3R15	0698-7199	1	5	RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-28R7-G
A3R16	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-28R7-G
A3R17	0698-3443	0	2	RESISTOR 287 1% .125W F TC=0+-100	24546	C4-1/8-T0-287R-F
A3R18	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-28R7-G
A3R19	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-28R7-G
A3R20	0757-0418	9	6	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A3R21	0757-0400	9		RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A3R22	0757-0159	5	1	RESISTOR 1K 1% .5W F TC=0+-100	28480	0757-0159
A3R23	1810-0203	5	2	NETWORK-RES 8-SIP470.0 OHM X 7	01121	208A471
A3R24	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R25	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R26	1810-0215	9	2	NETWORK-RES 8-SIP75.0K OHM X 7	01121	208A753
A3R27	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A3R28	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R29	0757-0405	4		RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
A3R30	0757-0422	5	2	RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A3R31	0757-0402	1	6	RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
A3R32	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A3R33	0698-8789	7	1	RESISTOR 866 .25% .125W F TC=0+-50	28480	0698-8789
A3R34	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A3R35	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A3R36	0757-1094	9	7	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A3R37	0757-0461	2	7	RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A3R38	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A3R39	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A3R40	1810-0215	9		NETWORK-RES 8-SIP75.0K OHM X 7	01121	208A753
A3R41	0757-0382	6	3	RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
A3R42	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A3R43	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R44	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A3R45	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R46	0698-3155	1	8	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R47	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R48	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R49	0683-1065	5	2	RESISTOR 10M 5% .25W FC TC=-900/+1200	01121	CB1065
A3R50	0698-3160	8	3	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A3R51	0757-0461	2		RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A3R52	0683-1065	5		RESISTOR 10M 5% .25W FC TC=-900/+1200	01121	CB1065
A3R53	0757-0402	1		RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
A3R54	0698-3160	8		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A3R55	0757-0402	1		RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
A3R56	0699-0264	9	1	RESISTOR-MATCHED SET 5.0M & 50K OHMS	28480	0699-0264
A3R57	2100-0569	2	1	RESISTOR-TRMR 1M 20% C TOP-ADJ 1-TRN	28480	2100-0569
A3R58	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A3R59	0699-0264	9		PART OF R56 (5.0M)	28480	0699-0264
A3R60	0757-0382	6		RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
A3R61	0757-0424	7	9	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A3R62	0757-0439	4	2	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A3R63	0698-7188	8	2	RESISTOR 10 1% .05W F TC=0+-100	24546	C3-1/8-T00-10R-G
A3R64	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A3R65	0757-0382	6		RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
A3R66	0757-0461	2		RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A3R67	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R68	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A3R69	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R70	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R71	0757-0461	2		RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A3R72	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A3R73	0698-3153	9	10	RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A3R74	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R75	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R76	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R77	0757-0290	5	2	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A3R78	0757-0397	3		RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
A3R79	0687-5661	5	1	RESISTOR 56M 10% .5W CC TC=0+1059	01121	EB5661
A3R80	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R81	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R82	0757-0458	7	2	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A3R83	0757-0461	2		RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A3R84	0683-5655	9	2	RESISTOR 5.6M 5% .25W FC TC=-900/+1100	01121	CB5655
A3R85	0698-3157	3	5	RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A3R86	0698-6866	7	1	RESISTOR 2.182K .25% .125W F TC=0+-50	28480	0698-6866
A3R87	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A3R88	0698-3150	6	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A3R89	0698-0084	9	8	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A3R90	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-T0-619R-F
A3R91	0757-0123	3	1	RESISTOR 34.8K 1% .125W F TC=0+-100	28480	0757-0123
A3R92	0683-5655	9		RESISTOR 5.6M 5% .25W FC TC=-900/+1100	01121	CB5655
A3R93	0683-2265	1	1	RESISTOR 22M 5% .25W FC TC=-900/+1200	01121	CB2265
A3R94	0757-0398	4	5	RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A3R95	0757-0402	1		RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
A3R96	0757-0402	1		RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
A3R97	0757-0402	1		RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
A3R98	0698-3429	2	1	RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
A3R99	1810-0203	5		NETWORK-RES 8-SIP470.0 OHM X 7	01121	208A471
A3R100	0698-3457	6	6	RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A3R101	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A3R102	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A3R103	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A3R104	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R105	0698-3437	2	1	RESISTOR 133 1% .125W F TC=0+-100	24546	C4-1/8-T0-133R-F
A3R106	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A3R107	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R108	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A3R109	0757-0465	6	9	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A3R110	2100-3659	7	1	RESISTOR-TRMR 20K 10% C TOP-ADJ 17-TRN	32997	3292W-1-203
A3R111	0698-7199	1		RESISTOR 28.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-28R7-G
A3R112	0698-3445	2	4	RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-348R-F
A3R113	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A3R114	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A3R115	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A3R116	0757-0405	4		RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
A3R117	0698-0082	7	4	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A3R118†	0757-0397	3	3	RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
A3R119	0757-0461	2		RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A3TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3TP3	1251-1556	7	56	CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3TP4	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3TP5	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3TP6	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3TP7	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3TP8	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3TP9	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3TP10	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A3U1	1826-0100	8	1	IC CONV 8-B-D/A 16-DIP-C PKG	04713	MC1408L-8
A3U2	1820-1722	6	1	IC RGTR CMOS 8-BIT	04713	MC14559BCP
A3U3	1858-0066	8	3	TRANSISTOR ARRAY 16-PIN CER DIP	32293	IH401A
A3U4	1820-1272	1	1	IC BFR TTL LS NOR QUAD 2-INP	01295	SN74LS33N
A3U5	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A3U6	1826-0522	4	3	IC OP AMP QUAD 14-DIP-P PKG	01295	TL074CN
A3U7	1858-0066	8		TRANSISTOR ARRAY 16-PIN CER DIP	32293	IH401A
A3U8	1826-0522	4		IC OP AMP QUAD 14-DIP-P PKG	01295	TL074CN
A3U9	1826-0174	2	2	IC COMPARATOR GP QUAD 14-DIP-P PKG	28480	1826-0174
A3U10	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A3U11	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U12	1826-0522	4		IC OP AMP QUAD 14-DIP-P PKG	01295	TL074CN
A3U13	1820-1211	8	2	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A3U14	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U15	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U16	1826-0174	2		IC COMPARATOR GP QUAD 14-DIP-P PKG	28480	1826-0174
A3U17	1820-1112	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U18	1858-0066	8		TRANSISTOR ARRAY 16-PIN CER DIP	32293	IH401A
A3U19	1820-1802	9	1	IC GATE ECL EXCL-OR QUAD	04713	MC10113L
A3U20	1820-2005	0	1	IC TIMER NMOS	0003J	UPD8253D

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U21	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U22	1826-0547	3	1	IC OP AMP DUAL 8-DIP-P PKG	01295	TL072ACP
A3U23	1820-1788	4	1	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A3U24	1820-2008	3	2	IC SHF-RGTR CMOS D-M/S SERIAL-IN PRL-OUT	04713	MC14015BCP
A3U25	1820-2008	3		IC SHF-RGTR CMOS D-M/S SERIAL-IN PRL-OUT	04713	MC14015BCP
A3U26	1820-1225	4	1	IC FF ECL D-M/S DUAL	04713	MC10231P
A3U27	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A3U28	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U29	1820-1383	5	2	IC CNTR ECL BCD POS-EDGE-TRIG	04713	MC10138L
A3U30	1820-0802	1	1	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A3U31	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U32	1820-1383	5		IC CNTR ECL BCD POS-EDGE-TRIG	04713	MC10138L
A3VR1	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
A3VR2	1902-0033	4	1	DIODE-ZNR 1N823 6.2V 5% DO-7 PD=.4W	24046	1N823
A3VR3	1902-0064	1	2	DIODE-ZNR 7.5V 5% DO-35 PD=.4W TC=+.05%	28480	1902-0064
A3VR4	1902-3139	7	4	DIODE-ZNR 8.25V 5% DO-35 PD=.4W	28480	1902-3139
A3VR5	1902-3139	7		DIODE-ZNR 8.25V 5% DO-35 PD=.4W	28480	1902-3139
A3VR6	1902-0041	4	1	DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A3VR7	1902-3139	7		DIODE-ZNR 8.25V 5% DO-35 PD=.4W	28480	1902-3139
A3Y1	0410-1130	8	1	CRYSTAL	28480	0410-1130
	1200-0758	2	1	SOCKET-XTAL 2-CONT HC-25/U DIP-SLDR	28480	1200-0758
A4	08656-60001	1	1	HIGH FREQUENCY LOOP ASSEMBLY	28480	08656-60001
A4C1	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A4C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C3	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A4C4	0160-4389	6	6	CAPACITOR-FXD 100PF +-5PF 200VDC CER	51642	200-200-NPO-101J
A4C5	0160-4082	6		CAPACITOR-FDTHRU 1000PF 20% 200V CER	28480	0160-4082
A4C6	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A4C7	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A4C8	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A4C9	0160-3560	1	6	CAPACITOR-FXD 2.7PF +-5% 200VDC CER	51642	100-100-NPO-279J
A4C10	0160-3560	1		CAPACITOR-FXD 2.7PF +-5% 200VDC CER	51642	100-100-NPO-279J
A4C11	0160-3560	1		CAPACITOR-FXD 2.7PF +-5% 200VDC CER	51642	100-100-NPO-279J
A4C12	0160-4764	1		CAPACITOR-FXD 150PF +-5% 100VDC CER	28480	0160-4764
A4C13	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A4C14	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A4C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C16	0160-3456	6	5	CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A4C17	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A4C18	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A4C19	0160-4389	6		CAPACITOR-FXD 100PF +-5PF 200VDC CER	51642	200-200-NPO-101J
A4C20	0160-4103	2	1	CAPACITOR-FXD 220PF +-5% 100VDC CER	72982	0121-N100-COG-221J
A4C21	0160-4498	8	4	CAPACITOR-FXD 5.6PF +-.5PF 200VDC CER	51642	200-200-NPO-569D
A4C22*	0160-3873	1	7	CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A4C23	0160-4498	8		CAPACITOR-FXD 5.6PF +-.5PF 200VDC CER	51642	200-200-NPO-569D
A4C24	0160-4510	3	3	CAPACITOR-FXD 3.9PF +-.5PF 200VDC CER	51642	200-200-NPO-399D
A4C25	0160-4389	6		CAPACITOR-FXD 100PF +-5PF 200VDC CER	51642	200-200-NPO-101J
A4C26	0160-4389	6		CAPACITOR-FXD 100PF +-5PF 200VDC CER	51642	200-200-NPO-101J
A4C27				NOT ASSIGNED		
A4C28	0160-3875	3	4	CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A4C29	0160-3873	1		CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A4C30	0160-3560	1		CAPACITOR-FXD 2.7PF +-5% 200VDC CER	51642	100-100-NPO-279J
A4C31	0160-3876	4	4	CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A4C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C33	0160-3029	9	3	CAPACITOR-FXD 7.5PF +-.5PF 100VDC CER	28480	0160-3029
A4C34†	0180-0197	8	9	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A4C35	0160-3029	9		CAPACITOR-FXD 7.5PF +-.5PF 100VDC CER	28480	0160-3029
A4C36	0160-4383	8	3	CAPACITOR-FXD 6.8PF +-.5PF 200VDC CER	28932	5024E0200RD689D
A4C37	0160-3029	9		CAPACITOR-FXD 7.5PF +-.5PF 100VDC CER	28480	0160-3029
A4C38	0160-4491	1	3	CAPACITOR-FXD 8.2PF +-5% 200VDC CER	51642	200-200-NPO-829J
A4C39	0160-2257	3	1	CAPACITOR-FXD 10PF +-5% 500VDC CER 0+-60	28480	0160-2257
A4C40				NOT ASSIGNED		
A4C41	0160-4491	1		CAPACITOR-FXD 8.2PF +-5% 200VDC CER	51642	200-200-NPO-829J
A4C42	0160-3875	3		CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A4C43	0160-3873	1		CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A4C44	0160-3926	5	1	CAPACITOR-FDTHRU 100PF 20% 200V CER	28480	0160-3926
A4C45	0160-3875	3		CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A4C46				NOT ASSIGNED		
A4C47	0160-3454	4	1	CAPACITOR-FXD 220PF +-10% 1KVDC CER	28480	0160-3454
A4C48	0160-3459	9	1	CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3459
A4C49	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A4C50	0160-4494	4	2	CAPACITOR-FXD 39PF +-5% 200VDC CER 0+-30	51642	200-200-NPO-390J

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4C51	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C52				NOT ASSIGNED		
A4C53	0121-0449	9	3	CAPACITOR-V TRMR-CER 3.5-10PF 63V PC-MTG	28480	0121-0449
A4C54				NOT ASSIGNED		
A4C55				NOT ASSIGNED		
A4C56				NOT ASSIGNED		
A4C57				NOT ASSIGNED		
A4C58				NOT ASSIGNED		
A4C59	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A4C60	0160-3070	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3070
A4C61	0160-3075	3		CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3075
A4C62	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A4C63	0160-3070	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3070
A4C64	0160-4767	4	1	CAPACITOR-FXD 20PF +-5% 200VDC CER 0+-30	28480	0160-4767
A4C65	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A4C66	0160-3070	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3070
A4C67	0160-4497	7	1	CAPACITOR-FXD 82PF +-5% 200VDC CER 0+-30	28480	0160-4497
A4C68	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C69	0160-3070	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3070
A4C70	0160-2204	0	1	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A4C71	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C72	0160-3070	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3070
A4C73†	0160-0155	6	1	CAPACITOR-FXD 3300PF +-10% 200VDC POLYE	28480	0160-0155
A4C74	0160-3453	3	3	CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0160-3453
A4C75	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C76	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C77†	0160-2210	6	1	CAPACITOR-FXD 1000PF +-5% 300VDC MICA	28480	0160-2210
A4C78	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C79	0160-3076	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3076
A4C80	0160-3074	2	2	CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3074
A4C81	0160-4382	9		CAPACITOR-FXD 3.3PF +-.25PF 200VDC CER	51642	200-200-NPO-339C
A4C82				NOT ASSIGNED		
A4C83	0160-3079	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3079
A4C84	0160-3074	2		CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3074
A4C85	0121-0449	9		CAPACITOR-V TRMR-CER 3.5-10PF 63V PC-MTG	28480	0121-0449
A4C86	0160-3560	1		CAPACITOR-FXD 2.7PF +-5% 200VDC CER	51642	100-100-NPO-279J
A4CR1	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR2	1901-0109	9	1	DIODE-STEP RECOVERY	28480	1901-0109
A4CR3	1906-0090	9	4	DIODE-MATCHED 1V	28480	1906-0090
A4CR4	1906-0090	9		DIODE-MATCHED 1V	28480	1906-0090
A4CR5	1906-0090	9		DIODE-MATCHED 1V	28480	1906-0090
A4CR6	1906-0090	9		DIODE-MATCHED 1V	28480	1906-0090
A4CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR14				NOT ASSIGNED		
A4CR15				NOT ASSIGNED		
A4CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR18	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A4J1	1251-6731	0	1	CONNECTOR	28480	1251-6731
A4L1	9100-1627	2	4	INDUCTOR RF-CH-MLD 39UH 5% .166DX.385LG	28480	9100-1627
A4L2	9100-1627	2		INDUCTOR RF-CH-MLD 39UH 5% .166DX.385LG	28480	9100-1627
A4L3	9100-1627	2		INDUCTOR RF-CH-MLD 39UH 5% .166DX.385LG	28480	9100-1627
A4L4	9100-1627	2		INDUCTOR RF-CH-MLD 39UH 5% .166DX.385LG	28480	9100-1627
A4L5	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A4L6				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L7				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L8				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L9				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L10	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A4L11	9135-0071	1		INDUCTOR RF-CH-MLD 62NH 5% .102DX.26LG	28480	9135-0071
A4L12				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L13	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A4L14				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L15	9135-0073	3		INDUCTOR RF-CH-MLD 51NH 6% .102DX.26LG	28480	9135-0073
A4L16	9135-0073	3		INDUCTOR RF-CH-MLD 51NH 6% .102DX.26LG	28480	9135-0073
A4L17				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L18				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L19	9135-0076	6	2	INDUCTOR RF-CH-MLD 39NH 6% .102DX.26LG	28480	9135-0076
A4L20	9135-0074	4	1	INDUCTOR RF-CH-MLD 47NH 4% .102DX.26LG	28480	9135-0074

See introduction to this section for ordering information
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4L21	9135-0081	3	3	INDUCTOR RF-CH-MLD 68NH 5% .102DX.26LG	28480	9135-0081
A4L22	9135-0081	3		INDUCTOR RF-CH-MLD 68NH 5% .102DX.26LG	28480	9135-0081
A4L23	9140-0158	6	20	INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0158
A4L24	9140-0158	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0158
A4L25				NOT ASSIGNED		
A4L26	9135-0081	3		INDUCTOR RF-CH-MLD 68NH 5% .102DX.26LG	28480	9135-0081
A4L27	9135-0076	6		INDUCTOR RF-CH-MLD 39NH 6% .102DX.26LG	28480	9135-0076
A4L28	9100-3512	0	2	INDUCTOR-50NH .285D X .4LG	28480	9100-3512
A4L29				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A4L30	9100-2248	5	2	INDUCTOR RF-CH-MLD 120NH 10% .105DX.26LG	28480	9100-2248
A4L31	9140-0141	7		INDUCTOR RF-CH-MLD 680NH 10% .105DX.26LG	28480	9140-0141
A4L32				NOT ASSIGNED		
A4L33	9100-2249	6	2	INDUCTOR RF-CH-MLD 150NH 10% .105DX.26LG	28480	9100-2249
A4L34	9100-1641	0	1	INDUCTOR RF-CH-MLD 240UH 5% .166DX.385LG	28480	9100-1641
A4L35	9135-0060	6	2	INDUCTOR RF-CH-MLD 33NH 6% .102DX.26LG	28480	9135-0060
A4L36	9100-3514	0	2	INDUCTOR-30NH .285D X .4LG	28480	9100-3514
A4L37	9100-3512	0		INDUCTOR-50NH .285D X .4LG	28480	9100-3512
A4L38	9100-3514	0		INDUCTOR-30NH .285D X .4LG	28480	9100-3514
A4L39	9100-3513	9	1	INDUCTOR-75NH .285D X .4LG	28480	9100-3513
A4L40	9135-0060	6		INDUCTOR RF-CH-MLD 33NH 6% .102DX.26LG	28480	9135-0060
A4L41	9100-2249	6		INDUCTOR RF-CH-MLD 150NH 10% .105DX.26LG	28480	9100-2249
A4MP1	0362-0227	1	1	CONNECTOR-SGL CONT SKT 1.14-MM-BSC-SZ	28480	0362-0227
A4MP2	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A4MP3	8150-0460	1		WIRE 24AWG W/BK/O 300V PVC 7X32 80C	28480	8150-0460
A4MP4	08656-00033	3	35	GROUND CLIP-SEMI-RIGID	28480	08656-00033
A4MP5†	08656-00009	9	1	BRACKET-HF LOOP FEEDTHRU	28480	08656-00009
A4MP6	08656-00074	2	1	PLATE-HF LOOP BRACKET	28480	08656-00074
A4MP7†				NOT ASSIGNED		
A4MP8	2420-0026	4	2	NUT	00000	ORDER BY DESCRIPTION
A4MP9	2190-0630	7	2	WASHER-LOCK	28480	2190-0630
A4MP10	8150-0449	8	1	WIRE-AWG,RED	28480	8150-0449
A4MP11	8150-0460	3		WIRE-AWG,WHITE ORANGE	28480	8150-0460
A4MP12†	08656-00090	2	1	GROUNDING SPRING	28480	08656-00090
A4Q1	1853-0020	4	4	TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A4Q2	1854-0632	6	8	TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-91
A4Q3	1854-0696	2		TRANSISTOR NPN SI TO-72 PD=200MW	28480	1854-0696
A4Q4	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A4Q5	1854-0477	7	2	TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A4Q6	1855-0235	7	1	TRANSISTOR J-FET N-CHAN D-MODE TO-52 SI	28480	1855-0235
A4Q7	1853-0007	7	8	TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A4Q8	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A4Q9	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A4Q10	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A4R1	0698-7227	6	4	RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-T0-422R-G
A4R2	0698-7189	9	2	RESISTOR 11 1% .05W F TC=0+-100	24546	C3-1/8-T00-11R0-G
A4R3	0698-7227	6		RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-T0-422R-G
A4R4	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A4R5	0757-0440	7	2	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A4R6*	0698-7210	5	2	RESISTOR 170 1% .05W F TC=0+-100	24546	C3-1/8-T0-170R-G
A4R7*	0698-7200	5	1	RESISTOR 31.6 1% .05W F TC=0+-100	24546	C3-1/8-T00-31R6-G
A4R8	0698-3430	3	5	RESISTOR 147 1% .125W F TC=0+-100	24546	C4-1/8-T0-147R-F
A4R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R10*	0698-7210	5		RESISTOR 170 1% .05W F TC=0+-100	24546	C3-1/8-T0-170R-G
A4R11	0698-3440	7	7	RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A4R12	0698-3440	7		RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A4R13	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A4R14	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A4R15	0757-0179	9	1	RESISTOR 196 1% .25W F TC=0+-100	24546	C5-1/4-T0-196R-F
A4R16	0698-7220	9	1	RESISTOR 215 1% .05W F TC=0+-100	24546	C3-1/8-T0-215R-G
A4R17	0698-7198	8	4	RESISTOR 26.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-26R1-G
A4R18	0698-7198	8		RESISTOR 26.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-26R1-G
A4R19	0698-7205	0	6	RESISTOR 51.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-51R1-G
A4R20	0698-7236	7	2	RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-G
A4R21†	0757-0280	3	20	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R22	0698-3430	3		RESISTOR 147 1% .125W F TC=0+-100	24546	C4-1/8-T0-147R-F
A4R23	0698-7205	0		RESISTOR 51.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-51R1-G
A4R24	0757-0394	0	3	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A4R25	0757-0346	2	5	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A4R26	0698-3440	7		RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A4R27	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A4R28	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A4R29	0698-3132	4	3	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A4R30	0698-3447	4	3	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R31	0698-3132	4		RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A4R32	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A4R33	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A4R34				NOT ASSIGNED		
A4R35	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R36	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A4R37	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A4R38	0698-7100	8		RESISTOR 10 1% .05W F TC=0+-100	24546	C3-1/8-T00-10R-G
A4R39	0698-8816	1	1	RESISTOR 2.15 1% .125W F TC=0+-100	28480	0698-8816
A4R40	0698-7221	0	5	RESISTOR 237 1% .05W F TC=0+-100	24546	C3-1/8-T0-237R-G
A4R41	0698-7221	0		RESISTOR 237 1% .05W F TC=0+-100	24546	C3-1/8-T0-237R-G
A4R42	0698-7221	0		RESISTOR 237 1% .05W F TC=0+-100	24546	C3-1/8-T0-237R-G
A4R43	0698-7221	0		RESISTOR 237 1% .05W F TC=0+-100	24546	C3-1/8-T0-237R-G
A4R44	0698-7221	0		RESISTOR 237 1% .05W F TC=0+-100	24546	C3-1/8-T0-237R-G
A4R45	0698-3442	9		RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A4R46	0698-3442	9		RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A4R47	0698-3442	9		RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A4R48	0698-3442	9		RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A4R49	0698-3442	9		RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A4R50	1810-0269	3	1	NETWORK-RES 9-SIP10.0K OHM X 8	28480	1810-0269
A4R51	0698-3150	4	2	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A4R52	2100-2216	0	1	RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	73138	82PR5K
A4R53	0698-3150	4		RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A4R54	0757-0438	3	3	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A4R55	2100-2030	6	1	RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	73138	82PR20K
A4R56	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A4R57	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A4R58	0698-3454	3	4	RESISTOR 215K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2153-F
A4R59	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R60	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A4R61				NOT ASSIGNED		
A4R62	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A4R63	0698-3154	0	4	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A4R64	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R65	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A4R66	0698-3266	5	1	RESISTOR 237K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2373-F
A4R67	0698-3438	3		RESISTOR 147 1% .125W F TC=0+-100	24546	C4-1/8-T0-147R-F
A4R68	0698-3445	2		RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-348R-F
A4R69	0698-3454	3		RESISTOR 215K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2153-F
A4R70	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A4R71†	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R72	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A4R73	0698-3452	1	2	RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
A4R74	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A4R75	0698-3452	1		RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
A4T1	00552-6024	9	1	TRANSFORMER-RF, YELLOW	28480	00552-6024
A4TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4TP2	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A4TP3	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A4TP4	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A4TP5	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A4TP6	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	12' 1-1556
A4TP7	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4TP8	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A4TP9	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A4TP10	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4TP11	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4TP12	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4TP13	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4TP14	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4TP15	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4TP16	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A4U1	0955-0146	0	1	MIXER-DOUBLE BALANCED, 1000 MHZ	28480	0955-0146
	0890-0714	2		SOLDER WIRE 354-DEG-F 2.4%-RMA	28480	0890-0714
A4U2	1820-1976	2	2	IC BFR CMOS NON-INV HEX	01928	CD4050BE
A4U3	1820-0618	7		IC BFR TTL NON-INV HEX	01295	SN7417N
A4U4	1820-1662	3	2	IC SHF-RGTR CMOS SERIAL-IN PRL-OUT 8-BIT	01928	CD4094BE
A4U5	1826-0323	3	2	IC OP AMP GP QUAD 14-DIP-C PKG	28480	1826-0323
A4U6	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A5	08656-60013	5	1	HIGH FREQUENCY OSCILLATOR ASSEMBLY	28480	08656-60013
A5C1	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C2	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A5C3	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C5	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5C6	0160-4309	6		CAPACITOR-FXD 100PF +-5PF 200VDC CER	51642	200-200-NP0-101J
A5C7	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C8	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C9	0160-3560	1		CAPACITOR-FXD 2.7PF +-5% 200VDC CER	51642	100-100-NP0-279J
A5C10	0160-4309	6		CAPACITOR-FXD 100PF +-5PF 200VDC CER	51642	200-200-NP0-101J
A5C11	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C12	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C13	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C14	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C15	0160-4386	3		CAPACITOR-FXD 33PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-330J
A5C16	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C17	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C18	0160-4494	4		CAPACITOR-FXD 39PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-390J
A5C19	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A5C20	0160-4498	8		CAPACITOR-FXD 5.6PF +-.5PF 200VDC CER	51642	200-200-NP0-569D
A5C21	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A5C22*	0160-0690	4	2	CAPACITOR-FXD 1PF +-.5PF 100VDC CER	28480	0160-0690
A5CR1	0122-0072	6	2	DIODE-VVC 2.2PF 5% C3/C25-MIN=4.5	04713	BB105B
A5CR2	0122-0072	6		DIODE-VVC 2.2PF 5% C3/C25-MIN=4.5	04713	BB105B
A5L1				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A5L2				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A5L3	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5L4				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A5L5	9140-0158	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0158
A5L6	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5L7	9140-0144	0		INDUCTOR RF-CH-MLD 4.7UH 10% .105DX.26LG	28480	9140-0144
A5L8				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A5L9	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5L10	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5L11				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A5L12	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5MP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A5MP2	8151-0014	5		WIRE 24AWG 1X24	28480	8151-0014
A5Q1	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A5Q2	1854-0632	6		TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-91
A5Q3	1854-0632	6		TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-91
A5R1	0698-3445	2		RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-348R-F
A5R2	0698-7222	1	1	RESISTOR 261 1% .05W F TC=0+-100	24546	C3-1/8-T0-261R-G
A5R3	0698-7225	4	1	RESISTOR 348 1% .05W F TC=0+-100	24546	C3-1/8-T0-348R-G
A5R4	0698-7202	7	2	RESISTOR 38.3 1% .05W F TC=0+-100	24546	C3-1/8-T00-38R3-G
A5R5	0698-7216	3	3	RESISTOR 147 1% .05W F TC=0+-100	24546	C3-1/8-T0-147R-G
A5R6	0757-0405	4		RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
A5R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R8	0698-3438	3		RESISTOR 147 1% .125W F TC=0+-100	24546	C4-1/8-T0-147R-F
A5R9	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A5R10	0698-7198	0		RESISTOR 26.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-26R1-G
A5R11	0698-7198	0		RESISTOR 26.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-26R1-G
A5R12	0698-7227	6		RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-T0-422R-G
A5R13	0698-7189	9		RESISTOR 11 1% .05W F TC=0+-100	24546	C3-1/8-T00-11R0-G
A5R14	0698-7227	6		RESISTOR 422 1% .05W F TC=0+-100	24546	C3-1/8-T0-422R-G
A5R15	0698-7212	9	1	RESISTOR 100 1% .05W F TC=0+-100	24546	C3-1/8-T0-100R-G
A5R16	0698-7216	3		RESISTOR 147 1% .05W F TC=0+-100	24546	C3-1/8-T0-147R-G
A5R17	0698-7202	7		RESISTOR 38.3 1% .05W F TC=0+-100	24546	C3-1/8-T00-38R3-G
A5R18	0757-0442	9	15	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R19	0698-7216	3		RESISTOR 147 1% .05W F TC=0+-100	24546	C3-1/8-T0-147R-G
A5R20	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A5R21	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A5R22	0698-7205	0		RESISTOR 51.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-51R1-G
A5R23	0698-7236	7		RESISTOR 1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1001-G
A5TP1	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A5TP2	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A5TP3	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A5TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A5TP5	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A6	08656-60002	2	1	OUTPUT ASSEMBLY	28480	08656-60002
A6C1	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C2	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C3	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C4	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A6C5	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6C6	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A6C7	0160-0576	5	2	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A6C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C9	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A6C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C11	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C12	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C13	0160-3877	5	5	CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A6C14	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A6C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C16	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A6C17	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C18†	0160-4519	4	1	CAPACITOR-FXD 9.1PF +-.5PF 200VDC CER	51642	200-200-NP0-919D
A6C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C20	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C21	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C22	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A6C23	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A6C24	0160-3877	5		CAPACITOR-FXD 100PF +-20% 200VDC CER	28480	0160-3877
A6C25	0180-0374	3	2	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A6C26	0140-0210	2	2	CAPACITOR-FXD 270PF +-5% 300VDC MICA	72136	DM15F271J0300WV1CR
A6C27	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A6C28	0160-0690	4		CAPACITOR-FXD 1PF +-.5PF 100VDC CER	28480	0160-0690
A6C29	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C30	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C31	0160-4490	8		CAPACITOR-FXD 1.8PF +-.25PF 200VDC CER	28480	0160-4490
A6C32				NOT ASSIGNED		
A6C33	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C34	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C35	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C36	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A6C37	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A6C38	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C39	0160-4498	8		CAPACITOR-FXD 5.6PF +-.5PF 200VDC CER	51642	200-200-NP0-569D
A6C40	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C41	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A6C42	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C43	0160-4381	8	1	CAPACITOR-FXD 1.5PF +-.25PF 200VDC CER	51642	150-200-NP0-159C
A6C44	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C45	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A6C46	0160-0375	2		CAPACITOR-FXD 2.2PF +-.1PF 300VDC CER	28480	0160-0375
A6C47	0160-4535	4	2	CAPACITOR-FXD 1UF +-10% 50VDC CER	28480	0160-4535
A6C48	0160-0375	2		CAPACITOR-FXD 2.2PF +-.1PF 300VDC CER	28480	0160-0375
A6C49	0160-0570	9		CAPACITOR-FXD 220PF +-20% 100VDC CER	28932	5024EM100RD221M
A6C50	0160-4493	3	7	CAPACITOR-FXD 27PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-270J
A6C51	0160-4493	3		CAPACITOR-FXD 27PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-270J
A6C52†	0160-4084	8	5	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A6C53	0160-3873	1		CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A6C54	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C55	0160-4535	4		CAPACITOR-FXD 1UF +-10% 50VDC CER	28480	0160-4535
A6C56†	0121-0448	8	3	CAPACITOR-V TRMR-CER 2.5-5PF 63V PC-MTG	28480	0121-0448
A6C57	0121-0449	9		CAPACITOR-V TRMR-CER 3.5-10PF 63V PC-MTG	28480	0121-0449
A6C58	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C59†	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A6C60				NOT ASSIGNED		
A6C61	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C62	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C63	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6C64	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A6CR1	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR3	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A6CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR5†	1901-0844	3	4	DIODE-PIN	04713	MPN3401
A6CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR7†	1901-0844	3		DIODE-PIN	04713	MPN3401
A6CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR9	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A6CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR12	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A6CR13	1901-1096	9	3	DIODE-PIN	28480	1901-1096
A6CR14	1901-1096	9		DIODE-PIN	28480	1901-1096
A6CR15	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050

See introduction to this section for ordering information
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† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR18	1901-1096	9		DIODE-PIN	28480	1901-1096
A6CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR20	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR21	1901-0844	3		DIODE-PIN	04713	MPN3401
A6CR22	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR23	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR24	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR25†	0122-0329	6	2	DIODE-VVC 2.2PF 5% C3/C25-MIN=4.5	28480	0122-0329
A6CR26	0122-0065	7		DIODE-VVC 29PF 3%	28480	0122-0065
A6CR27	0122-0065	7		DIODE-VVC 29PF 3%	28480	0122-0065
A6CR28†	0122-0329	6		DIODE-VVC 2.2PF 5% C3/C25-MIN=4.5	28480	0122-0329
A6CR29	0122-0065	7		DIODE-VVC 29PF 3%	28480	0122-0065
A6CR30	0122-0065	7		DIODE-VVC 29PF 3%	28480	0122-0065
A6CR31	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR32	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR33	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR34	1901-0844	3		DIODE-PIN	04713	MPN3401
A6CR35	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR36	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR37	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR38	1906-0245	0	1	DIODE-MATCHED PAIR	28480	1906-0245
A6CR39	1906-0245	0		PART OF A6CR38	28480	1906-0245
A6CR40	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR41	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR42	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6J1	1251-5560	9		CONNECTOR 8-PIN M POST TYPE	28480	1251-5560
A6J2	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A6J3	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A6J4	1251-4051	3	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-4051
A6K1	0490-1171	7	1	RELAY-REED 2A 500MA 200VAC 5VDC-COIL	28480	0490-1171
A6L1	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L2	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L3	9100-1610	1		INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1610
A6L4	9100-1610	1		INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1610
A6L5	9100-1610	1		INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1610
A6L6	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L7	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L8	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L9	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L10	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L11	9100-1610	1		INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1610
A6L12	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L13	9100-2250	7	1	INDUCTOR RF-CH-MLD 1.2UH 10% .105DX.26LG	28480	9100-2250
A6L14	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L15	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L16	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L17	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A6L18	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A6L19				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L20				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L21	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A6L22	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L23	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L24	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L25				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L26				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L27	9100-2248	5		INDUCTOR RF-CH-MLD 120NH 10% .105DX.26LG	28480	9100-2248
A6L28				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L29				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L30	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A6L31				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L32				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L33	9100-3922	4	5	CHOKE, TOROIDAL 1.0UH	28480	9100-3922
A6L34	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L35				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L36	9100-3922	4		INDUCTOR-FIXED 120-1300 HZ	28480	9100-3922
A6L37	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L38				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L39				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L40				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L41				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L42				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L43				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L44				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L45				PART IS ETCHED TRACE ON CIRCUIT BOARD		

See introduction to this section for ordering information
*Indicates factory selected value
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6L46				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A6L47	9135-0073	3		INDUCTOR, 51NH	28480	9135-0073
A6L48	9135-0070	0	1	INDUCTOR 82NH	28480	9135-0070
A6L49	9135-0073	3		INDUCTOR, 51NH	28480	9135-0073
A6L50	9100-2255	4	1	INDUCTOR RF-CH-MLD 470NH 10% .105DX.26LG	28480	9100-2255
A6L51	9140-0150	6		INDUCTOR RF-CH-MLD 1UH 10% .105DX.26LG	28480	9140-0150
A6L52	9100-2252	1	1	INDUCTOR RF-CH-MLD 270NH 10% .105DX.26LG	28480	9100-2252
A6L53	9100-1640	7	1	INDUCTOR RF-CH-MLD 560UH 5% .2DX.45LG	28480	9100-1640
A6L54	9135-0075	5	2	INDUCTOR, 43NH	28480	9135-0075
A6MP1	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A6MP2	08656-00033	3		GROUND CLIP, SEMI-RIGID	28480	08656-00033
A6Q1	1854-0696	2		TRANSISTOR NPN SI TO-72 PD=200MW	28480	1854-0696
	1200-0172	4	2	INSULATOR-XSTR DAP-GL	28480	1200-0172
A6Q2	1854-0632	6		TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-91
A6Q3	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q4	1853-0281	9	1	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A6Q5	1853-0012	4	1	TRANSISTOR PNP 2N2904A SI TO-39 PD=600MW	01295	2N2904A
A6Q6	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q7	1854-0720	3	1	TRANSISTOR NPN SI PD=500MW FT=4GHZ	28480	1854-0720
A6Q8	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q9	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q10	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q11	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q12	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A6Q13	1853-0007	7		TRANSISTOR PNP 2N3251 SI TO-18 PD=360MW	04713	2N3251
A6Q14	1854-0696	2		TRANSISTOR NPN SI TO-72 PD=200MW	28480	1854-0696
	1200-0172	4		INSULATOR-XSTR DAP-GL	28480	1200-0172
A6Q15	1854-0721	4	1	TRANSISTOR NPN SI TO-39 PD=1.5W	25403	BFR 95
	1200-0173	5	3	INSULATOR-XSTR DAP-GL	28480	1200-0173
	1205-0011	0	1	HEAT SINK TO-5/TO-39-CS	28480	1205-0011
A6R1	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A6R2	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R3	0698-7194	6	1	RESISTOR 17.8 1% .05W F TC=0+-100	24546	C3-1/8-T00-17R8-G
A6R4*	0757-0400	9	2	RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A6R5	0698-7223	2	3	RESISTOR 287 1% .05W F TC=0+-100	24546	C3-1/8-T0-287R-G
A6R6	0698-7223	2		RESISTOR 287 1% .05W F TC=0+-100	24546	C3-1/8-T0-287R-G
A6R7	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A6R8	0698-3132	4		RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A6R9	0698-3440	7		RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A6R10	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R11	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R12	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A6R13	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A6R14	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R15	0698-3439	4	4	RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A6R16	0698-3440	7		RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A6R17	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A6R18	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R19	0698-3440	7		RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A6R20	0698-3161	9		RESISTOR 38.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3832-F
A6R21	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A6R22	0757-0401	0	8	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A6R23	0757-0420	3	2	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A6R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R25	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R26	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R27	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A6R28	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R29	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A6R30	2100-2031	7	1	RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	73138	82PR50K
A6R31	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A6R32	0698-3162	0	7	RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A6R33	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A6R34	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A6R35	2100-2061	3	1	RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	73138	82PR200
A6R36	0698-3162	0		RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A6R37	0698-3438	3		RESISTOR 147 1% .125W F TC=0+-100	24546	C4-1/8-T0-147R-F
A6R38	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R39	0698-7209	4	4	RESISTOR 75 1% .05W F TC=0+-100	24546	C3-1/8-T00-75R0-G
A6R40	0757-0200	7	2	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A6R41	0698-3162	0		RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A6R42	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R43	0698-7209	4		RESISTOR 75 1% .05W F TC=0+-100	24546	C3-1/8-T00-75R0-G
A6R44	0698-7209	4		RESISTOR 75 1% .05W F TC=0+-100	24546	C3-1/8-T00-75R0-G
A6R45	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6R46	0698-3442	9		RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A6R47	0698-7209	4		RESISTOR 75 1% .05W F TC=0+-100	24546	C3-1/8-T00-75R0-G
A6R48†	0757-0395	1	1	RESISTOR 56.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-56R2-F
A6R49	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R50	0699-0584	6	1	RESISTOR 90.9 1% .05W F TC=0+-100	28480	0699-0584
A6R51	0698-3445	2		RESISTOR 348 1% .125W F TC=0+-100	24546	C4-1/8-T0-348R-F
A6R52	0757-0397	3		RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
A6R53	0699-0583	5	1	RESISTOR 34.8 1% .05W F TC=0+-100	28480	0699-0583
A6R54	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R55	0698-7206	1	2	RESISTOR 56.2 1% .05W F TC=0+-100	24546	C3-1/8-T00-56R2-G
A6R56	0698-7205	0		RESISTOR 51.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-51R1-G
A6R57	0698-7223	2		RESISTOR 287 1% .05W F TC=0+-100	24546	C3-1/8-T0-287R-G
A6R58	0698-7206	1		RESISTOR 56.2 1% .05W F TC=0+-100	24546	C3-1/8-T00-56R2-G
A6R59	0698-7205	0		RESISTOR 51.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-51R1-G
A6R60	0757-0421	4	5	RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A6R61	0698-7205	0		RESISTOR 51.1 1% .05W F TC=0+-100	24546	C3-1/8-T00-51R1-G
A6R62	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A6R63	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R64	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R65	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A6R66	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R67	0698-7192	4	6	RESISTOR 14.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-14R7-G
A6R68	0757-0405	4		RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
A6R69	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A6R70	0698-7192	4		RESISTOR 14.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-14R7-G
A6R71	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R72	0698-7192	4		RESISTOR 14.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-14R7-G
A6R73	0698-3449	6	1	RESISTOR 28.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2872-F
A6R74	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A6R75	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R76	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R77	0698-7192	4		RESISTOR 14.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-14R7-G
A6R78	0757-0796	6	1	RESISTOR 82.5 1% .5W F TC=0+-100	28480	0757-0796
A6R79	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A6R80	0698-0083	8	5	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
A6R81	0698-7192	4		RESISTOR 14.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-14R7-G
A6R82	0698-7192	4		RESISTOR 14.7 1% .05W F TC=0+-100	24546	C3-1/8-T00-14R7-G
A6R83	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R84	0698-3390	4	1	RESISTOR 46.4 1% .5W F TC=0+-100	28480	0698-3390
A6R85	0698-8819	4	1	RESISTOR 3.83 1% .125W F TC=0+-100	28480	0698-8819
A6R86	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A6R87	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
A6R88	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R89	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A6R90	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A6R91	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
A6R92	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R93	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A6R94	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R95	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A6R96	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
A6R97	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1961-F
A6R98	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A6S1	3101-1162	6	1	SWITCH-SL SPDT MINTR .5A 125VAC/DC PC	28480	3101-1162
A6TP1	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A6TP2	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A6TP3	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A6TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A6TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A6TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A6U1	1820-1011	4	1	IC-DIGITAL	28480	1820-1011
	0340-0834	0	1	INSULATOR-XSTR POLYI	28480	0340-0834
A6U2	1820-2106	2	1	IC FF ECL D-M/S POS-EDGE-TRIG	07263	F11C06DC
A6U3	1826-0013	8	2	IC OP AMP LOW-NOISE TO-99 PKG	06665	SS8741CJ
A6U4	1820-1976	2		IC BFR CMOS NON-INV HEX	01928	CD4050BE
A6U5	1820-0618	7		IC BFR TTL NON-INV HEX	01295	SN7417N
A6U6	1826-0400	1	1	IC OP AMP WB TO-99 PKG	27014	LM218H
A6U7	1820-1662	3		IC SHF-RGTR CMOS SERIAL-IN PRL-OUT 8-BIT	01928	CD4094BE
A6U8	1820-1422	3	2	IC MV TTL LS MONOSTBL RETRIG	01295	SN74LS122N
A6U9	1820-0304	8	1	IC FF TTL J-K M/S PULSE PRESET/CLEAR	01295	SN7472N
A6U10	1826-0013	8		IC OP AMP LOW-NOISE TO-99 PKG	06665	SS8741CJ
A6U11	0955-0145	9		MIXER, DOUBLE BALANCED 1000MHZ	28480	0955-0145

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	08656-60063	5	1	RFI ASSEMBLY	28480	08656-60063
A7C1	0160-0571	0	7	CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A7C2	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A7C3	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A7C4	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A7C5	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A7C6	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A7C7	0160-0571	0		CAPACITOR-FXD 470PF +-20% 100VDC CER	28480	0160-0571
A7J1				PART OF ETCHED TRACE ON CIRCUIT BOARD		
A7J2				PART OF ETCHED TRACE ON CIRCUIT BOARD		
A7L1	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A7L2	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A7L3	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A7L4	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A7L5	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A7L6	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A7L7	9100-2247	4		INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A8	08656-60004	4	1	FREQUENCY MULTIPLIER ASSEMBLY	28480	08656-60004
A8C1	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A8C2	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C3	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C4	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C5	0160-4527	4	4	CAPACITOR-FXD 56PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-560J
A8C6	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C7	0160-2249	3	1	CAPACITOR-FXD 4.7PF +-.25PF 500VDC CER	28480	0160-2249
	4330-0145	9	8	INSULATOR-BEAD GLASS	28480	4330-0145
A8C8	0160-4527	4		CAPACITOR-FXD 56PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-560J
A8C9	0160-4527	4		CAPACITOR-FXD 56PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-560J
A8C10	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C11	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C12	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C13	0160-4383	8		CAPACITOR-FXD 6.8PF +-.5PF 200VDC CER	20932	5024E0200RD689D
A8C14	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C15	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C16	0160-4493	3		CAPACITOR-FXD 27PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-270J
A8C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C18	0160-2243	7	1	CAPACITOR-FXD 2.7PF +-.25PF 500VDC CER	28480	0160-2243
	4330-0145	9		INSULATOR-BEAD GLASS	28480	4330-0145
A8C19	0160-4493	3		CAPACITOR-FXD 27PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-270J
A8C20	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C21	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C22	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C23	0160-4493	3		CAPACITOR-FXD 27PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-270J
A8C24	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C25	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C26	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C27	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C28	0160-3873	1		CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A8C29	0160-3873	1		CAPACITOR-FXD 4.7PF +-.5PF 200VDC CER	28480	0160-3873
A8C30	0160-2237	9	1	CAPACITOR-FXD 1.2PF +-.25PF 500VDC CER	28480	0160-2237
	4330-0145	9		INSULATOR-BEAD GLASS	28480	4330-0145
A8C31	0121-0448	8		CAPACITOR-V TRMR-CER 2.5-5PF 63V PC-MTG	28480	0121-0448
A8C32	0160-4491	1		CAPACITOR-FXD 8.2PF +-5% 200VDC CER	51642	200-200-NP0-829J
A8C33	0160-4518	3		CAPACITOR-FXD 3.9PF +-.5PF 200VDC CER	51642	200-200-NP0-399D
A8C34	0160-4527	4		CAPACITOR-FXD 56PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-560J
A8C35†	0160-4382	9	3	CAPACITOR-FXD 3.3PF +-.25PF 200VDC CER	51642	200-200-NP0-339C
A8C36	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C37	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C38	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C39	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C40	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C41	0160-4383	8		CAPACITOR-FXD 6.8PF +-.5PF 200VDC CER	20932	5024E0200RD689D
A8C42	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C43	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C44	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C45	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C46	0160-2234	6	1	CAPACITOR-FXD .51PF +-.25PF 500VDC CER	28480	0160-2234
	4330-0145	9		INSULATOR-BEAD GLASS	28480	4330-0145
A8C47	0121-0452	4	1	CAPACITOR-V TRMR-AIR 1.3-5.4PF 175V	74970	187-0103-028
A8C48	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C49				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8C50	0160-4518	3		CAPACITOR-FXD 3.9PF +-.5PF 200VDC CER	51642	200-200-NP0-399D
A8C51				PART IS ETCHED TRACE ON CIRCUIT BOARD		

See introduction to this section for ordering information
*Indicates factory selected value
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8C52	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C53				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8C54	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C55	0160-3878	6		CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A8C56	0160-4382	9		CAPACITOR-FXD 3.3PF +-.25PF 200VDC CER	51642	200-200-NP0-339C
A8C57†	0160-4490	0	2	CAPACITOR-FXD 1.8PF +-.25PF 200VDC CER	28480	0160-4490
A8J1	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A8J2	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A8J3	1250-1626	0		CONNECTOR-RF SMC M PC 50-OHM	28480	1250-1626
	2190-0124	4	4	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0124
	2950-0078	9	2	NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	28480	2950-0078
A8J4	1250-1626	0		CONNECTOR-RF SMC M PC 50-OHM	28480	1250-1626
	2190-0124	4		WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0124
	2950-0078	9		NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	28480	2950-0078
A8L1	9100-1618	1		INDUCTOR RF-CH-MLD 5.6UH 10%	28480	9100-1618
A8L2	9140-0141	7		INDUCTOR RF-CH-MLD 680NH 10% .105DX.26LG	28480	9140-0141
A8L3				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L4				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L5				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L6				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L7	9100-3922	4		INDUCTOR-FIXED 120-1300 HZ	28480	9100-3922
A8L8				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L9				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L10				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L11	9100-2251	0	3	INDUCTOR RF-CH-MLD 220NH 10% .105DX.26LG	28480	9100-2251
A8L12				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L13				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L14				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L15				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L16	9100-3922	4		INDUCTOR-FIXED 120-1300 HZ	28480	9100-3922
A8L17				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L18				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L19				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L20				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L21				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L22				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L23				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L24	9100-2251	0		INDUCTOR RF-CH-MLD 220NH 10% .105DX.26LG	28480	9100-2251
A8L25				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L26				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L27	9100-3922	4		INDUCTOR-FIXED 120-1300 HZ	28480	9100-3922
A8L28				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L29				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L30				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L31				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L32				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L33				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L34				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L35				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L36				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L37				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L38				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L39				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L40	9100-2251	0		INDUCTOR RF-CH-MLD 220NH 10% .105DX.26LG	28480	9100-2251
A8L41				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L42				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8L43				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A8MP1	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A8MP2	1251-2194	1	2	CONNECTOR-SGL CONT SKT .021-IN-BSC-SZ	28480	1251-2194
A8MP3	8150-0459	0		WIRE 24AWG W/R 300V PVC 7X32 80C	28480	8150-0459
A8MP4	08656-00033	3		GROUND CLIP-SEMIRIGID	28480	08656-00033
A8Q1	1854-0632	6		TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-91
A8Q2	1854-0632	6		TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-91
A8Q3	1854-0632	6		TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-91
A8Q4	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
A8Q5	1854-0632	6		TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-91
A8Q6	1854-0696	2		TRANSISTOR NPN SI TO-72 PD=200MW	28480	1854-0696
A8Q7	1854-0247	9		TRANSISTOR NPN SI TO-39 PD=1W FT=800MHZ	28480	1854-0247
	1200-0173	5		INSULATOR-XSTR DAP-GL	28480	1200-0173
A8Q8	1854-0247	9		TRANSISTOR NPN SI TO-39 PD=1W FT=800MHZ	28480	1854-0247
	1200-0173	5		INSULATOR-XSTR DAP-GL	28480	1200-0173
A8R1	0757-0294	9	1	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
A8R2	0757-0403	2	1	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
A8R3	0698-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A8R4	0698-3443	0		RESISTOR 287 1% .125W F TC=0+-100	24546	C4-1/8-T0-287R-F
A8R5	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F

See introduction to this section for ordering information
*Indicates factory selected value
†FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8R6	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A8R7	0757-0398	4		RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A8R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A8R9	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A8R10	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A8R11†	0698-3442	9	7	RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A8R12	0757-0278	9	2	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A8R13	0757-0398	4		RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A8R14	0757-0278	9		RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A8R15	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A8R16	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A8R17	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A8R18	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A8R19	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A8R20	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A8R21	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A8R22	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A8R23	0757-0398	4		RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A8R24	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A8R25	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A8R26	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A8R27	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A8R28	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A8R29	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A8R30	0698-3153	9		RESISTOR 3.83K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3831-F
A8R31	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A8R32	0757-0398	4		RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A8R33	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A8R34	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A8R35	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A8R36	0757-0424	7		RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A8R37	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A8R38	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A8TP1	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A8TP2	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A8TP3	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A8U1†	0955-0145	9	2	MIXER, DOUBLE BALANCED, 1000MHZ	28480	0955-0145
A8W1	08656-20010	6	1	CABLE, COAX SEMI-RIGID #2	28480	08656-20010
A9	08656-60010	0	1	ATTENUATOR ASSEMBLY	28480	08656-60010
A9L1	0491-0106	8	1	SOLENOID BANK ASSEMBLY	28480	0491-0106
A9MP1	0400-0126	1	7	GROMMET-RND .125-IN-ID .180-IN-GRV-OD	28480	0400-0126
A9MP2	08656-00013	9	21	CONTACT, SWITCH ATTENUATOR	28480	08656-00013
A9MP3	08656-40002	0	7	CAM, ATTENUATOR	28480	08656-40002
A9MP4	08656-40003	1	4	CAM GUIDE, DUAL	28480	08656-40003
A9MP5	08656-40004	2	1	CAM GUIDE, SINGLE	28480	08656-40004
A9S1				PART IS COMPRISED OF MP1,MP2, & MP3		
A9A1	08656-60014	6	1	HETERODYNE/PAD/REVERSE POWER ASSEMBLY	28480	08656-60014
A9A1C1	0151-0013	4		WIRE 22AWG 1X22	28480	0151-0013
A9A1C2	0151-0013	4		WIRE 22AWG 1X22	28480	0151-0013
A9A1C3	0151-0013	4		WIRE 22AWG 1X22	28480	0151-0013
A9A1C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9A1C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A9A1C6	0151-0013	4		WIRE 22AWG 1X22	28480	0151-0013
A9A1C7	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A9A1C8	0151-0013	4		WIRE 22AWG 1X22	28480	0151-0013
A9A1CR1	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9A1CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A9A1J1	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A9A1J2	1250-1627	1	1	CONNECTOR-RF SMC M PC 50-OHM	28480	1250-1627
A9A1K1	0490-1073	8	1	RELAY-REED 1A 250MA 120VAC 4.5VDC-COIL	28480	0490-1073
A9A1L1	9135-0075	5		INDUCTOR RF-CH-MLD 43NH 8% .102DX.26LG	28480	9135-0075
A9A1MP1	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A9A1MP2	2190-0124	4		WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0124
A9A1MP3	2740-0010	4	2	NUT-HEX-DBL-CHAM 10-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A9A1MP4	08656-00033	3		GROUND CLIP-SEMI-RIGID	28480	08656-00033
A9A1MP5	08656-00057	1	1	BRACKET-ATTENUATOR WALL	28480	08656-00057

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9A1R1	0699-0089	6	6	RESISTOR 53.27 .1% .25W F TC=0+-50	28480	0699-0089
A9A1R2	0699-0094	3	3	RESISTOR 790 .1% .25W F TC=0+-50	28480	0699-0094
A9A1R3	0699-0089	6		RESISTOR 53.27 .1% .25W F TC=0+-50	28480	0699-0089
A9A1R4	0699-0092	1	2	RESISTOR 96.25 .1% .25W F TC=0+-50	28480	0699-0092
A9A1R5	0699-0091	0	1	RESISTOR 71.15 .1% .25W F TC=0+-50	28480	0699-0091
A9A1R6	0699-0092	1		RESISTOR 96.25 .1% .25W F TC=0+-50	28480	0699-0092
A9A1R7	0699-0089	6		RESISTOR 53.27 .1% .25W F TC=0+-50	28480	0699-0089
A9A1R8	0699-0094	3		RESISTOR 790 .1% .25W F TC=0+-50	28480	0699-0094
A9A1R9	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A9A1R10	0699-0089	6		RESISTOR 53.27 .1% .25W F TC=0+-50	28480	0699-0089
A9A1R11	0699-0090	9	2	RESISTOR 61.11 .1% .25W F TC=0+-50	28480	0699-0090
A9A1R12	0699-0093	2	1	RESISTOR 247.5 .1% .25W F TC=0+-50	28480	0699-0093
A9A1R13	0699-0090	9		RESISTOR 61.11 .1% .25W F TC=0+-50	28480	0699-0090
A9A1R14	0699-0089	6		RESISTOR 53.27 .1% .25W F TC=0+-50	28480	0699-0089
A9A1R15	0699-0094	3		RESISTOR 790 .1% .25W F TC=0+-50	28480	0699-0094
A9A1R16	0699-0089	6		RESISTOR 53.27 .1% .25W F TC=0+-50	28480	0699-0089
A9A1VR1	1902-0579	3	2	DIODE-ZNR 5.11V 5% DO-15 PD=1W TC=-.009%	28480	1902-0579
A9A1VR2	1902-0579	3		DIODE-ZNR 5.11V 5% DO-15 PD=1W TC=-.009%	28480	1902-0579
A10	08656-60006	6	1	AUDIO/POWER SUPPLY ASSEMBLY	28480	08656-60006
A10C1	0160-5035	1	1	CAPACITOR, FXD .051UF 2%	28480	0160-5035
A10C2	0160-5036	2	1	CAPACITOR, FXD .27UF 2%	28480	0160-5036
A10C3	0180-1835	3	1	CAPACITOR-FXD 68UF+-20% 15VDC TA	56289	150D686X0015R2
A10C4	0160-2225	5	1	CAPACITOR-FXD 2000PF +-5% 300VDC MICA	28480	0160-2225
A10C5	0160-0336	5	1	CAPACITOR-FXD 100PF +-1% 300VDC MICA	28480	0160-0336
A10C6	0160-3490	8	1	CAPACITOR-FXD 1UF +-20% 50VDC CER	28480	0160-3490
A10C7	0160-0127	2	2	CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
A10C8	0160-0127	2		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
A10C9	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10C10	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10C11	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A10C12	0140-0210	2		CAPACITOR-FXD 270PF +-5% 300VDC MICA	72136	DM15F271J0300WV1CR
A10C13	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A10C14	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A10C15	0160-3453	3		CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0160-3453
A10C16	0160-3453	3		CAPACITOR-FXD .05UF +80-20% 100VDC CER	28480	0160-3453
A10C17	0180-2074	2	3	CAPACITOR-FXD 3200UF+75-10% 40VDC AL	28480	0180-2074
A10C18	0180-2911	8	1	CAPACITOR-FXD .013F+75-10% 25VDC AL	28480	0180-2911
A10C19	0180-2074	2		CAPACITOR-FXD 3200UF+75-10% 40VDC AL	28480	0180-2074
A10C20	0180-2074	2		CAPACITOR-FXD 3200UF+75-10% 40VDC AL	28480	0180-2074
A10C21	0180-2141	6	1	CAPACITOR-FXD 3.3UF+-10% 50VDC TA	56289	150D335X9050B2
A10C22	0180-0550	5	1	CAPACITOR-FXD 470UF+-20% 10VDC TA	56289	150D477X0010S2
A10C23	0180-2144	9	2	CAPACITOR-FXD 200UF+75-10% 25VDC AL	56289	30D207G025DH9
A10C24	0180-1700	7	1	CAPACITOR-FXD 500UF+75-10% 10VDC AL	28480	0180-1700
A10C25	0180-2144	9		CAPACITOR-FXD 200UF+75-10% 25VDC AL	56289	30D207G025DH9
A10C26	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A10C27	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A10C28	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A10CR1	1901-0040	1	4	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A10CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A10CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A10CR4	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A10CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A10CR6	1901-0328	8	8	DIODE-PWR RECT 400V 1A 6US	03508	A14D
A10CR7	1901-0328	8		DIODE-PWR RECT 400V 1A 6US	03508	A14D
A10CR8	1901-0200	5	4	DIODE-PWR RECT 100V 1.5A	28480	1901-0200
A10CR9	1901-0200	5		DIODE-PWR RECT 100V 1.5A	28480	1901-0200
A10CR10	1901-0200	5		DIODE-PWR RECT 100V 1.5A	28480	1901-0200
A10CR11	1901-0200	5		DIODE-PWR RECT 100V 1.5A	28480	1901-0200
A10CR12	1901-0328	8		DIODE-PWR RECT 400V 1A 6US	03508	A14D
A10CR13	1901-0328	8		DIODE-PWR RECT 400V 1A 6US	03508	A14D
A10CR14	1901-0328	8		DIODE-PWR RECT 400V 1A 6US	03508	A14D
A10CR15	1901-0328	8		DIODE-PWR RECT 400V 1A 6US	03508	A14D
A10CR16	1901-0328	8		DIODE-PWR RECT 400V 1A 6US	03508	A14D
A10CR17	1901-0328	8		DIODE-PWR RECT 400V 1A 6US	03508	A14D
A10DS1	1990-0523	2	3	LED-LAMP LUM-INT=1MCD IF=50MA-MAX BVR=5V	28480	5082-4950
A10DS2	1990-0523	2		LED-LAMP LUM-INT=1MCD IF=50MA-MAX BVR=5V	28480	5082-4950
A10DS3	1990-0523	2		LED-LAMP LUM-INT=1MCD IF=50MA-MAX BVR=5V	28480	5082-4950
A10F1†	2110-0519	3	1	FUSE 4A 125V NTD .340X.25	75915	273004
	1251-1998	1	8	CONNECTOR-SGL CONT SKT .025-IN-BSC-SZ	28480	1251-1998
A10F2	2110-0516	0	2	FUSE 1A 125V NTD .340X.25	75915	273001
	1251-1998	1		CONNECTOR-SGL CONT SKT .025-IN-BSC-SZ	28480	1251-1998
A10F3	2110-0516	0		FUSE 1A 125V NTD .340X.25	75915	273001
	1251-1998	1		CONNECTOR-SGL CONT SKT .025-IN-BSC-SZ	28480	1251-1998

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10F4	2110-0520	6	1	FUSE 5A 125V NTD .340X.25	75915	273005
	1251-1990	1		CONNECTOR-SGL CONT SKT .025-IN-BSC-SZ	28480	1251-1990
A10J1	1251-5571	4	2	CONNECTOR 17-PIN M POST TYPE	28480	1251-5571
A10J2	1251-5569	8	2	CONNECTOR 7-PIN M POST TYPE	28480	1251-5569
A10J3	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A10J4	1251-5569	8		CONNECTOR 7-PIN M POST TYPE	28480	1251-5569
A10J5	1251-5611	3	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-5611
A10J6	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A10L1	9140-0144	0		INDUCTOR RF-CH-MLD 4.7UH 10% .105DX.26LG	28480	9140-0144
A10L2	9140-0142	8	1	INDUCTOR RF-CH-MLD 2.2UH 10% .105DX.26LG	28480	9140-0142
A10L3	9140-0144	0		INDUCTOR RF-CH-MLD 4.7UH 10% .105DX.26LG	28480	9140-0144
A10L4	9100-1635	2	1	INDUCTOR RF-CH-MLD 91UH 5% .166DX.385LG	28480	9100-1635
A10MP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A10MP2	1400-0482	3	6	CABLE TIE .062-3-DIA .14-WD NYL	28480	1400-0482
A10MP3	1400-0966	0		CLIP-HINGE	91506	6015-13AT
A10Q1	1884-0012	9	2	THYRISTOR-SCR 2N3528 TC-8 VRRM=200	01928	2N3528
A10Q2	1854-0010	2	2	TRANSISTOR NPN SI PD=625MW FT=200MHZ	28480	1854-0010
A10Q3	1884-0012	9		THYRISTOR-SCR 2N3528 TO-8 VRRM=200	01928	2N3528
A10Q4	1855-0253	9	2	TRANSISTOR J-FET N-CHAN D-MODE TO-92 SI	28480	1855-0253
A10Q5				NOT ASSIGNED		
A10Q6	1855-0020	0	5	TRANSISTOR J-FET N-CHAN D-MODE TO-18 SI	28480	1855-0020
A10Q7	1855-0020	0		TRANSISTOR J-FET N-CHAN D-MODE TO-18 SI	28480	1855-0020
A10Q8	1855-0020	0		TRANSISTOR J-FET N-CHAN D-MODE TO-18 SI	28480	1855-0020
A10Q9	1855-0020	0		TRANSISTOR J-FET N-CHAN D-MODE TO-18 SI	28480	1855-0020
A10Q10	1855-0020	0		TRANSISTOR J-FET N-CHAN D-MODE TO-18 SI	28480	1855-0020
A10Q11	1855-0253	9		TRANSISTOR J-FET N-CHAN D-MODE TO-92 SI	28480	1855-0253
A10Q12	1884-0010	5	1	THYRISTOR-SCR 2N4186 VRRM=200	04713	2N4186
A10R1	0757-0814	9	1	RESISTOR 511 1% .5W F TC=0+-100	28480	0757-0814
A10R2	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
A10R3	2100-0568	1	2	RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A10R4	0698-3440	7		RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A10R5	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A10R6	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R7	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A10R8	0698-3441	0		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
A10R9	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A10R10	0757-0461	2		RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A10R11	0698-3457	6		RESISTOR 316K 1% .125W F TC=0+-100	28480	0698-3457
A10R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R13	0757-0288	1	2	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A10R14	0757-0420	3		RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-T0-751-F
A10R15	0698-5405	0	1	RESISTOR 600 1% .25W F TC=0+-100	24546	C5-1/4-T0-600R-F
A10R16	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A10R17	0698-8827	4	3	RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A10R18	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A10R19	0698-8827	4		RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A10R20	0698-3160	0		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A10R21	0683-1065	7	1	RESISTOR 10M 5% .25W CC TC=-900/+1100	01121	CB1065
A10R22	0698-6983	9	4	RESISTOR 20.4K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-2042-B
A10R23	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A10R24	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A10R25	0698-6983	9		RESISTOR 20.4K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-2042-B
A10R26	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A10R27	0698-6320	0	2	RESISTOR 5K .1% .125W F TC=0+-25	03888	PME55-1/8-T9-5001-B
A10R28	0698-8863	0	2	RESISTOR 5.2K .1% .125W F TC=0+-25	28480	0698-8863
A10R29	0757-0288	1		RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A10R30	0698-8863	0		RESISTOR 5.2K .1% .125W F TC=0+-25	28480	0698-8863
A10R31	0698-6320	0		RESISTOR 5K .1% .125W F TC=0+-25	03888	PME55-1/8-T9-5001-B
A10R32	2100-0567	8	2	RESISTOR-TRMR 2K 10% C TOP-ADJ 1-TRN	28480	2100-0567
A10R33	2100-3212	0	1	RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	28480	2100-3212
A10R34	0757-0401	8		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A10R35	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A10R36	0698-3151	7		RESISTOR 2.87K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2871-F
A10R37	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R38	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R39	0757-0422	5		RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A10R40	0698-4424	9	1	RESISTOR 1.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1401-F
A10R41	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R42	0698-3454	3		RESISTOR 215K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2153-F
A10R43	0698-3454	3		RESISTOR 215K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2153-F
A10R44	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A10R45	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10R46	0698-3459	8	1	RESISTOR 383K 1% .125W F TC=0+-100	28480	0698-3459
A10R47	2100-0558	9	1	RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	28480	2100-0558
A10R48	0698-8827	4		RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A10R49	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A10R50	0698-6347	9	1	RESISTOR 1.5K .1% .125W F TC=0+-25	28480	0698-6347
A10R51	0698-7394	8	1	RESISTOR 698 .1% .125W F TC=0+-25	19701	MF4C1/8-T9-698R-B
A10R52	0698-3451	0	2	RESISTOR 133K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1333-F
A10R53	0698-3451	0		RESISTOR 133K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1333-F
A10R54	0698-6983	9		RESISTOR 20.4K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-2042-B
A10R55	0698-6983	9		RESISTOR 20.4K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-2042-B
A10R56	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A10R57	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A10R58	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A10R59	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R60	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A10R61	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A10R62	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A10R63	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A10R64	2100-0567	0		RESISTOR-TRMR 2K 10% C TOP-ADJ 1-TRN	28480	2100-0567
A10R65	0698-3405	4	1	RESISTOR 422 1% .5W F TC=0+-100	28480	0698-3405
A10R66	0698-3407	6	3	RESISTOR 1.96K 1% .5W F TC=0+-100	28480	0698-3407
A10R67	0757-0816	1	1	RESISTOR 681 1% .5W F TC=0+-100	28480	0757-0816
A10R68	0698-3407	6		RESISTOR 1.96K 1% .5W F TC=0+-100	28480	0698-3407
A10R69	0698-3407	6		RESISTOR 1.96K 1% .5W F TC=0+-100	28480	0698-3407
A10R70	0757-0198	2	1	RESISTOR 100 1% .5W F TC=0+-100	28480	0757-0198
A10R71	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10R72	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A10R73	0698-6942	0	1	RESISTOR 25K .1% .125W F TC=0+-50	28480	0698-6942
A10R74	0698-8284	7	1	RESISTOR 110.37K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-110371-B
A10R75	0810-0056	1	1	RESISTOR 1 3% 10W PW TC=0+-50	91637	CW10-1-11W-T2-1R0-H
A10R76	0698-7861	4	1	RESISTOR 25.42K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-25421-B
A10R77	0698-6722	4	1	RESISTOR 124K .1% .125W F TC=0+-50	28480	0698-6722
A10R78	0757-1000	7	1	RESISTOR 51.1 1% .5W F TC=0+-100	28480	0757-1000
A10R79	2100-1760	5	1	RESISTOR-TRMR 20 5% WW TOP-ADJ 1-TRN	28480	2100-1760
A10R80	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A10R81	0698-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A10R82	0757-0158	4	2	RESISTOR 619 1% .5W F TC=0+-100	28480	0757-0158
A10R83	0698-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-T0-178R-F
A10R84	0757-0158	4		RESISTOR 619 1% .5W F TC=0+-100	28480	0757-0158
A10TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A10TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A10U1	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A10U2	1826-0412	1	1	IC COMPARATOR PRCN DUAL 8-DIP-P PKG	27014	LM393N
A10U3	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A10U4	1826-0462	1	3	IC CONV 10-B-D/A 16-DIP-C PKG	04713	MC3410CL
A10U5	1820-1730	6	7	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A10U6	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A10U7	1820-2111	9	3	IC DRVR TTL INV	01295	SN75468N
A10U8	1826-0462	1		IC CONV 10-B-D/A 16-DIP-C PKG	04713	MC3410CL
A10U9	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A10U10	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A10U11	1820-2111	9		IC DRVR TTL INV	01295	SN75468N
A10U12	1820-2111	9		IC DRVR TTL INV	01295	SN75468N
A10U13	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A10U14	1826-0462	1		IC CONV 10-B-D/A 16-DIP-C PKG	04713	MC3410CL
A10U15	1826-0371	1	2	IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	27014	LF256H
A10U16	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A10U17	1826-0521	3	2	IC OP AMP DUAL 8-DIP-P PKG	01295	TL072CP
A10U18	1826-0323	3		IC OP AMP GP QUAD 14-DIP-C PKG	28480	1826-0323
A10U19	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A10U20	1826-0521	3		IC OP AMP DUAL 8-DIP-P PKG	01295	TL072CP
A10U21	1826-0138	8	2	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A10U22	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A10U23	1826-0371	1		IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG	27014	LF256H
A10VR1	1902-1299	6	2	DIODE-ZNR 3.3V 10% DO-15 PD=1W TC=-.061%	28480	1902-1299
A10VR2	1902-1299	6		DIODE-ZNR 3.3V 10% DO-15 PD=1W TC=-.061%	28480	1902-1299
A10VR3	1902-0777	3	1	DIODE-ZNR 1N825 6.2V 5% DO-7 PD=.4W	04713	1N825
A10VR4	1902-0064	1		DIODE-ZNR 7.5V 5% DO-35 PD=.4W TC=+.05%	28480	1902-0064
A10VR5	1902-3301	1	1	DIODE-ZNR 68.1V 5% DO-7 PD=.4W TC=+.079%	28480	1902-3301
A10VR6	1902-3139	7		DIODE-ZNR 8.25V 5% DO-35 PD=.4W	28480	1902-3139
A11	08656-60007	7	1	MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY	28480	08656-60007

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11C1	0180-2207	5	1	CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2
A11C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A11C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C4	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A11C5	0180-0116	1	4	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A11C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C8	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A11C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C10	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A11C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C16	0160-4493	3		CAPACITOR-FXD 27PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-270J
A11C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C20	0160-0574	3		CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-0574
A11C21	0160-0574	3		CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-0574
A11C22	0160-4493	3		CAPACITOR-FXD 27PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-270J
A11CR1	1901-0518	8	1	DIODE-SM SIG SCHOTTKY	28480	1901-0518
A11J1	1251-5571	4		CONNECTOR 17-PIN M POST TYPE	28480	1251-5571
	1251-5595	2	1	KEY, POLARIZING	28480	1251-5595
A11J2	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A11J3	1251-5835	3	1	CONNECTOR 6-PIN M POST TYPE	28480	1251-5835
A11J4	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A11J5	1251-5855	7	1	CONNECTOR 16-PIN M POST TYPE	28480	1251-5855
A11J6	1251-5671	5	1	CONNECTOR 20-PIN M POST TYPE	28480	1251-5671
A11MP1	1400-0966	8		CLIP-HINGE	91506	6015-13AT
A11Q1	1854-0810	2		TRANSISTOR NPN SI PD=625MW FT=200MHZ	28480	1854-0810
A11R1	0698-3162	0		RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A11R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R4	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R5	0698-3162	0		RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A11R6	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A11R7	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A11R8	0698-3162	0		RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A11R9	1810-0278	4	1	NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
A11R10	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A11R11	0757-0279	0		RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A11R12	0698-3162	0		RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A11R13	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A11R14	1810-0205	7	1	NETWORK, RES 4.7K 8-PIN-SIP .1-PIN-SPCG	01121	208A472
A11R15	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A11R16	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A11S1	3101-2172	8	2	SWITCH-TGL DIP-RKR-ASSY SPDT .05A 30VDC	28480	3101-2172
A11S2	3101-2172	8		SWITCH-TGL DIP-RKR-ASSY SPDT .05A 30VDC	28480	3101-2172
A11S3	3101-2335	7	1	SWITCH-RKR DIP-RKR-ASSY 3PDT .05A 30VDC	28480	3101-2335
A11S4	3101-2135	5	1	SWITCH-RKR DIP-RKR-ASSY DPDT .05A 30VDC	28480	3101-2135
A11TP1	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP6	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP7	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP8	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP9	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP10	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP11	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP12	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP13	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP14	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP15	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP16	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP17	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A11TP18	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11U1	1820-1240	3	3	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A11U2†	1818-1365	8	1	ROM #1	18324	N2616N MASKED
A11U3	1818-0701	4	2	IC NMOS 1024 (1K) RAM STAT 360-NS 3-S	04713	MCM68A10P
A11U4	1818-0701	4		IC NMOS 1024 (1K) RAM STAT 360-NS 3-S	04713	MCM68A10P
A11U5†	1818-1362	5	1	ROM #6	18324	N2616N MASKED
A11U6†	1818-1361	4	1	ROM #5	18324	N2616N MASKED
A11U7†	1818-1360	3	1	ROM #4	18324	N2616N MASKED
A11U8†	1818-1359	0	1	ROM #3	18324	N2616N MASKED
A11U9†	1818-1358	9	1	ROM #2	18324	N2616N MASKED
A11U10	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A11U11	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A11U12	1820-1759	9	4	IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A11U13	1820-2099	2	1	IC MICPROC NMOS 8-BIT	04713	MC6802P
A11U14	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
A11U15	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
A11U16	1820-1491	6	1	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
A11U17	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A11U18	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A11U19	1820-2219	8	1	IC MICPROC-ACCESS NMOS 8-BIT	04713	MC68488P
A11U20	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A11U21	1820-1200	5	1	IC INV TTL LS HEX	01295	SN74LS05N
A11U22	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A11U23	1820-1609	4	4	IC UART TTL QUAD	01295	MC3446P
A11U24	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A11U25	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A11U26	1820-1609	4		IC UART TTL QUAD	01295	MC3446P
A11U27	1820-1609	4		IC UART TTL QUAD	01295	MC3446P
A11U28	1820-1422	3		IC MV TTL LS MONOSTBL RETRIG	01295	SN74LS122N
A11U29	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A11U30	1820-1609	4		IC UART TTL QUAD	01295	MC3446P
A11U31	1820-1560	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A11U32	1820-2056	1		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS378N
A11U33	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A11VR1	1902-3070	5	1	DIODE-ZNR 4.22V 5% DO-35 PD=.4W	28480	1902-3070
A11Y1	0410-0465	2	1	CRYSTAL-QUARTZ 4.00000 MHZ HC-6/U-HLDR	28480	0410-0465
A12	08656-60016	8	1	VOLTAGE REGULATOR ASSEMBLY	28480	08656-60016
A12C1	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A12C2	0160-0575	4		CAPACITOR-FXD .047UF +-20% 50VDC CER	28480	0160-0575
A12C3	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A12C4	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A12C5	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A12C6	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A12J1	1251-5810	4	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-5810
A13	08656-60064	6	1	HP-IB CONNECTOR ASSEMBLY	28480	08656-60064
A13J1				PART IS ETCHED TRACE ON CIRCUIT BOARD		
A13J2	1251-3283	1	1	CONNECTOR 24-PIN F MICRORIBBON	28480	1251-3283
A13MP1	0380-0644	4	2	STANDOFF-HEX .327-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
A13MP2	1530-1098	4	2	CLEVIS 0.070-IN W SLT: 0.454-IN PIN CTR	00000	ORDER BY DESCRIPTION
A13MP3	2190-0034	5		WASHER-LK HLCL NO. 10 .194-IN-ID	28480	2190-0034
A13MP4	2200-0109	8	2	SCREW-MACH 4-40 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A13MP5	2260-0009	3	4	NUT-HEX-W/LKWR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A14	08656-60070	2	1	FILTER BANK ASSEMBLY	28480	08656-60070
A14J1	1251-5080	8	1	CONNECTOR 15-PIN M D SUBMINIATURE	28480	1251-5080
A14J2	1251-4966	9	2	CONNECTOR 8-PIN M POST TYPE	28480	1251-4966
A14J3	1251-4966	9		CONNECTOR 8-PIN M POST TYPE	28480	1251-4966
A14MP1	0460-1439	7		TAPE, INDUSTRIAL (1 INCH)	28480	0460-1439
A14MP2	2200-0103	2		SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A14MP3	2260-0009	3		NUT-HEX-W/LKWR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A14MP4	08656-00047	9	1	CORNER BRACKET, REAR PANEL	28480	08656-00047
A14MP5	08656-00048	0	1	GASKET, CORNER BRACKET	28480	08656-00048
A15	0960-0443	1	1	LINE POWER MODULE	28480	0760-0443
	0360-0001	5	3	TERMINAL-SLDR LUG LK-MTG FOR-#6-SCR	28480	0360-0001
	0890-0983	5		TUBING-HS .125-D/.062-RCVD .02-WALL	28480	0890-0983
	8150-2919	1		WIRE 18AWG G/Y 600V PVC 19X30 105C	28480	8150-2919
	8151-0013	4	5	WIRE 22AWG 1X22	28480	8151-0013
	7120-8986	0	1	LABEL	28480	7120-8986

See introduction to this section for ordering information
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† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A16	0950-0411	2	1	10 MHZ REFERENCE OSCILLATOR ASSEMBLY	28480	0950-0411
	8150-2090	7	1	WIRE 18AWG BK 600V PVC 19X30 105C	28480	8150-2090
	8150-0447	6	1	WIRE 24AWG BK 300V PVC 7X32 80C	28480	8150-0447
	2200-0103	2	20	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2360-0113	2		SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	0360-0001	5		TERMINAL-SLDR LUG LK-MTG FOR-#6-SCR	28480	0360-0001
	0360-0053	7	2	TERMINAL-SLDR LUG LK-MTG FOR-#10-SCR	28480	0360-0053
	0590-1245	8	5	NUT-SHMET-U-TP 6-32-THD .017-IN-THK	00000	ORDER BY DESCRIPTION
	3050-0066	8	6	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
	08656-00005	7	1	FINGER GUARD-INTERNAL	28480	08656-00005
	2360-0199	4	3	SCREW-MACH 6-32 .430-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A16W1	08656-60066	8	1	CABLE-COAXIAL, REF. OSC./A16J1	28480	08656-60066
A16W2	8120-2682	2	1	CABLE-COAXIAL, A16J1/J3	28480	8120-2682
A17†	08656-60001	7	1	FRONT FEEDTHRU ASSEMBLY	28480	08656-60001

See introduction to this section for ordering information
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Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
B1	3160-0346	0	1	FAN-TBAX 36-CFM 115V 50/60-HZ 1.5KV-DIEL	28480	3160-0346
	0590-1245	8		NUT-SHMET-U-TP 6-32-THD .017-IN-THK	00000	ORDER BY DESCRIPTION
	2360-0205	3	2	SCREW-MACH 6-32 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2360-0199	4		SCREW-MACH 6-32 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
C1	0160-4900	7	19	CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C2	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C3	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C4	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C5	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C6	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C7	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C8	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C9	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C10	0160-4082	6		CAPACITOR-FDTHRU 1000PF 20% 200V CER (INCLUDES MOUNTING HARDWARE)	28480	0160-4082
C11	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C12	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C13	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C14	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C15	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C16	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C17	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C18	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C19	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C20	0160-4900	7		CAPACITOR-FDTHRU 1000PF +80 -20% 200V	72982	2425-011-X5U0-102-M
C21	0160-4090	2	2	CAPACITOR-FDTHRU 100PF +80 -20% 200V CER	72982	2425-011-X5U0-101-M
C22	0160-4090	2		CAPACITOR-FDTHRU 100PF +80 -20% 200V CER	72982	2425-011-X5U0-101-M
C23	0160-4071	3	1	CAPACITOR-FDTHRU 20PF 20% 200V CER	28480	0160-4071
	08656-00071	9	1	MOUNTING FLANGE	28480	08656-00071
	08656-20079	9	1	NUT-FLANGE	28480	08656-20079
F1	2110-0016	5	1	FUSE .6A 250V TD 1.25X.25 UL (FOR 220/240V OPERATION)	75915	313.600
F1	2110-0305	5	1	FUSE 1.25A 250V TD 1.25X.25 UL (FOR 100/120V OPERATION)	75915	3131.25
FL1	08656-60005	5	1	FILTER, BANDPASS	28480	08656-60005
	8151-0013	4		WIRE 22AWG 1X22	28480	8151-0013
	8159-0005	0		WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
FL2	9135-0099	3	2	FILTER, LOW-PASS	28480	9135-0099
FL3	9135-0099	3		FILTER, LOW-PASS	28480	9135-0099
J1	1250-0110	3	5	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM (MOD INPUT/OUTPUT;EXCEPT OPT 002)	28480	1250-0110
	2190-0016	3	5	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
	2950-0001	8	5	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
	8150-0464	7		WIRE 24AWG W/V 300V PVC 7X32 80C	28480	8150-0464
J2				CONNECTOR, NSR P/O W11 (RF OUTPUT)		
J3	1250-0110	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM (TIME BASE INPUT)	28480	1250-0110
	0360-1190	5	2	TERMINAL-SLDR LUG PL-MTG FOR-#3/8-SCR	28480	0360-1190
	0890-0050	7		TUBING-HS .405-D/.29-RCVD .02-WALL PVC	28480	0890-0050
	0890-0983	5		TUBING-HS .125-D/.062-RCVD .02-WALL	28480	0890-0983
	2190-0016	3		WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
	2950-0001	8		NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
	8150-0462	5	1	WIRE 24AWG W/G 300V PVC 7X32 80C	28480	8150-0462
J4	1250-0110	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM (TIME BASE OUTPUT)	28480	1250-0110
	0360-1190	5		TERMINAL-SLDR LUG PL-MTG FOR-#3/8-SCR	28480	0360-1190
	0890-0983	5		TUBING-HS .125-D/.062-RCVD .02-WALL	28480	0890-0983
	2190-0016	3		WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
	2950-0001	8		NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
	8150-0460	3	2	WIRE 24AWG W/O 300V PVC 7X32 80C	28480	8150-0460
J5	1250-0110	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM (SEQ; EXCEPT OPT. 002)	28480	1250-0110
	2190-0016	3		WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
	2950-0001	8		NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
J6	1250-0110	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM (MOD INPUT/OUTPUT;OPT 002 ONLY)	28480	1250-0110
	2190-0016	3		WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
	2950-0001	8		NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
	8150-0404	5	1	WIRE 18AWG O 300V PVC 19X30 80C	28480	8150-0404
L1†	9100-2257	6	2	INDUCTOR RF-CH-MLD 820NH 10% .105DX.26LG	28480	9100-2257
L2†	9100-2257	6		INDUCTOR RF-CH-MLD 820NH 10% .105DX.26LG	28480	9100-2257

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP1	08656-20100	7	1	FRAME-MACHINED	28480	08656-20100
MP2	08656-00004	8	1	COVER-INSTRUMENT-TOP	28480	08656-00004
MP3	08656-40001	9	2	COVER-INSTRUMENT-SIDE	28480	08656-40001
MP4	5060-9803	2	2	HANDLE-STRAP	28480	5060-9803
MP5	08656-20102	9	2	CAP-FRONT	28480	08656-20102
MP6	2680-0110	5	4	SCREW-MACH 10-32 .5-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
MP7	08656-20103	0	2	CAP-REAR	28480	08656-20103
MP8	5040-7202	9	1	TRIM-TOP	28480	5040-7202
MP9	5001-0439	8	2	TRIM-SIDE	28480	5001-0439
MP10†	08656-00076	4	1	COVER-INTERNAL RF-TOP	28480	08656-00076
MP11	08656-00034	4	1	HINGE-TOP	28480	08656-00034
MP12	1460-1761	9	4	HINGE-SPRING	28480	1460-1761
MP13	08656-00069	5		HINGE LOCK	28480	08656-00069
MP14	2360-0111	8	4	SCREW-MACH 6-32 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP15	08656-00059	3	1	HINGE-BOTTOM	28480	08656-00059
MP16†	08656-00069	5	3	HINGE LOCK	28480	08656-00069
MP17	08656-20083	5	1	CLAMP-ATTENUATOR PLATE	28480	08656-20083
MP18	2360-0203	1	17	SCREW-MACH 6-32 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP19	2190-0006	1	25	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0006
MP20†	08656-00078	6	2	GASKET-ATTENUATOR	28480	08656-00078
MP21	08656-00045	7	2	INSULATOR-ATTENUATOR	28480	08656-00045
MP22	08656-00068	4	1	INSULATOR-ATTENUATOR	28480	08656-00068
MP23†	08656-00075	3	1	COVER-INTERNAL RF-BOTTOM	28480	08656-00075
MP24	2360-0113	2		SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP25	08656-00005	9	1	COVER-BOTTOM	28480	08656-00005
MP26	08656-20101	8	2	FOOT-FRONT	28480	08656-20101
MP27	5040-7201	8	2	FOOT-REAR	28480	5040-7201
MP28	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP29†	08656-00079	7	4	COVER-INTERNAL RF #1	28480	08656-00079
MP30†	08656-00080	0	2	COVER-INTERNAL RF #2	28480	08656-00080
MP31†	08656-00081	1	2	COVER-INTERNAL RF #3	28480	08656-00081
MP32†	08656-00082	2	2	COVER-INTERNAL RF #4	28480	08656-00082
MP33†	08656-00083	3	2	COVER-INTERNAL RF #5	28480	08656-00083
MP34†	08656-00084	4	2	COVER-INTERNAL RF #6	28480	08656-00084
MP35†	08656-00085	5	1	COVER-INTERNAL RF #7	28480	08656-00085
MP36†	08656-00086	6	7	COVER-INTERNAL RF #8	28480	08656-00086
MP37†	08656-00087	7	3	COVER-INTERNAL RF #9	28480	08656-00087
MP38	08656-00027	5	2	SHIELD-PIN MODULATOR	28480	08656-00027
MP39	0590-1285	6	62	NUT-SELF THREADING .375 IN A/F; .116 IN	00000	ORDER BY DESCRIPTION
MP40	0360-1665	9	1	TERMINAL STRIP 3-TERM PHEN 1.13-IN-L	28480	0360-1665
MP41	2510-0133	5	5	SCREW-MACH 8-32 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP42	2190-0010	7	1	WASHER-LK EXT T NO. 8 .168-IN-ID	28480	2190-0010
MP43	08656-00037	7	1	SR WALL CLIP	28480	08656-00037
MP44	08656-00039	9	1	CLIP-FEED THRU	28480	08656-00039
MP45	1400-0249	0	14	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
MP46	1400-0510	8		CLAMP-CABLE .15-DIA .62-WD NYL	28480	1400-0510
MP47	2740-0003	5	29	NUT-HEX-W/LKWR 10-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
MP48	08656-20082	4	1	GASKET-ATTENUATOR PLATE CLAMP	28480	08656-20082
MP49	7120-0726	6	1	LABEL 'AM ADJ/DET ADJ'	28480	7120-0726
MP50	7120-0130	6	1	LABEL 'CAUTION DO NOT REMOVE'	28480	7120-0130
MP51	7120-0346	6	1	LABEL 'FRONT'	28480	7120-8346
MP52	2360-0135	0	1	SCREW-MACH 6-32 1.5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP53†	0160-0350	1	1	GASKET-RFI BEAD	28480	0160-0350
MP54†	0160-0351	2	4	GASKET-RFI BEAD	28480	0160-0351
MP55	3050-0002	2	1	WASHER-FL MTLC NO. 10 .203-IN-ID	28480	3050-0002
MP56	2360-0121	2	1	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP57	3050-0227	3	1	WASHER-FL MTLC NO. 6 .149-IN-ID	28480	3050-0227
MP58	2190-0007	2	1	WASHER-LK INTL T NO. 6 .141-IN-ID	28480	2190-0007
MP59- MP99				NOT ASSIGNED		
MP100	08656-00046	0	1	PANEL-FRONT(EXCEPT OPT 002)	28480	08656-00046
MP100	08656-00094	6	1	PANEL-FRONT(OPT 002 ONLY)	28480	08656-00094
MP101	2360-0105	0	4	SCREW-MACH 6-32 .5-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
MP102	08656-20066	4	1	WINDOW-FRONT PANEL-RIGHT	28480	08656-20066
MP103	08656-20067	5	1	WINDOW-FRONT PANEL-LEFT	28480	08656-20067
MP104	08656-20068	6	1	WINDOW-FRONT PANEL-CENTER	28480	08656-20068
MP105†	08731-210	2	1	NUT-LOCK	28480	08731-210
MP106	7120-1254	1	1	NAMEPLATE .312-IN-WD .54-IN-LG AL	28480	7120-1254
MP107	2200-0103	2		SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP108				NOT ASSIGNED		
MP109				NOT ASSIGNED		
MP110	08656-00063	9	1	SHROUD-FAN	28480	08656-00063
MP111	2360-0302	1	3	SCREW-MACH 6-32 1.625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP112	2190-0087	8		WASHER-LK HLCL NO. 8 .168-IN-ID	28480	2190-0087
MP113	08656-40009	7	1	FOOT-LEFT REAR	28480	08656-40009

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP114	2510-0124	4	2	SCREW-MACH 8-32 .625-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
MP115	2190-0017	4	4	WASHER-LK HLCL NO. 8 .168-IN-ID	28480	2190-0017
MP116	3050-0139	6	2	WASHER-FL MTLC NO. 8 .172-IN-ID	28480	3050-0139
MP117	2580-0004	6	2	NUT-HEX-DBL-CHAM 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
MP118†	08656-40013	3	1	SERIES REGULATOR COVER	28480	08656-40013
MP119	0361-1090	4	1	RIVET-PRESS ON	28480	0361-1090
MP120	08656-00007	1	1	PANEL-LEFT REAR(EXCEPT OPT 002)	28480	08656-00007
MP120	08656-00095	7	1	PANEL-LEFT REAR(OPT 002 ONLY)	28480	08656-00095
MP121	08656-00049	1	1	GASKET-LEFT REAR PANEL (EXCEPT OPT. 002)	28480	08656-00049
MP121	08656-00096	0	1	GASKET-LEFT REAR PANEL (OPT 002 ONLY)	28480	08656-00096
MP122	2360-0195	0	5	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP123	08656-00064	0	1	BRACKET-CRYSTAL	28480	08656-00064
MP124	2360-0115	4	1	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP125	08656-40010	8	1	FOOT-RIGHT REAR	28480	08656-40010
MP126	3050-0066	0		WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
MP127	08656-40011	1	1	GROMMET-LARGE HOLE	28480	08656-40011
MP128	7120-4295	6	2	LABEL-'HAZARDOUS VOLTAGE'	28480	7120-4295
MP129	7120-5911	5	1	LABEL-'METRIC THREADED FASTENERS'	28480	7120-5911
MP130	1251-6539	6	1	CONNECTOR-MIN. F RECP	28480	1251-6539
MP131	1251-6540	9	1	CONNECTOR-MIN-M PLUG	28480	1251-6540
MP132	1251-6541	0	2	HOOD-MINIATURE	28480	1251-6541
MP133	6960-0002	4	1	PLUG-HOLE DOME-HD FOR .5-D-HOLE STL	28480	6960-0002
MP134	3160-0300	6	1	GUARD-FINGER-EXTERNAL	28480	3160-0300
MP135†				NOT ASSIGNED		
MP136	1400-0510	8		CLAMP-CABLE .15-DIA .62-WD NYL (OPT. 002 ONLY)	28480	1400-0510
MP137	6960-0009	1	1	PLUG-HOLE FL-HD FOR .430-D-HOLE BRS (OPT. 002 ONLY)	28480	6960-0009
T1	9100-5000	3	1	TRANSFORMER	28480	9100-5000
	0360-0053	7		TERMINAL-SLDR LUG LK-MTG FOR-#10-SCR	28480	0360-0053
	2190-0034	5	7	WASHER-LK HLCL NO. 10 .194-IN-ID	28480	2190-0034
	1251-3252	4	2	CONTACT-CONN U/W-SUBMIN-D FEM CRP	28480	1251-3252
	1251-4283	3	2	CONTACT-CONN U/W-POST-TYPE FEM CRP	28480	1251-4283
	2680-0073	1	4	SCREW-MACH 10-32 2-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
U1†	1826-0019	2	1	IC-VOLTAGE REGULATOR TO-3	28480	1826-0019
	2200-0111	2	1	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2200-0113	4	8	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
U2	1826-0513	3	1	IC V RGLTR TO-3	80103	LAS-1905
U2†	1200-0043	0	1	INSULATOR-XSTR ALUMINUM	28480	1200-0043
	2200-0113	4		SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	08660-40002	6	3	INSULATOR	28480	08660-40002
U3†	1826-0020	5	1	IC-VOLTAGE REGULATOR TO-3	28480	1826-0020
	0340-0875	9	2	INSULATOR-XSTR THRM-CNDCT	28480	0340-0875
	2200-0113	4		SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	08660-40002	6		INSULATOR	28480	08660-40002
U4	1906-0231	2	1	DIODE-CT-RECT 200V 15A	28480	1906-0231
	0340-0875	9		INSULATOR-XSTR THRM-CNDCT	28480	0340-0875
	2200-0113	4		SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	08660-40002	6		INSULATOR	28480	08660-40002
W1	08656-60045	3	1	WIRING HARNESS, A1J1 TO A2J2	28480	08656-60045
	7120-0725	5	1	LABEL 'A1-J1'	28480	7120-0725
W2	08656-60037	3	1	WIRING HARNESS, A2J1 TO C1-8	28480	08656-60037
W3	08656-60020	4	1	CABLE, COAX,60-110MHZ A3J4 TO A8J4	28480	08656-60020
W4	08656-60039	5	1	WIRING HARNESS, A3J1 TO A7J1/C11-13 TO C15-17, 19	28480	08656-60039
W5	08656-60019	1	1	CABLE, COAX, 50MHZ, A3J5 TO A8J3	28480	08656-60019
W6	08656-60028	2	1	WIRING HARNESS, A6J1 TO A4J1	28480	08656-60028
W7	08656-60027	1	1	WIRING HARNESS, A7J2 TO A6J4/FL2, 3	28480	08656-60027
	1400-0510	8	13	CLAMP-CABLE .15-DIA .62-WD NYL	28480	1400-0510
W8	08656-20022	2	1	CABLE, SEMI-RIGID, 690-740MHZ, FL1 TO A4	28480	08656-20022
W9	08656-20019	7	1	CABLE, SEMI-RIGID, 690-740MHZ, A8 TO A4	28480	08656-20019
W10	08656-20023	3	1	CABLE, SEMI-RIGID, 800MHZ, A8 TO A6	28480	08656-20023
W11	8120-2896	0	1	CABLE, SEMI-RIGID,.1-990MHZ,A9A1J2/J2 (EXCEPT OPT. 002) INCL J2	28480	8120-2896
W11	08656-20117	6	1	CABLE-SEMI-RIGID,REAR 0.1-990MHZ W12 TO J2 (OPT. 002 ONLY;INCL J2)	28480	08656-20117
W12	08656-20116	5	1	CABLE-SEMI-RIGID,FRONT 0.1-990MHZ A9A1J2 TO W11(OPT. 002 ONLY)	28480	08656-20116
W13	08656-20021	1	1	CABLE,SEMI-RIGID,800.1-923.5MHZ,A6/A9A1	28480	08656-20021
W14	08656-20017	5	1	CABLE,SEMI-RIGID,123.5-990MHZ,A6 TO A9A1	28480	08656-20017
W15	08656-60033	9	1	WIRING HARNESS, A11J1 TO A10J1	28480	08656-60033
	7120-0724	4	1	LABEL 'A10-J1'	28480	7120-0724

See introduction to this section for ordering information
*Indicates factory selected value
† FOR BACKDATING INFORMATION REFER TO SECTION VII

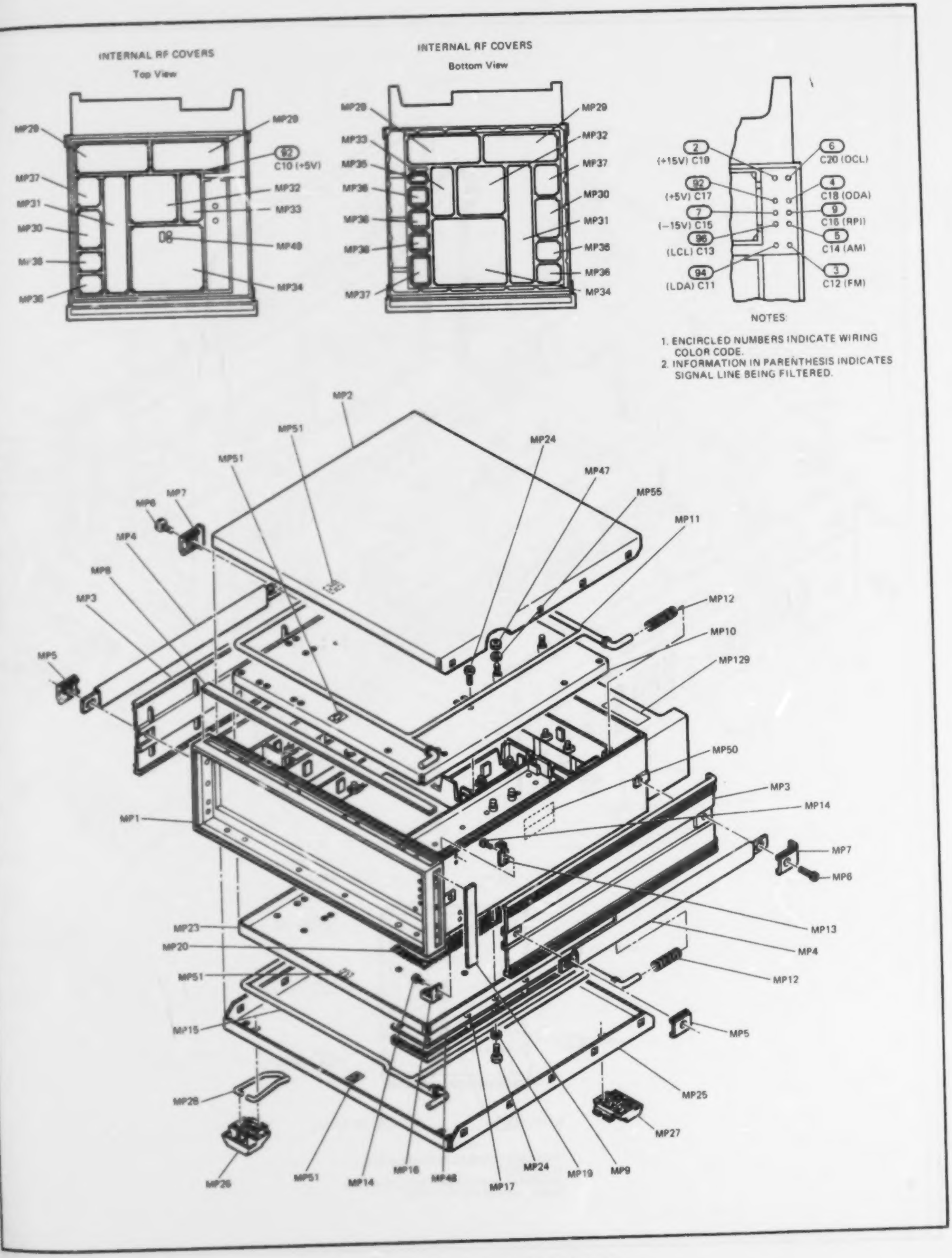
Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
W16	08656-60029	3	1	WIRING HARNESS, MAIN (EXCEPT OPT 002)	28480	08656-60029
W16	08656-60004	0	1	WIRING HARNESS,MAIN (OPT 002 ONLY)	28480	08656-60004
W17	8120-2993	0	1	CABLE, RIBBON, A10J3 TO A9A1J1	28480	8120-2993
W18	8120-2946	1	1	CABLE, RIBBON, A11J6 TO A13J1	28480	8120-2946
W19	08656-60072	6	1	WIRING HARNESS, A12J1 TO A14J1	28480	08656-60072
W20	8120-1378	1	1	CABLE, MAINS POWER	28480	8120-1378

Table 6-4. Code List of Manufacturers

Mfr Code	Manufacturer Name	Address	Zip Code
00000	ANY SATISFACTORY SUPPLIER		
0003J	NIPPON ELECTRIC CO		
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75222
01928	RCA CORP SOLID STATE DIV	SOMERVILLE NJ	08876
02114	FERROXCUBE CORP	SAUGERTIES NY	12477
03508	GE CO SEMICONDUCTOR PROD DEPT	SYRACUSE NY	13201
03888	KDI PYROFILM CORP	WHIPPANY NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85062
06001	GE CO ELEK CAP & BAT PROD DEPT	IRMO SC	29063
06383	PANDUIT CORP	TINLEY PARK IL	60477
06665	PRECISION MONOLITHICS INC	SANTA CLARA CA	95050
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW CA	94042
17856	SILICONIX INC	SANTA CLARA CA	95054
18324	SIGNETICS CORP	SUNNYVALE CA	94086
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
20932	EMCON DIV ITW	SAN DIEGO CA	92129
24046	TRANSITRON ELECTRONIC CORP	WAKEFIELD MA	01880
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
25403	AMPEREX ELEK CORP SEMICON & MC DIV	SLATERSVILLE RI	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
32293	INTERSIL INC	CUPERTINO CA	95014
32997	BOURNS INC TRIMPOT PROD DIV	RIVERSIDE CA	92507
51642	CENTRE ENGINEERING INC	STATE COLLEGE PA	16801
52763	STETTNER-TRUSH INC	CAZENOVIA NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC CT	06226
72982	ERIE TECHNOLOGICAL PRODUCTS INC	ERIE PA	16512
73138	BECKMAN INSTRUMENTS INC HELIPOT DIV	FULLERTON CA	92634
74970	JOHNSON E F CO	WASECA MN	56093
75915	LITTELFUSE INC	DES PLAINES IL	60016
80103	LAMBDA ELECTRONICS CORP	MELVILLE NY	11746
91506	AUGAT INC	ATTLEBORO MA	02703
91637	DALE ELECTRONICS INC	COLUMBUS NE	68601

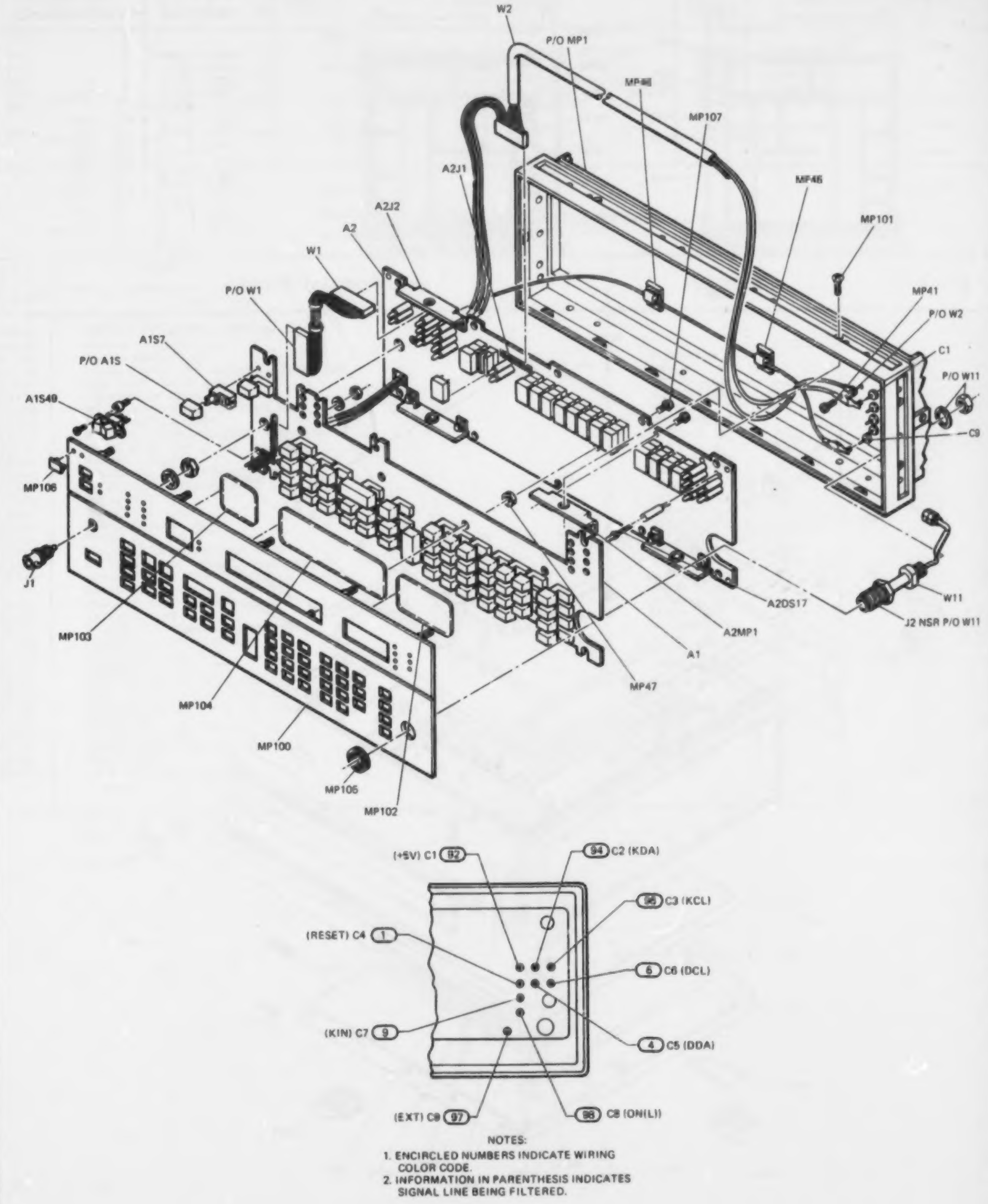
See introduction to this section for ordering information
*Indicates factory selected value


INTERNAL RF COVERS
Top View
MP29
MP29
92
C10 (+5V)
MP37
MP32
MP31
MP33
MP30
MP49
MP38
MP36
MP34
INTERNAL RF COVERS
Bottom View
MP29
MP29
MP33
MP32
MP35
MP37
MP36
MP30
MP38
MP31
MP38
MP36
MP37
MP34
2
(+15V) C19
6
C20 (OCL)
92
(+5V) C17
4
C18 (ODA)
7
(−15V) C15
9
C16 (RPI)
96
(LCL) C13
5
C14 (AM)
94
(LDA) C11
3
C12 (FM)
MP2
MP51
MP51
MP24
MP47
MP55
MP11
MP7
MP6
MP4
MP8
MP3
MP5
MP12
MP10
MP129
MP50
MP3
MP14
MP1
MP7
MP6
MP13
MP4
MP23
MP20
MP51
MP12
MP15
MP5
MP25
MP28
MP27
MP26
MP51
MP14
MP16
MP48
MP17
MP24
MP19
MP9

NOTES:

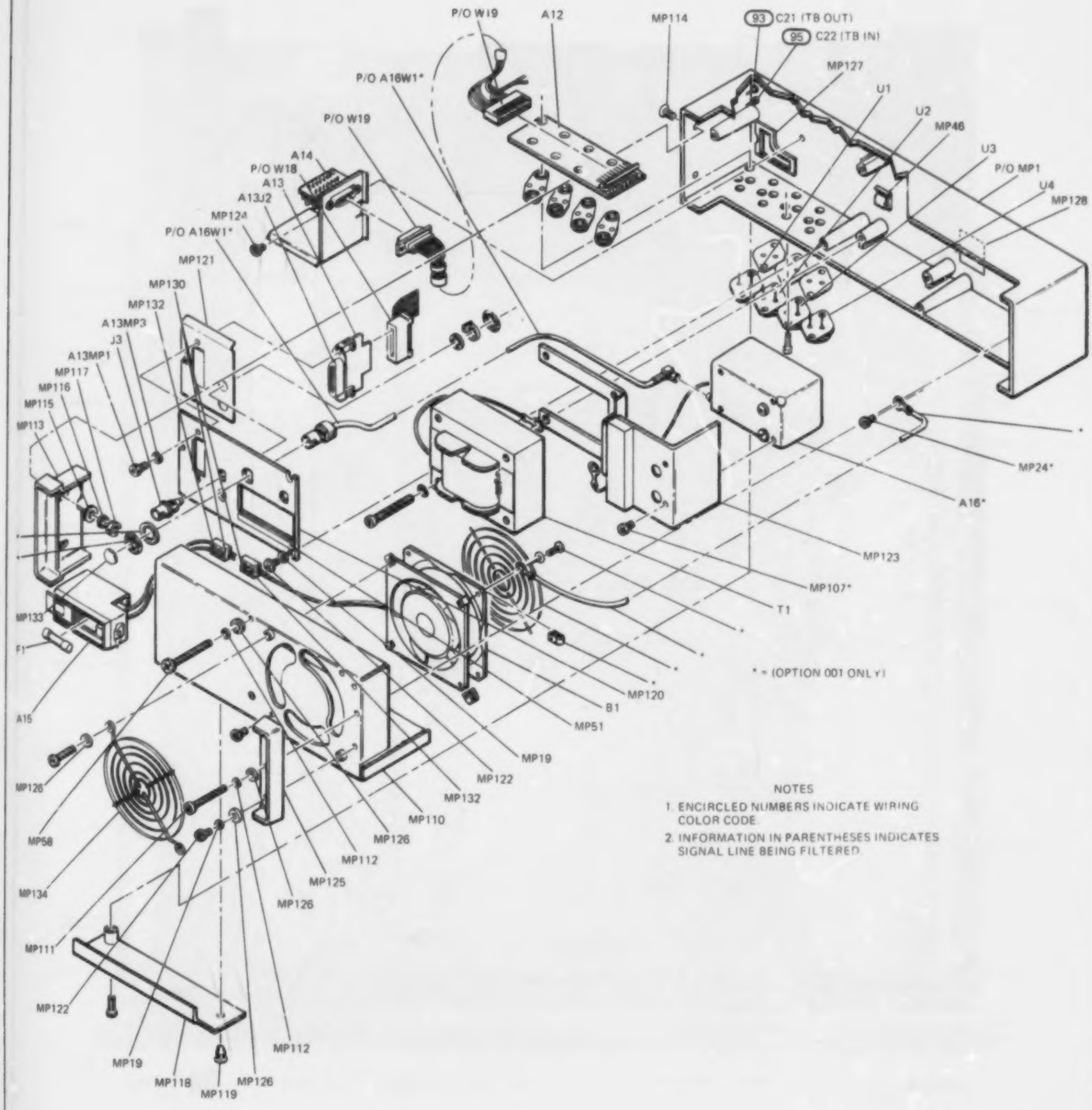
1. ENCIRCLED NUMBERS INDICATE WIRING COLOR CODE.
2. INFORMATION IN PARENTHESIS INDICATES SIGNAL LINE BEING FILTERED.

Figure 6-1. Cabinet, Parts Identification


W2
P/O MP1
MP46
MP107
MP45
MP101
MP41
P/O W2
C1
P/O W11
C9
A2J1
A2J2
A2
W1
P/O W1
A1S7
P/O A1S
A1S49
MP106
J1
MP103
MP104
MP100
MP105
MP102
MP47
A1
A2MP1
A2DS17
W11
J2 NSR P/O W11
(+5V) C1 92
94 C2 (KDA)
96 C3 (KCL)
(RESET) C4 1
6 C6 (DCL)
(KIN) C7 9
4 C5 (DDA)
(EXT) C9 97
98 C8 (ON(L))

NOTES:
1. ENCIRCLED NUMBERS INDICATE WIRING COLOR CODE.
2. INFORMATION IN PARENTHESIS INDICATES SIGNAL LINE BEING FILTERED.

Figure 6-2. Front Panel, Parts Identification


P/O W19
A12
MP114
(93) C21 (TB OUT)
(95) C22 (TB IN)
MP127
U1
U2
MP46
U3
P/O MP1
U4
MP128
P/O A16W1*
P/O W19
A14
P/O W18
A13
A13J2
MP124
P/O A16W1*
MP121
MP130
MP132
A13MP3
J3
A13MP1
MP117
MP116
MP115
MP113
MP24*
A16*
MP123
MP107*
T1
MP133
F1
A15
MP120
B1
MP51
MP19
MP122
MP132
MP110
MP126
MP112
MP125
MP126
MP126
MP58
MP134
MP111
MP122
MP19
MP118
MP119
MP126
MP112

* = (OPTION 001 ONLY)

NOTES

1. ENCIRCLED NUMBERS INDICATE WIRING COLOR CODE.
2. INFORMATION IN PARENTHESES INDICATES SIGNAL LINE BEING FILTERED.

Figure 6-3. Rear Panel, Parts Identification

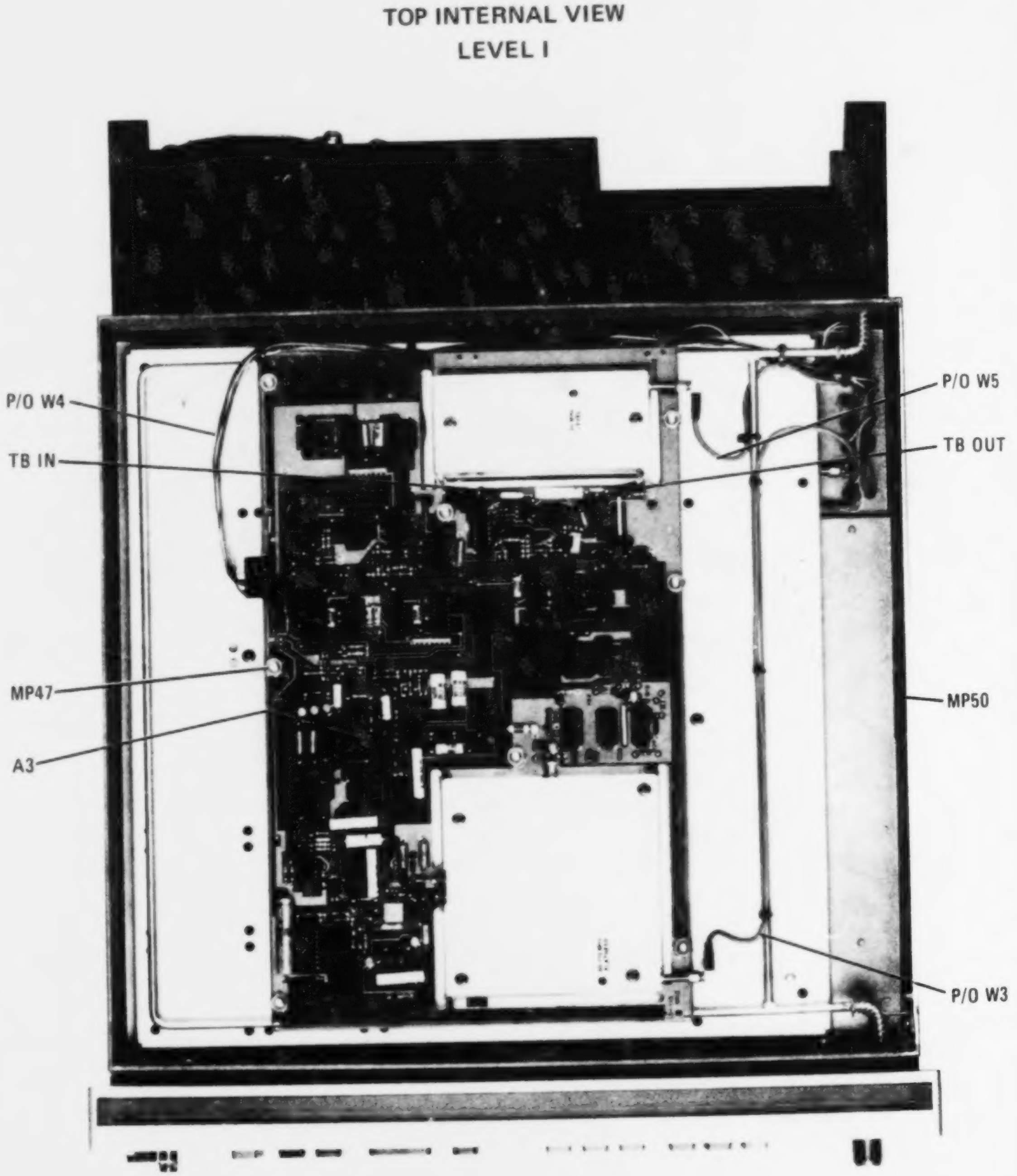

TOP INTERNAL VIEW
LEVEL I
P/O W4
TB IN
MP47
A3
P/O W5
TB OUT
MP50
P/O W3

Figure 6-4. Top Internal View; Top Cover Removed

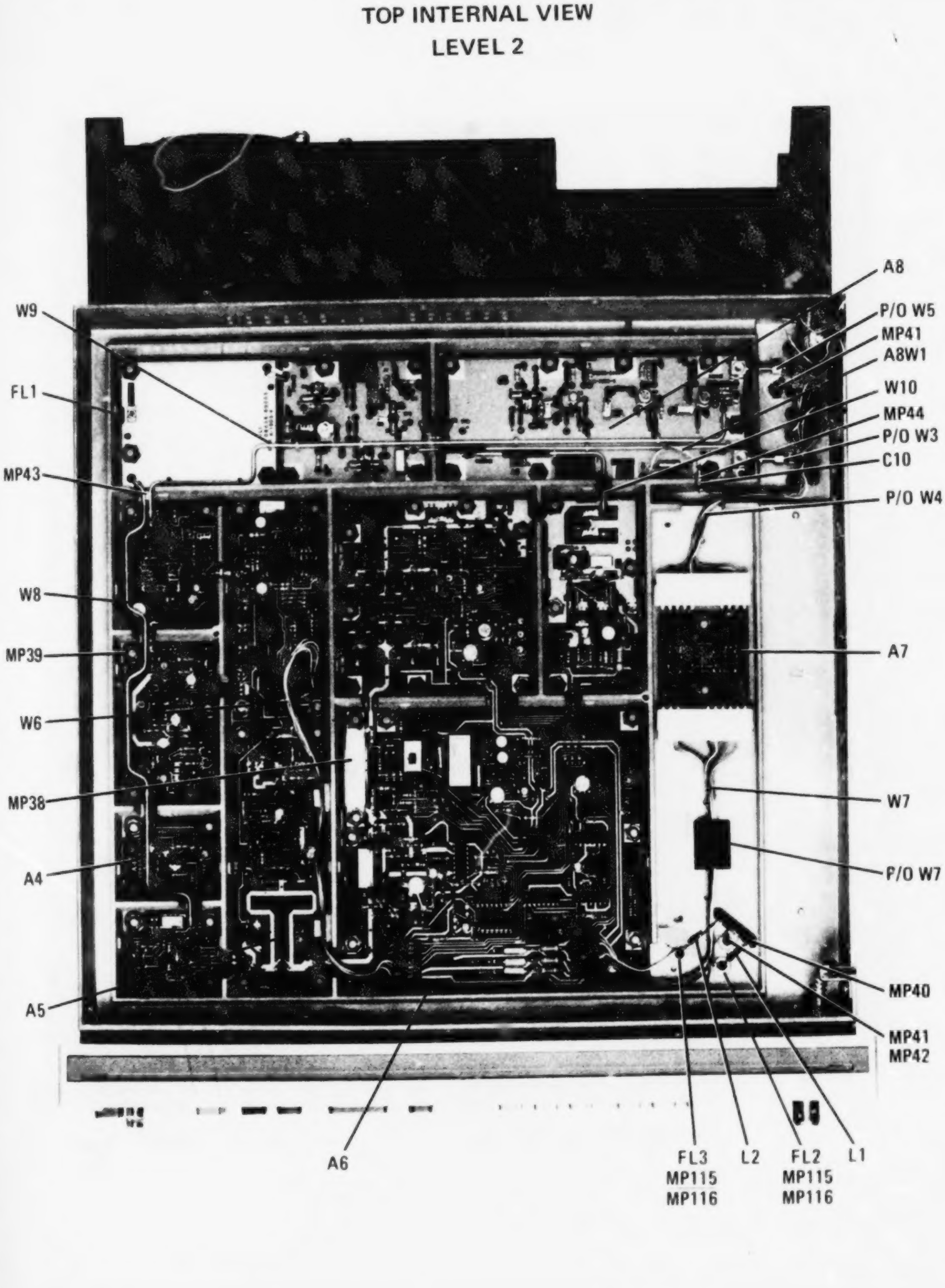

TOP INTERNAL VIEW
LEVEL 2
A8
P/O W5
MP41
A8W1
W10
MP44
P/O W3
C10
P/O W4
A7
W7
P/O W7
MP40
MP41
MP42
W9
FL1
MP43
W8
MP39
W6
MP38
A4
A5
A6
FL3
MP115
MP116
L2
FL2
MP115
MP116
L1

Figure 6-5. Top Internal View; A3 Assembly in Service Position

BOTTOM INTERNAL VIEW
LEVEL 3

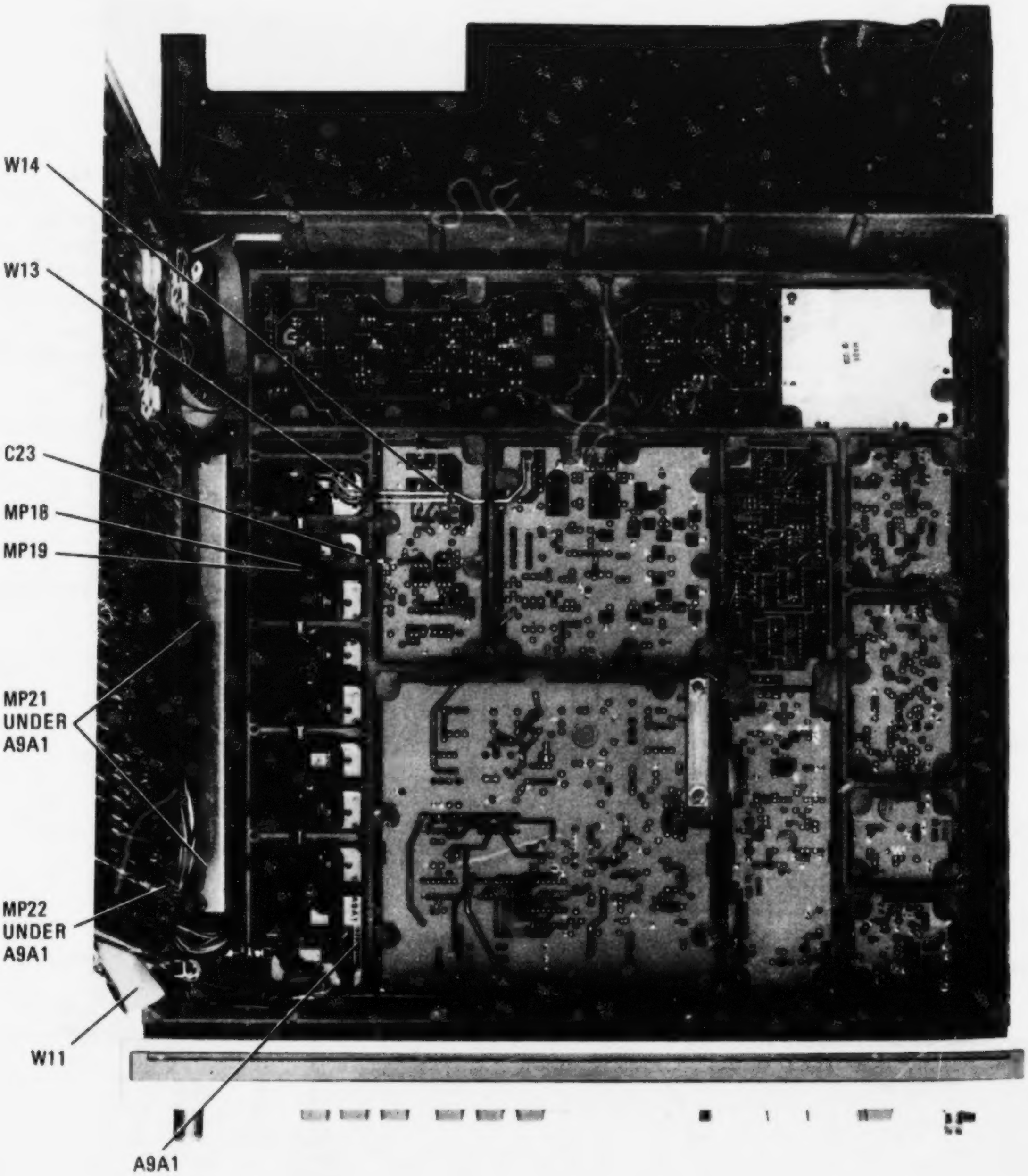

W14
W13
C23
MP18
MP19
MP21
UNDER
A9A1
MP22
UNDER
A9A1
W11
A9A1

Figure 6-6. Bottom Internal View; A10/A11 Assemblies in Service Position

BOTTOM INTERNAL VIEW
LEVEL 4

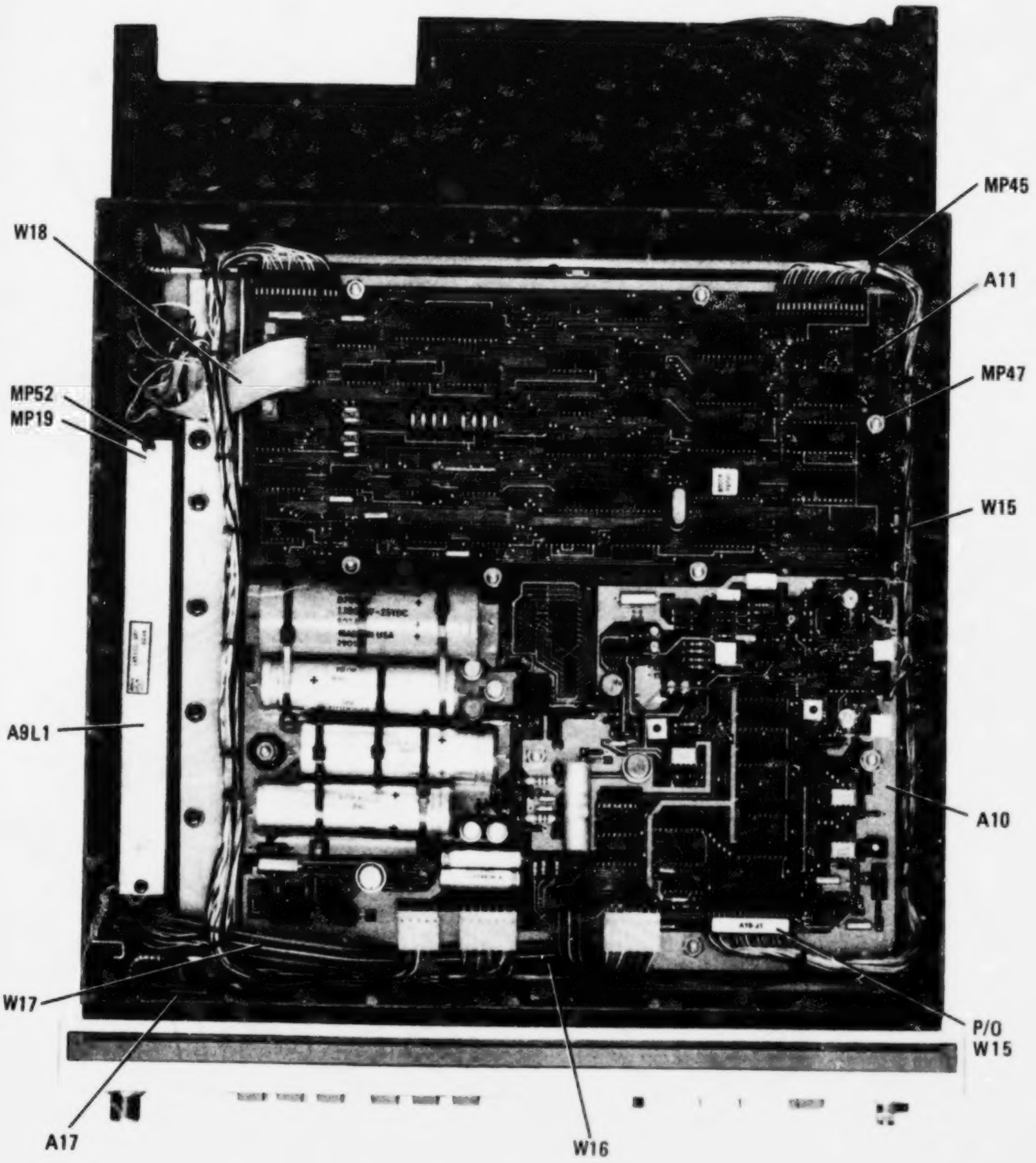

MP45
W18
A11
MP47
MP52
MP19
W15
A9L1
A10
W17
P/O
W15
A17
W16

Figure 6-7. Bottom Internal View; Bottom Cover Removed

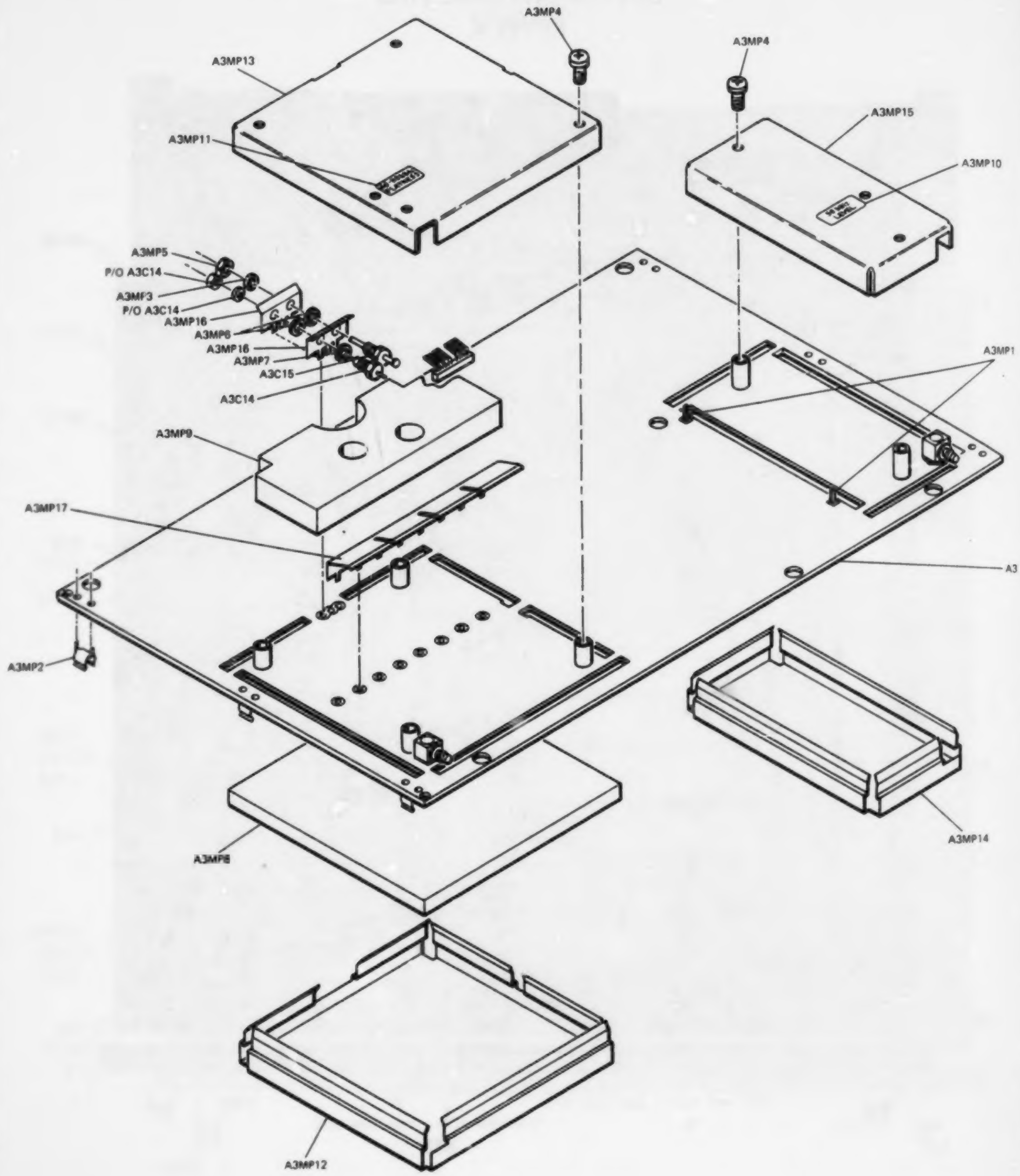

A3MP4
A3MP4
A3MP13
A3MP15
A3MP11
A3MP10
A3MP5
P/O A3C14
A3MP3
P/O A3C14
A3MP16
A3MP6
A3MP16
A3MP7
A3C15
A3C14
A3MP9
A3MP1
A3MP17
A3
A3MP2
A3MP14
A3MP8
A3MP12

Figure 6-8. Low Frequency Loop Assembly – A3, Parts Identification

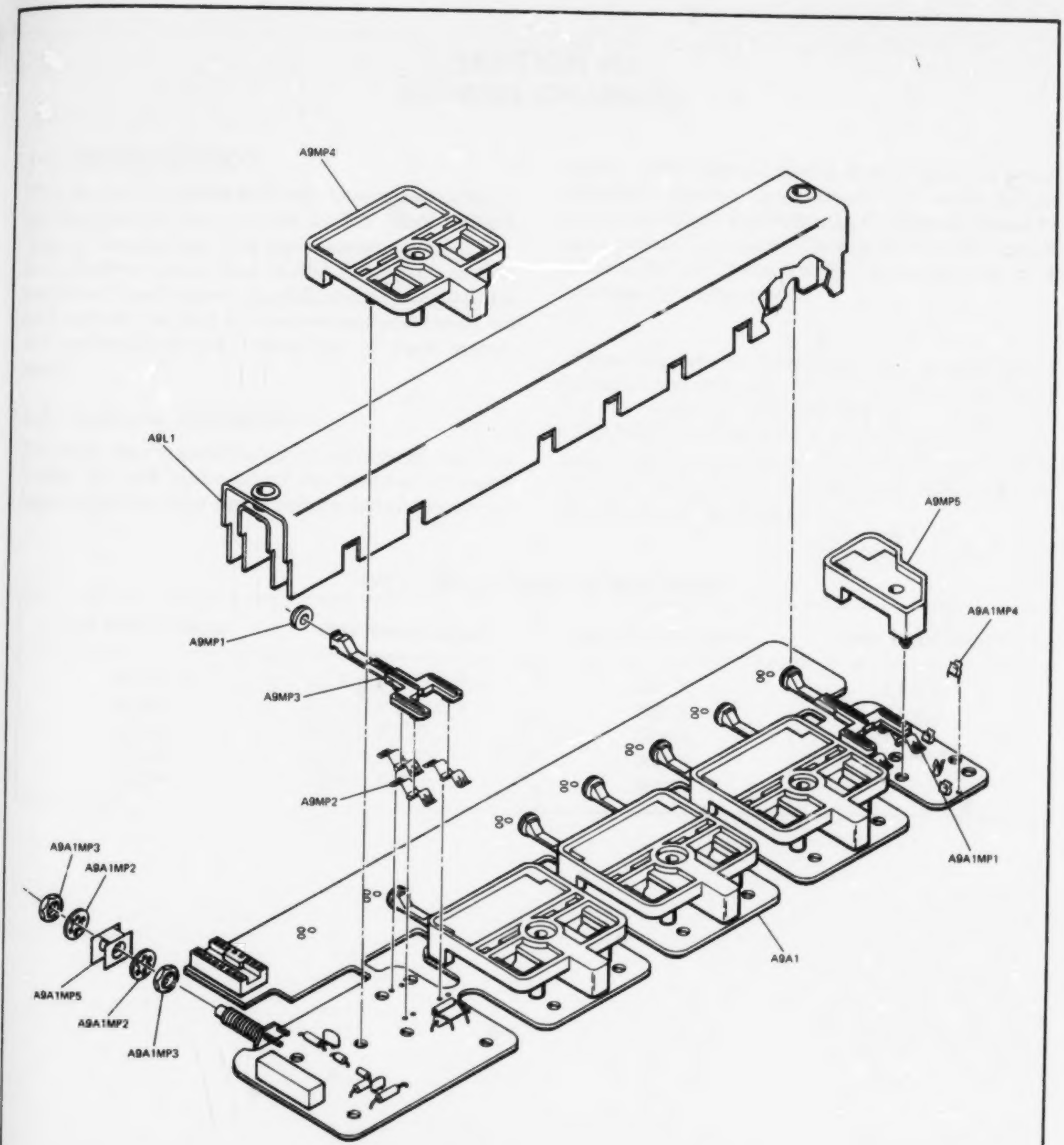

A9MP4
A9L1
A9MP5
A9A1MP4
A9MP1
A9MP3
A9MP2
A9A1MP1
A9A1MP3
A9A1MP2
A9A1MP5
A9A1MP2
A9A1MP3
A9A1

Figure 6-9. Attenuator Assembly – A9, Parts Identification

[illegible]

[illegible]

SECTION VII
MANUAL CHANGES

7-1. INTRODUCTION

This section contains manual change instructions for backdating this manual for HP Model 8656A Signal Generators that have serial number prefixes that are lower than 2035A. This section also contains instrument modification suggestions and procedures that are recommended to improve the performance and reliability of your instrument.

7-2. MANUAL CHANGES

To adapt this manual to your instrument, refer to Table 7-1 and make all of the manual changes listed opposite your instrument's serial number or prefix. The manual changes are listed in serial number sequence and should be made in the sequence listed. For example, Change A should be made after Change B; Change B should be made after Change C; etc. Table 7-2 is a summary of changes by component.

If your instrument's serial number or prefix is not listed on the title page of this manual or in Table 7-1, it may be documented in a MANUAL CHANGES supplement. For additional important information about serial number coverage, refer to INSTRUMENTS COVERED BY MANUAL in Section I of this manual.

Table 7-1. Manual Changes by Serial Number

Serial Prefix or Number	Make Manual Changes
2009A	J,I,H,G,F,E,D,C,B,A
2014A	J,I,H,G,F,E,D,C,B
2018A	J,I,H,G,F,E,D,C
2022A	J,I,H,G,F,E,D
2023A	J,I,H,G,F,E
2024A	J,I,H,G
2025A	J,I,H,F
2026A	J,H,F
2027A	J,I
2032A	J

Table 7-2. Summary of Changes by Component

Manual Change	Assemblies								
	A2	A3	A4	A6	A8	A10	A11	A17	Chassis
A				C18	C57, U1				MP23
B					C35			(*)	MP16, MP105
C							U2, U5, U6, U7, U8, U9, (**)		P/O U2, MP135
D			MP5, MP12						
E			MP7						MP29-37
F									MP10, MP23
G				C52, C59, CR5, CR7, R48					
H	(**)			CR25, CR28					
I			C34, C73, C77, R71		R11	F1			
J		L23, R118		C56					L1, L2, MP20, MP118, U1, U3

*New Assembly

**Circuit Change

MANUAL CHANGES

7-3. MANUAL CHANGE INSTRUCTIONS

CHANGE A

Table 6-3:

The components affected by this change are:

A6C18, 0160-3873, 4.7 pF
A8C57, 0160-3568, 2.7 pF
A8U1, 0955-0146, Mixer—Double Balanced
MP23, 08656-00003, Cover—Internal RF Bottom.

In each case the new part listed in Table 6-3 is the recommended replacement. Therefore no manual change is recommended. These parts may be replaced independently of the others listed in this change.

Service Sheet 3 schematic:

A8C57 originally was 2.7 pF. The part shown on the schematic is the recommended replacement. Therefore, no manual change is recommended. This part may be replaced independently of the others listed in this change.

Service Sheet 4 schematic:

A6C18 originally was 4.7 pF. The part shown on the schematic is the recommended replacement. Therefore, no manual change is recommended. This part may be replaced independently of the others listed in this change.

CHANGE B

Table 6-3:

The components affected by this change are:

A8C35, 0160-4382, 3.9 pF
A17, 08656-60087, Front Feedthru Assembly
MP16, 08656-00070, Hinge Lock-Bottom
MP105, 0590-0505, Nut-Knurled

The new parts listed in Table 6-3 for A8C35, MP16 and MP105 are the recommended replacements. For these parts no manual change is recommended. These parts may be replaced independently of the others listed in this change. Delete A17 from Table 6-3.

Service Sheet 3 schematic:

A8C35 originally was 2.7 pF. The part shown on the schematic is the recommended replacement. Therefore, no manual change is recommended. This part may be replaced independently of the others listed in this change.

Service Sheet 6 schematic:

At the MOD INPUT/OUTPUT connector J1, eliminate the A17 assembly and show the white/violet wire P/O W16 connected to C9.

Service Sheet 18 schematic:

At the KEYBOARD CLOCK input, eliminate the A17 assembly and show the white/blue wire P/O W16 connected to C3.

At the outputs on the right side of the schematic, eliminate the A17 assembly and show the wires on the right connected as follows:

1) white/yellow to C2
2) white to C7
3) white/gray to C8
4) brown to C4.

MANUAL CHANGES

MANUAL CHANGE INSTRUCTIONS (Cont'd)

CHANGE B (Cont'd)

Service Sheet 19 schematic:
At the inputs on the left side of the schematic, eliminate the A17 assembly and show the wires on the left connected as follows:

1) blue to C6
2) yellow to C5

Service Sheet 22 schematic:
At the +5V output on the right side of the schematic, eliminate the A17 assembly and show the white/red wire on the left connected to C1.

CHANGE C

Table 6-3:
The components affected by this change are:
Under U2, 1200-0043, Insulator-Thermal Conductive Transistor
A11U2, 08656-80006, ROM #1 Alternate
A11U5, 08656-80011, ROM #6 Alternate
A11U6, 08656-80010, ROM #5 Alternate
A11U7, 08656-80009, ROM #4 Alternate
A11U8, 08656-80008, ROM #3 Alternate
A11U9, 08656-80007, ROM #2 Alternate
MP135, 3150-0376, Foam Filter

In each case the new part listed in Table 6-3 is the recommended replacement. Therefore, no manual change is recommended. These parts may be replaced independently of the other parts listed in this change.

NOTES

Refer to paragraph 7-5 for information about a recommended modification to the Signal Generator involving the thermal conductive transistor insulator listed under U2.

MP135 has been deleted from Table 6-3. See paragraph 7-5 for important information concerning this part.

Service Sheet 2, Troubleshooting Using Signature Analysis:
Delete.

Service Sheet 5, Troubleshooting Using Signature Analysis:
Delete.

Service Sheet 9, Troubleshooting Using Signature Analysis:
Delete.

MANUAL CHANGES

MANUAL CHANGE INSTRUCTIONS (Cont'd)

CHANGE C (Cont'd)

Service Sheet 15 schematic:
Replace appropriate portion of schematic with the following partial schematic:

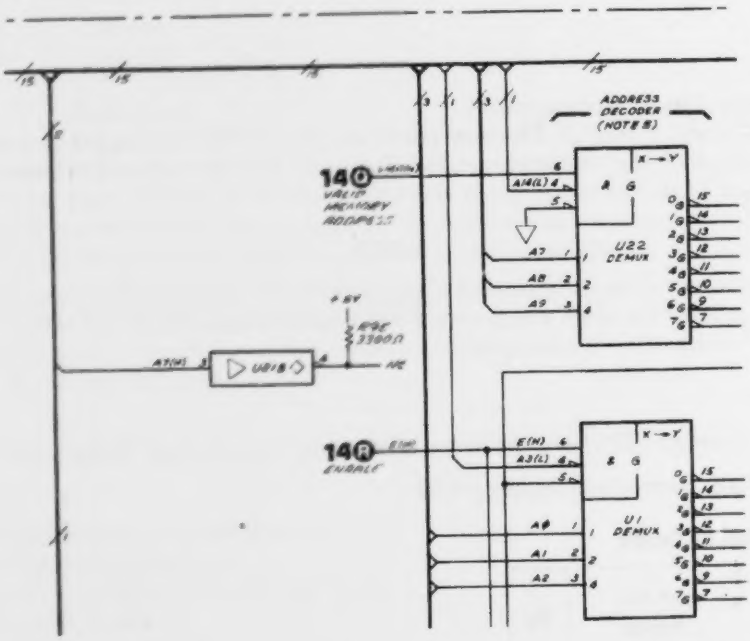

ADDRESS DECODER (NOTE 5)
14 V
VALID MEMORY ADDRESS
A14(L)
A7
A8
A9
U22 DEMUX
X→Y
& G
+5V
R95 3300Ω
A7(H)
U21B
NC
14 R
ENABLE
E(H)
A3(L)
A0
A1
A2
U1 DEMUX
15
14
13
12
11
10
9
7

Figure 7-1. Address Buffering and Decoding, Serial I/O and Control Schematic Diagram (P/O Change C)

Service Sheet 16 schematic:
The components affected by this change are:
A11U2, 08656-80006, ROM #1 Alternate
A11U5, 08656-80011, ROM #6 Alternate
A11U6, 08656-80010, ROM #5 Alternate
A11U7, 08656-80009, ROM #4 Alternate
A11U8, 08656-80008, ROM #3 Alternate
A11U9, 08656-80007, ROM #2 Alternate

In each case the new part shown on the schematic is the recommended replacement. Therefore, no manual change is recommended. These parts may be replaced independently of the others listed in this change.

Service Sheet 18, Troubleshooting Using Signature Analysis:
Delete

Service Sheet 19, Troubleshooting Using Signature Analysis:
Delete

MANUAL CHANGES

MANUAL CHANGE INSTRUCTIONS (Cont'd)

CHANGE C (Cont'd)

Service Sheet 20, Troubleshooting Using Signature Analysis:
Delete.

Service Sheet 21, Troubleshooting Using Signature Analysis:
Delete.

CHANGE D

Table 6-2:
The components affected by this change are:
A4MP5, 08656-00073 and A4MP12. The new part listed for A4MP5 is the recommended replacement. Therefore, no manual change is recommended. This part may be replaced independently of A4MP12.
Delete A4MP12 from Table 6-3.

NOTE

Refer to paragraph 7-6 for information about a recommended modification for the Signal Generator involving the High Frequency Loop Feedthrough Bracket, A4MP5.

CHANGE E

Table 6-3:
A4MP7 and MP29 through MP37 are the parts affected by this change. These parts are listed below.

A4MP7, 0624-0208, Screw-Self Tapping 6-32.

Internal RF Covers

Reference Designation	HP Part Number	Qty
MP29	08656-00018	4
MP30	08656-00019	2
MP31	08656-00020	2
MP32	08656-00021	2
MP33	08656-00022	2
MP34	08656-00023	2
MP35	08656-00024	1
MP36	08656-00025	7
MP37	08656-00026	3

In each case the new part listed in Table 6-3 is the recommended replacement. Therefore no manual change is recommended. These parts may be replaced independently of the others listed in this change. However, if one or more of MP29 through MP37 is replaced, it is recommended that MP29 through MP37 all be replaced to take full advantage of this change. Add A4MP37 to Table 6-3.

NOTE

Refer to paragraph 7-7 for information about a recommended modification for this Signal Generator involving the Internal RF Covers, MP29 through MP37.

MANUAL CHANGES

MANUAL CHANGE INSTRUCTIONS (Cont'd)

CHANGE F

Table 6-3:

MP10 and MP23 are the parts affected by this change. These parts are listed in the table below.

Signal Generator Covers

Reference Designation	HP Part Number	Qty
MP10	08656-00002	1
MP23	08656-00072	1

In each case the new part number listed in Table 6-3 is the recommended replacement. Therefore, no manual change is recommended. Each part may be replaced independently of the other. However, if one is replaced it is recommended that the other be replaced to take full advantage of the change.

NOTE

Refer to paragraph 7-7 for information about a recommended modification for this Signal Generator involving MP10 and MP23.

CHANGE G

Table 6-3:

The components affected by this change are:

A6C52 and C59, 0160-4535, 1 μF
A6CR5 and CR7, 1901-0050, Switching Diode
A6R48, 0757-0395, 61.9Ω.

In each case the new part listed in Table 6-3 is the recommended replacement. Therefore, no manual change is necessary. If either A6C52 or A6C59 as listed above is changed to the value shown in Table 6-3, replace both. If either A6CR5 or A6CR7 as listed above is changed to the value shown in Table 6-3, replace both. A6R48 may be replaced independently of the other parts listed in this change.

Service Sheet 4 schematic:

A6CR5 and CR7 were originally PIN diodes. A6R48 was originally 61.9Ω.

The new parts shown on the schematic are the recommended replacements. Therefore, no change to the manual is recommended. If either A6CR5 or A6CR7 (PIN diode) is replaced with the parts listed in Table 6-3 (switching diode), replace both. A6R48 may be replaced independently of the other components listed in this change.

Service Sheet 5 schematic:

The original values of A6C52 and C59 were 1 μF. Because the new parts are the recommended replacements, no change to the manual is recommended. If either of these parts is replaced by the value shown in Table 6-3, replace both.

MANUAL CHANGE INSTRUCTIONS (Cont'd)

CHANGE H

Table 6-3:

The following parts are affected by this change:

A6CR25 and CR28, 0122-0072, DIODE-VVC 2.2 pF 5%

In each case the new part listed in Table 6-3 is the recommended replacement. Therefore no manual change is recommended. If either of these parts is replaced by the value shown in Table 6-3, replace both. This change is independent of the accompanying circuit change.

NOTE

Refer to paragraph 7-8 for information about a recommended modification for this Signal Generator involving A6CR25 and CR28.

Service Sheet 18 schematic:

The original circuit had no connection from +5V to U18-pin 10. The circuit shown on the schematic is the recommended configuration. Therefore no manual change is recommended. This circuit change is independent of the accompanying diode change.

NOTE

Refer to paragraph 7-9 for an explanation of the recommended circuit modification and how it can be done.

CHANGE I

Table 6-3:

The components originally affected by this change are:

A4C34, 0180-0291, 1.0 μF
A4C73, 0160-0155, 0.15 μF
A4C77, 0160-2230, 3300 pF
A4R71, 0757-0442, 10kΩ
A8R11, 0698-3439, 178Ω
A10F1, 2110-0518, Fuse 3A, 125V.

In each case the new part listed in Table 6-3 is the recommended replacement. Therefore, no manual change is recommended.

NOTES

1. *If A4C34, A4C73, A4C77 and A4R71 are the values shown above, and if one or more parts are changed to the value shown in Table 6-3, they should all be changed to the values shown in Table 6-3.*
2. *A8R11 and A10F1 may be replaced independently of the others listed in this change.*

Service Sheet 1 schematic:

A4C34 was originally 2.2 μF. The part shown on the schematic is the recommended replacement. Therefore no manual change is recommended. Refer to Note 1 above.

MANUAL CHANGES

MANUAL CHANGE INSTRUCTIONS (Cont'd)

CHANGE I (Cont'd)

Service Sheet 2 schematic:

The components affected by this change are:

A4C73, 0.15 μF
A4C77, 3300 pF
A4R71, 10 kΩ.

In each case the part shown on the schematic is the recommended replacement. Therefore no manual change is recommended. Refer to Note 1 above.

Service Sheet 3 schematic:

A8R11 was originally 178Ω. The part shown on the schematic is the recommended replacement. Therefore no manual change is recommended. Refer to Note 2 above.

Service Sheet 22 schematic:

A10F1 was originally 3A. The part shown on the schematic is the recommended replacement. Therefore no manual change is recommended. Refer to Note 2 above.

CHANGE J

Table 6-3:

The components affected by this change are:

A3L23, 9140-0141, 680 nH (A3R118 shown in Table 6-3 is the direct replacement for A3L23.)
A6C56, 0121-0449, CAPACITOR-V TRMR-CER 3.5-10 pF
L1 and L2, 9100-2258, 1.2 μH
MP20, 08656-00058, Attenuator Gasket
MP118, 08656-40008, Series Regulator Cover
U1, 1826-0203, IC V RGLTR
U3, 1826-0169, IC V RGLTR.

In each case the new part listed in Table 6-3 is the recommended replacement. Therefore no manual change is necessary.

NOTES

Refer to the Heterodyne Band Accuracy and Flatness Adjustment in Section V. It may be necessary to change A6C56 to the value listed in Table 6-3 in order to make the adjustment.

If either L1 or L2 is changed from the value shown above to the value listed in Table 6-3, change the other to the value listed in Table 6-3.

MP20, MP118, U1 and U3 may be replaced independently of the other parts listed in this change. However, if U1 or U3 is changed to the value listed in Table 6-3, it is recommended that both be changed to take full advantage of the change.

Service Sheet 5 schematic:

A6C56 was originally 3.5-10 pF. The part shown on the schematic is the recommended replacement. Therefore no manual change is recommended. Refer to Note 1 above.

Service Sheet 7 schematic:

L1 and L2 were originally 1.2 μH. The parts shown on the schematic are the recommended replacement. Therefore no manual change is recommended. Refer to Note 2 above.

MANUAL CHANGES

MANUAL CHANGE INSTRUCTIONS (Cont'd)

CHANGE J (Cont'd)

Service Sheet 13 schematic:

R118 68.1Ω is the part used in place of the original L23 680 nH. Because R118 is the recommended replacement and is shown on the schematic, no manual change is recommended.

Service Sheet 22 schematic:

The original part number of U1 was 1826-0203. U3 was 1826-0875. The new part numbers shown on the schematic are the recommended replacements. Therefore no manual change is recommended. Refer to Note 3 above.

INSTRUMENT MODIFICATIONS

7-4. INSTRUMENT IMPROVEMENT MODIFICATIONS

7-5. Improving Power Supply Reliability

On instruments with serial prefixes 2018A and below, it is recommended that the thermal insulator, P/O U2, be replaced to increase reliability. Also, the Foam Filter MP135 should be removed and discarded. It may slip into the fan and stop the blade rotation.

Remove the Series Regulator Cover MP118. Refer to Figure 6-3. Remove the No. 1 Pozidriv screws that hold U2 in place. Remove U2. Replace the thermal insulator with an HP 1200-0043 (check digit 8) aluminum transistor insulator. Reinstall U2 and the Series Regulator Cover.

Loosen the screws on the External Finger Guard MP134. Refer to Figure 6-3. Pull the Foam Filter from behind the External Finger Guard. Discard the filter; tighten the screws.

7-6. Decreasing Spurious Signal Output

For an instrument that has a spurious signal at 500.5 MHz with serial prefix 2022A or below, it is recommended that a new High Frequency Loop Feedthrough Bracket A4MP5, HP 08656-00089 be installed in place of the old bracket. Refer to the paragraph entitled Disassembly Procedure in Section VIII for instructions used to gain access to the A4 Assembly. Refer to the component location diagram for the A4 Assembly (refer to Service Sheets 1 and 2) for the location of A4MP5. Unsolder A4C5, C44 and MP5 from the circuit board. Extract the bracket assembly from the circuit board casting. Insert the capacitors into the new bracket in the same relative positions. Insert the assembly into the casting and resolder the capacitors and mounting bracket. Clean the circuit board. Reassemble the instrument in the reverse order of the way it was taken apart.

7-7. Improving Low Level Accuracy

For instruments with low level RF accuracy problems, improvement may be gained by following these suggestions.

On instruments with serial prefixes 2023A and below, replace the old internal covers with those listed in the table.

Internal RF Covers

Reference Designation	HP Part Number	C D	Qty
MP29	08656-00079	4	4
MP30	08656-00080	5	2
MP31	08656-00081	8	2
MP32	08656-00082	9	2
MP33	08656-00083	0	2
MP34	08656-00084	1	2
MP35	08656-00085	2	1
MP36	08656-00086	3	7
MP37	08656-00087	4	3

Improving Low Level Accuracy (Cont'd)

Refer to the paragraph entitled Disassembly Procedures in Section VIII and Figure 6-1 for information about gaining access to the covers.

On instruments with serial prefixes 2023A and below, 2025A and 2026A, replace the old internal covers with those listed in the table.

Signal Generator Covers

Reference Designation	HP Part Number	C D	Qty
MP10	08656-00076	6	1
MP23	08656-00075	0	1

On instruments with serial prefixes 2032A and below, replace L1 and L2 with 9100-2257, 0.82 μH inductors, check digit 6. These parts are mounted near FL2 and FL3. Refer to the Disassembly procedures in Section VIII.

7-8. Improving RF Frequency Response

If the RF output level rolls off near 990 MHz on instruments with serial prefixes 2026A and below, it is recommended that diodes A6CR25 and CR28 be replaced by varactor diodes (HP 0122-0329). Refer to the Disassembly Procedures and A6 Assembly component location diagram (part of Service Sheet 4) for instructions about gaining access to these components.

7-9. Loss of Signal Generator Control by the Keyboard

Intermittent control of Signal Generator operation by the keyboard may occur on instruments with serial prefixes of 2026A and below. Furthermore, certain keys may be more prone to problems than others if this condition exists.

For instruments experiencing this problem, it is recommended that the +5V supply be connected to A2U18-pin 10. Refer to the Disassembly Procedures in Section VIII for instructions about removing the A2 Assembly.

When the A2 assembly is removed, connect a red 26 AWG wire from +5V U18 pin 16 to U18-pin 10.

SECTION VIII
SERVICE

8-1. INTRODUCTION

This section contains information for troubleshooting and repairing the Signal Generator. Included are block and circuit diagrams, principles of operation, troubleshooting tests, and repair procedures.

8-2. SERVICE SHEETS

The foldout pages in the last part of this section are the service sheets. They consist of block diagrams, circuit schematic diagrams, supplemental diagrams and associated information. For more information, refer to the paragraphs under the general heading of Troubleshooting in this section.

8-3. Block Diagrams

The block diagrams and related information are found on Service Sheets BD1 through BD4. BD1 is the overall block diagram that shows the major functional sections. BD1 serves as an index to the troubleshooting blocks and as a starting point for troubleshooting.

The troubleshooting block diagrams and related information are found on Service Sheets BD2 through BD4. Each troubleshooting block diagram shows the major circuits in their functional groupings. These blocks serve as indexes to the circuit schematic diagrams. The High Frequency Loop and Output Section is shown on BD2, the Low Frequency Loop on BD3 and the digital (control) circuits are on BD4.

8-4. Circuit Schematic Diagrams

The circuit schematic diagrams and their associated information are part of Service Sheets 1 through 22. These diagrams, in functional groupings, are aids for understanding operation and for troubleshooting the Signal Generator. Refer to the paragraphs entitled Troubleshooting for more information.

8-5. SAFETY CONSIDERATIONS

8-6. Before Applying Power

Verify that the instrument is set to match the available line voltage and that the correct fuse is installed. An uninterrupted safety earth ground must be provided from the main power source to the instrument input wiring terminals, power cord, or supplied power cord set.

8-7. Warnings and Cautions

Pay attention to WARNINGS and CAUTIONS. They must be followed for your protection and to avoid damage to the equipment.

WARNINGS

Maintenance described herein is performed with power supplied to the instrument and with the protective covers removed. Such maintenance should be performed only by service-trained personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power supplied, the power should be removed.

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnection of the protective earth terminal will create a potential shock hazard that could result in personal injury. Grounding one conductor of a two conductor outlet is not sufficient. Whenever it is likely that the protection has been impaired, the instrument must be made inoperative (i.e., secured against unintended operation).

If this instrument is to be energized via an autotransformer, make sure that the autotransformer's common terminal is connected to the earth terminal of the power source.

Capacitors inside the instrument can still be charged even if the instrument is disconnected from its source of supply.

Make sure that only 250 volt fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. Do not use repaired fuses or short-circuited fuseholders. To do so could create a shock or fire hazard.

Warnings and Cautions (Cont'd)

CAUTIONS

Do not disconnect or remove any boards in the Signal Generator unless the instrument is unplugged. Some boards contain devices which can be damaged if the board is removed when the power is on. Use conductive foam when removing MOS devices from sockets. Use care when unplugging ICs from high-grip sockets.

8-8. RECOMMENDED TEST EQUIPMENT AND ACCESSORIES

Test equipment and test accessories required to maintain the Signal Generator are listed in the table of Recommended Test Equipment in Section I. Equipment other than that listed may be used if it meets the listed critical specifications.

8-9. SERVICE TOOLS, AIDS AND INFORMATION

8-10. Service Tools

There are unique tools available that will make servicing of this instrument easier. Service aids are provided in the instrument. Service information is provided in this manual. Information provided in the paragraph entitled Repair (found in this section) shows how the instrument is accessed for repair purposes. Refer also to Figure 8-1.

Pozidriv Screwdrivers. Many screws in the Signal Generator appear to be Phillips type, but are not. To avoid damage to the screw slots, Pozidriv screwdrivers should be used. HP 8710-0899 is the No. 1 Pozidriv. HP 8710-0900 is the No. 2 Pozidriv.

Tuning Tools. For adjustments requiring nonmetallic tuning tools, use the HP 8710-0033 blade tuning tool or the HP 8710-1010 (JFD Model No. 5284) hex tuning tool. For other adjustments an ordinary small screwdriver or suitable tool is sufficient. No matter which tool is used, never force any adjustment control. This is especially critical when adjusting variable inductors or capacitors.

Heat Staking Tool. The front panel pushbutton switches have small plastic pins protruding from the back. These tabs fit through holes in the keyboard printed circuit board and are melted down to hold the switch in place. This process is known as heat staking. the heat stasking tool is a standard

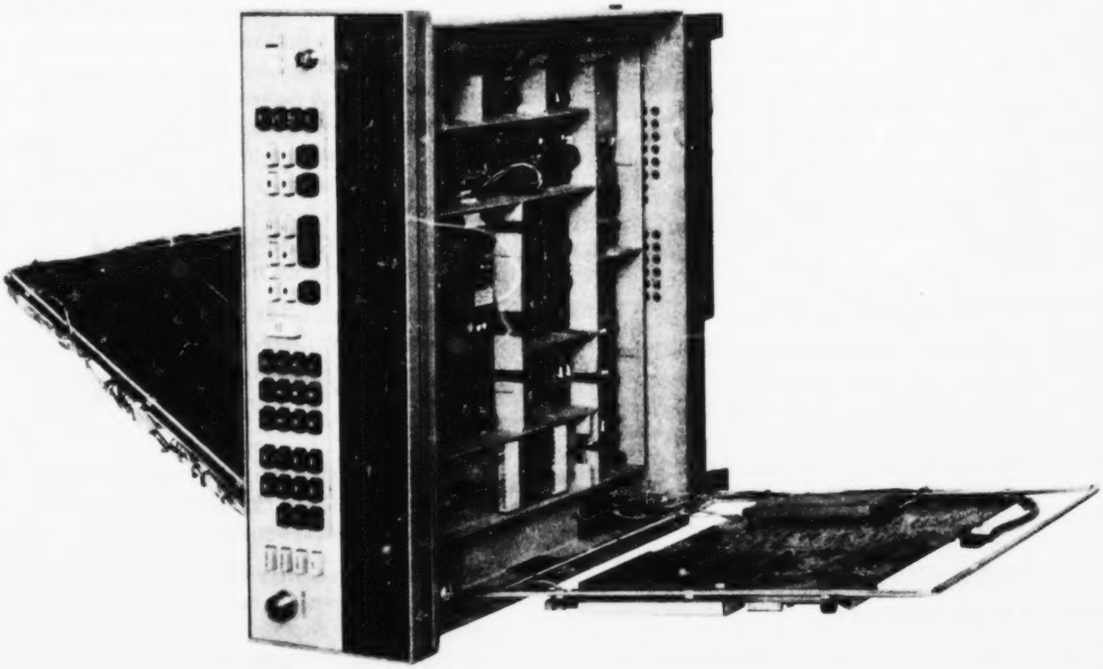


Figure 8-1. Recommended Position for Maintenance and Servicing

Service Tools (Cont'd)
soldering iron with a special tip attached (refer to Figure 8-5, under paragraphs entitled Replacement of Key Cap and Pushbutton Switches).

Refer to the paragraphs entitled Replacement of Key Cap and Pushbutton Switches under REPAIR in Section VIII for the heat staking procedure.

8-11. Assembly Locations

Assemblies in the Signal Generator are numbered sequentially, front to back, left to right, top to bottom. For example, A1 and A2 are part of the front panel assembly of the instrument.

8-12. Parts and Cable Locations

The locations of individual components mounted on printed circuit boards or other assemblies are shown adjacent to the schematic diagram on the appropriate Service Sheet. The part reference designator is the assembly designator plus the part designator. For example, A6R9 is R9 on the A6 assembly. For specific component descriptions and ordering information, refer to Table 6-3, Replaceable Parts, in Section VI. Chassis and frame parts, as well as mechanical parts and cables, are identified on Figures 6-1 through 6-5.

Major mechanical parts have reference designations that begin with the letters MP. Other mechanical parts, such as screws, are listed in the replaceable parts list below the part to which they fasten. To find the part number and description of a mechanical part, find the part in one of the figures in Section VI or Section VIII. The part in the figure will be labelled with its reference designator. Look up that reference designator in the Table of Replaceable Parts. If the part is a fastener, such as a screw, nut, or washer, look to the figure for the part to which it fastens. Then, look up the fastened part in the parts list. Just below it you will see the part numbers and description of the desired hardware.

Illustrated parts breakdowns of chassis and frame parts, as well as assemblies and mechanical parts and cables, can be identified on Figues 6-1 through 6-9. Parts breakdowns of the front and rear panels are located on Figures 6-2 and 6-3.

8-13. Test Points and Adjustment Locations

Most test points and adjustments are indicated on individual circuit board assemblies. Test points and adjustments can also be found on the component locator photograph adjacent to the assembly's schematic diagram.

8-14. Service Aids on Printed Circuit Boards

Service aids on printed circuit boards include test points, indicator lights, transistor and integrated circuit and relay designations, adjustment names, and assembly part numbers. Of particular importance are the three test LEDs on the A10 Audio/Power Supply Assembly.

8-15. Other Service Documents

Service Notes, Manual Change Supplements, and other service literature are available through Hewlett-Packard. For further information, contact your nearest Hewlett-Packard office.

3-16. TROUBLESHOOTING

8-17. General

Instrument problems usually fall into three general categories: operator errors, operation out of specification and catastrophic failures. The troubleshooting strategy is different for each category. For more information refer to the table of Specifications in Section I and the detailed operating instructions found in Section III.

Operator Error. Apparent failures sometimes result from operator errors. These may take one of several forms. The operator may allow external influences which affect instrument operation. At times he may attempt to operate the instrument in an "out of specification" mode. Under certain circumstances the Signal Generator allows the out of specification operation. Under other conditions it doesn't.

A reverse power level of greater than 0.2 watts (3 volts) coupled to the front panel RF connector will cause an apparent failure. There is no output signal and the Amplitude display flashes. This, however, is normal operation under the circumstances. The instrument has temporarily disconnected itself from the high power level that could do damage to internal circuits. To bring the instrument back to its normal operating mode, remove the high reverse power at the RF output connector and enter a new output power level at the front panel.

NOTE

The Reverse Power Protection provided by this circuit is adequate up to 50 watts (50 volts).

The Signal Generator does allow out of specification operation at frequencies below 0.1 MHz. The

TROUBLESHOOTING (Cont'd)

frequency is accurate but other specifications, such as RF output power level may be incorrect.

Not-allowed operation is generally indicated by displays that flash or default to the last valid entry. An example of the former is a flashing FM display that occurs when the frequency is changed to a range that will not allow wide deviation. To stop the flashing display, press the FM mode select button. This will change the FM deviation to a level that is acceptable.

Examples of not-allowed operation where the Signal Generator defaults to the last valid entry are: selecting an RF output level that is too high or selecting an AM depth that causes the maximum total RF output power level to be too high.

Instrument Out of Specification. If it is suspected that the instrument's operating parameters are out of tolerance, the Abbreviated Performance Tests table in Section IV tells which test may be performed to verify proper operation. This table may also be used to determine which assembly requires adjusting and on what service sheet the adjustable components are located. The Post-Repair Adjustments table in Section V tells which adjustments are related and may also require adjustment. After adjustments are complete, perform the performance test(s) in Section IV. If the performance is still out of tolerance, refer to the troubleshooting information. Although the problem may be solved very quickly by going to the service sheet where the adjustment is located, it is good practice to begin with the overall troubleshooting information found on Service Sheet BD1.

Catastrophic Failures. When a catastrophic failure occurs, begin troubleshooting on Service Sheet BD1. The information there is used to quickly isolate the problem to one of the three major sections of the instrument.

8-18. Strategy

Troubleshooting for the Signal Generator is organized into three levels. The overall troubleshooting level is where problems are isolated to the power supply or one of the functional sections. The functional section level of troubleshooting isolates the malfunction to the circuit level. At the circuit level, the problem is isolated to a stage within the circuits shown on the schematic. It is expected that further troubleshooting, to the component level, depends on the skill and experience of the troubleshooter.

8-19. Overall Troubleshooting (Service Sheet BD1)

Overall troubleshooting begins with verifying that the power-on sequence occurs properly. At this point, power supply problems become evident. The effect of inputs from the keyboard and an external computer are compared. It is possible to separate a digital or analog problem at this level. Digital problems are usually referred to Service Sheet BD4. Further troubleshooting determines which analog (phase lock) loop is defective. Problems here are referred to Service Sheet BD2 or BD3. If none of the sections or circuits above are defective, further troubleshooting isolates a malfunction in the special circuits.

8-20. Functional Section Troubleshooting (Service Sheets BD2-BD4)

Troubleshooting of the loop sections (Service Sheets BD2 and BD3) is done primarily from an analog viewpoint with the intent of isolating a malfunction to the circuit level. The digital section (Service Sheet BD4) continues with troubleshooting from Service Sheet BD1 but with the intent of isolating the problem to the circuit level.

8-21. Circuit Troubleshooting (Service Sheets 1-22)

The goal of troubleshooting at the previous service sheet level is to be confident that the problem is within the circuits shown by the schematic. Because of the interaction of circuits in the Signal Generator, it may be necessary to refer to other service sheets to completely isolate a problem. Some of the circuits that are mostly analog have digital control circuits. In these cases, troubleshooting the digital circuits first is offered as an alternative.

When the problem is isolated to a stage, the ability of the one doing the troubleshooting is utilized to isolate the defective component.

8-22. Signature Analysis

Signature analysis is a simple method of verifying the operation of digital circuitry. When properly used, signature analysis can detect extremely subtle hardware faults. Signatures must identically match those given in the signature tables located opposite the schematics. If everything is working correctly, signatures will all match exactly. If they don't match, by even one digit, something is wrong.

With the Generator's internal signature analysis routine, the signature analyzer's test probe is used

Signature Analysis (Cont'd)

to check nodes in the circuit under test. The signature analyzer converts the signals at the node into a four digit "signature", which it displays. The signature is then compared to the signature in the troubleshooting checks adjacent to the appropriate schematic. These two signatures must be identical.

Signature analysis can be speeded up if the following considerations are kept in mind:

1. Make sure that every step is performed as described in the set-up procedure. That is, make sure that the clock, start, and stop connections and triggering are correct.
2. Double-check that the signatures are being taken at the correct node.
3. Make sure that the signature analyzer probe is making good contact with the pin being checked. Oxidation on pins can cause invalid signatures due to poor contacts.
4. When you think that you have found a bad signature, double check to make sure.
5. When checking a node, check that the unstable-signature indicator is not blinking.

8-23. Additional Information

Additional troubleshooting information may be found in various locations in the manual. Reference is made to the information in the appropriate troubleshooting procedure. Examples of this information are the Power-On Sequence, the Basic Functional Checks and the HP-IB Functional Checks which are all found in Section III.

8-24. REPAIR

8-25. Disassembly Procedures

For the most part, disassembling the Signal Generator is quite straightforward. Most of the procedures simply indicate the size, number, type and general location of the mounting hardware. Where it is necessary, the procedures are more detailed. Table 8-1 indicates which procedure will give access to a particular assembly and which figure shows the location of a particular assembly. Reference to the appropriate exploded view in Section VI is included. If a circuit board within the main casting is to be removed from the Signal Generator, seek access to its component (top) side. To reassemble the Signal Generator, follow the procedures in the reverse order.

WARNING

Before beginning any disassembly procedure, be sure that the line (Mains) voltage is disconnected.

CAUTION

DO NOT REMOVE the circuit boards mounted on the casting unless absolutely necessary. With repeated reassembly, the Pal nut cuts new threads in the boss. It then becomes impossible to tighten the Pal nut to provide an effective ground.

Front Panel Removal. Remove the knurled nut MP105 from the RF Output connector with a pair of soft jawed pliers (HP part number 8710-0986). Remove the top trim MP8 and four No 2 Pozidriv screws MP101 from the top and bottom edge of the front panel casting. Pull the front panel forward with the BNC connector until it is free of the casting.

A1 Keyboard and A2 Display Assembly Removal. The front panel has already been removed. Place the front panel face down. To free the A2 Assembly, remove fourteen 4-40 machine screws MP107 from the back of the circuit board with a No 2 Pozidriv screwdriver. Unsolder the front panel switch and BNC connector wires and remove them from the cable clamp MP46 on the casting wall. Remove the cable connectors at A2J1 and A2J2.

CAUTION

During reassembly, be sure that you reconnect A2J1 and J2 correctly. It is possible to reverse the connectors. For reference, the second pins of both connectors are connected to yellow wires while the fourth pins are connected to blue wires. The pin numbers are etched on the circuit board.

Remove the A1 assembly by first removing the eleven 10-32 hex nuts MP47 which hold the assembly in place. Lift the assembly from the mounting lugs.

Cover Removal, Top and Bottom (Levels 1 and 4 Access). Set the Signal Generator in its normal operating position. Free the handles and side covers by removing four No. 2 Posidriv screws MP6.

Table 8-1. Assembly Access Information

To Gain Access to an Assembly or Module	Perform Procedure(s)	For Disassembly Information Refer to Figure(s)
A1 and A2	Front Panel Removal and, if required, A1 Keyboard and A2 Display Assembly Removal	6-2
A3 (top)	Cover Removal, Top (Level 1 Access)	6-1, 6-4, 6-8
A3 (top and bottom)	Cover Removal, Top (Level 1 Access) A3 Assembly Service Position	6-1, 6-4, 6-8, 8-1
A4, A5, A6, A7, A8 (top), A9A1 (bottom) and FL1, FL2, FL3, L1, L2	Cover Removal, Top (Level 1 Access) A3 Assembly Service Position Level 2 Access	6-1, 6-4, 6-5, 8-1 (A9 Only) 6-9
A4, A5, A6, A8 (bottom) A9A1 (top) and A9L1	Cover Removal, Bottom (Level 4 Access) A10/A11 Assemblies Service Position Level 3 Access	6-1, 6-6, 6-7, 8-1
A10 and A11 (top) A17	Cover Removal, Bottom (Level 4 Access)	6-1, 6-7
A10 and A11 (top and bottom)	Cover Removal, Bottom (Level 4 Access) A10/A11 Assemblies Service Position	6-1, 6-7, 8-1
A12, A13, A14, A15	Rear Panel Removal	6-3, 8-2
A16, B1, T1	Fan Shroud Removal	6-3, 8-2

Disassembly Procedures (Cont'd)

Remove the front and rear handle caps (MP5 and MP7) and the handles MP4. Push the side covers toward the Signal Generator's rear panel to release the angled tabs that fit into the holes in the top and bottom covers. Remove the side covers. The top cover may now be lifted off for Level 1 Access or the instrument may be turned over and the bottom cover lifted off for Level 4 Access.

A3 Assembly Service Position. The top cover has been removed. Remove eight 10-32 inch nuts and washers (MP47 and MP55) from the top of the circuit board. Rotate the circuit board and the hinged carrier MP11 up and to the right. To lock the carrier in place, press the spring loaded hinge toward the rear of the instrument until it slides around the hinge lock MP13.

Level 2 Access. Remove two No 2 Pozidriv screws MP24 from the top internal cover. Lift the cover up and out by the cover handles. Place a standard blade screwdriver under the corner of the small internal RF cover which covers the individual board. Lift the cover from the casting.

NOTES

Insert all shield braid removed during disassembly into the appropriate space(s) in the casting wall before the small internal RF covers are reinstalled.

Disassembly Procedures (Cont'd)

NOTES (Cont'd)

DO NOT PRESS the small internal RF covers all the way into the casting during reassembly. Make sure the top of the cover is the same level as the top of the casting.

A10/A11 Assemblies Service Position. The bottom cover has been removed. Remove eleven 10-32 nuts and associated washers (MP47 and MP55) from the top of the circuit board. Raise the circuit board and hinged carrier MP15 up and to the left. To lock the carrier in place, press the spring loaded hinge toward the rear of the Signal Generator until it slides around the hinge lock MP13.

Level 3 Access. A10/A11 Assemblies have been locked into the service position. Remove seven No 2 Pozidriv screws MP24 from the bottom internal cover. Remove twelve sets of No 2 Pozidriv screws and washers (MP56 and MP57) from the attenuator cover. Lift the attenuator cover off the bottom internal cover. Lift the bottom internal cover up and out by the cover handles. Access to individual boards is achieved by raising the corners of the small internal RF covers with a standard blade screwdriver.

NOTE

DO NOT PRESS the small internal RF covers all the way in. Make sure the top of the cover is the same level as the top of the casting.

Rear Panel Removal. Position the instrument so you are facing the rear panel as shown in Figure 8-2.

1. Free the left rear foot (item 1) by removing two sets of No 2 Pozidriv screws, washers, lockwashers and nuts (items 2).
2. Free the Rear Panel (item 4) by removing three sets of No 2 Pozidriv screws and lockwashers (items 3).
3. Pull the rear panel toward yourself. Be careful not to pinch the black wire.
4. Remove the flat ribbon cable connector from the HP-IB Connector Assembly—A13.

CAUTION

While reinstalling the rear panel, be sure the thin wall metal gasket MP121 is not twisted or bent against the top, bottom or side of the machined frame (casting) MP1.

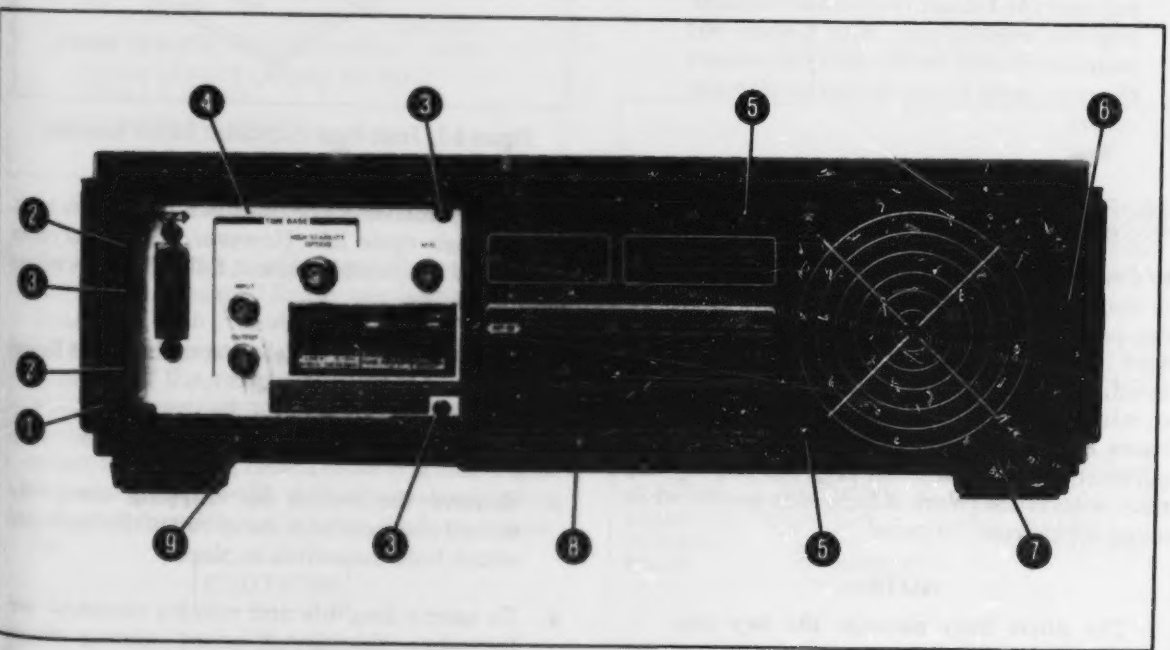


Figure 8-2. Rear-Panel and Fan Shroud Removal

Disassembly Procedures (Cont'd)

5. While reinstalling the rear panel, reverse the steps of the preceding procedure.

Fan Shroud Removal. Position the instrument on either side.

1. Remove the plastic pin (item 3) that attaches the series regulator cover (item 9) to the Fan Shroud (item 7). (Refer to Figure 6-3).
2. Position the instrument so you are facing the rear panel as shown in Figure 8-2.
3. Free the fan shroud (item 7) by removing three sets of attaching hardware. Two sets are No 2 Pozidriv screws, lockwashers and flatwashers (item 5). The other set is a No 2 Pozidriv screw, lockwasher and flatwasher (item 6).

NOTE

Removing the transformer will free the bracket holding the Option 001 10 MHz Reference Oscillator if it has been installed.

CAUTION

Be sure that none of the wires within this assembly are crushed between the casting and the transformer while reinstalling the transformer. With Option 001 installed, it may be necessary to remove the rear panel to ensure that no damage occurs.

8-26. Replacement of Key Cap and Pushbutton Switches

Key Cap Replacement. Removing a front-panel key cap may be easily done in one of two ways. If the front panel has been removed (refer to the Front Panel Removal procedure), use a small flat blade screwdriver to press on the switch side of the key cap while working it from side-to-side with your fingers. Removing the key cap without opening the instrument is done as follows. Grasp the key cap firmly with pliers. Work it from side-to-side while pulling away from the panel.

NOTE

The pliers may damage the key cap unless the jaws are covered with a protective material.

Be sure the key cap is aligned properly before snapping into place. Note that the key cap has 8 possible positions. Refer to Figure 8-3.

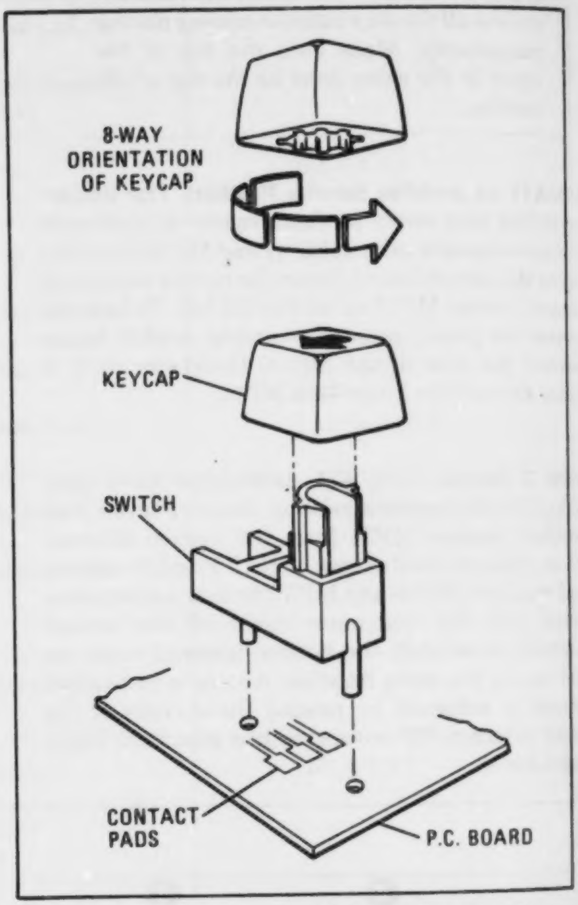


Figure 8-3. Front-Panel Pushbutton Switch Assembly

Switch Replacement. The front-panel switches have a very high cycle life. However, if one becomes faulty and needs replacement, follow the procedure outlined below:

1. Remove the front panel (refer to the Front Panel Removal Procedure).
2. Remove the key cap as indicated above.
3. Remove the switch by chipping away the melted plastic tabs at the circuit of the keyboard which hold the switch in place.
4. To assure long life and reliable electrical performance, the circuit board contact traces (which are found underneath the switch) should

Disassembly Procedures (Cont'd)

be clean and free of surface imperfections. Clean the switch contact pads before installing a new switch.

5. For reliable operation, any method of assembly must assure that the switch is mounted tightly against the pc board. To facilitate the heat staking operation, specially molded support anvils (HP 5040-6881) can be ordered. Refer to Figure 8-4.

NOTE

The following operation should be done in a well ventilated area. If the heat staking tip is too hot, the plastic will vaporize and emit fumes. These fumes, however, are non-toxic.

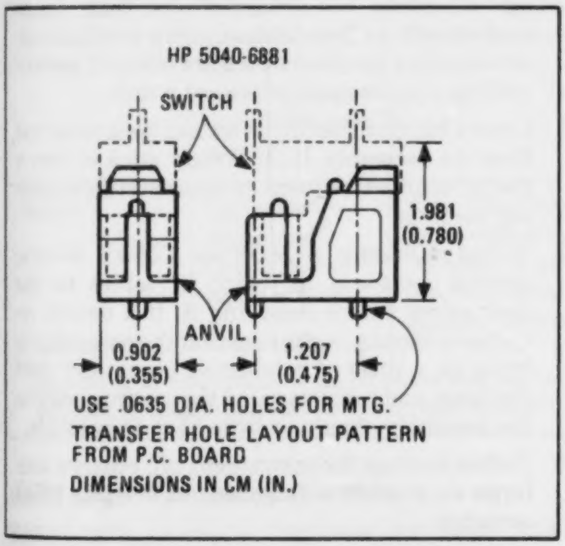

HP 5040-6881
SWITCH
1.981
(0.780)
ANVIL
0.902
(0.355)
1.207
(0.475)
USE .0635 DIA. HOLES FOR MTG.
TRANSFER HOLE LAYOUT PATTERN
FROM P.C. BOARD
DIMENSIONS IN CM (IN.)

Figure 8-4. Pushbutton Switch Support Anvil

6. To assure proper switch assembly, verify that the switch is pushed firmly against the circuit board and, with the hot (440C or 825°F) staking tip (refer to Figure 8-5) push down on each of the posts (2) of the switch. Each post should take about one second to stake. With the proper cycle, the post should turn a darker color and, in about ten seconds, return to its original bright red color. The correctly staked post should have a smooth round "rivet" like top. Refer to Figure 8-6.

CAUTIONS

Do not disturb the assembly for at least 10 seconds after heat staking.

If not enough heat is applied, the plastic will tend to stick to the tip of the iron.

If too much heat is applied, the plastic will fume profusely, the "rivet" will be irregularly shaped, and the plastic will be permanently discolored.

If the staking tool is worn or flaked, it will cause a misshaped rivet and/or a contamination deposit on the surface.

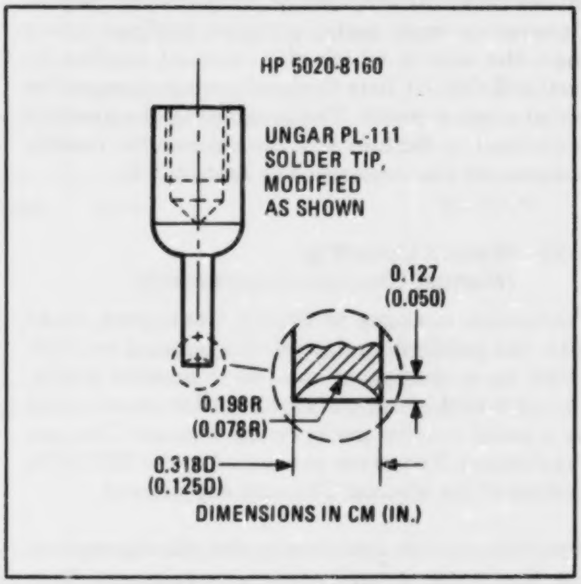

HP 5020-8160
UNGAR PL-111
SOLDER TIP,
MODIFIED
AS SHOWN
0.127
(0.050)
0.198R
(0.078R)
0.318D
(0.125D)
DIMENSIONS IN CM (IN.)

Figure 8-5. Heat Staking Tip

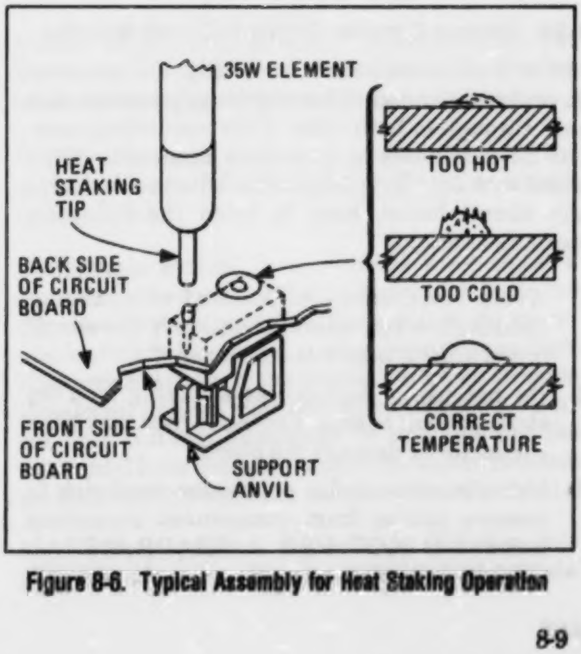

35W ELEMENT
HEAT
STAKING
TIP
BACK SIDE
OF CIRCUIT
BOARD
FRONT SIDE
OF CIRCUIT
BOARD
SUPPORT
ANVIL
TOO HOT
TOO COLD
CORRECT
TEMPERATURE

Figure 8-6. Typical Assembly for Heat Staking Operation

8-27. Factory-Selected Components (*)

Some component values are selected at the time of final checkout at the factory (see Table 5-1). These values are selected to provide optimum compatibility with associated components. These components are identified on individual schematics and the parts list by an asterisk (*).

8-28. Manual Backdating (†)

A dagger (†) by an item of service information means that information is different for Signal Generators with serial number prefixes lower than the one to which this manual applies directly. Table 7-1 lists the backdating changes by serial number prefix. The backdating changes are contained in Section VII. Recommended modifications are also contained in Section VII.

8-29. Manual Updating (Manual Changes Supplement)

Production changes to Signal Generators made after the publication date of this manual are indicated by a change in the serial number prefix. Changes to this manual's information are recorded by a serial number prefix on the Manual Changes supplement. Errors are also noted in the ERRATA portion of the Manual Changes supplement.

Keep this manual up to date by periodically requesting the latest, complimentary supplement from your Hewlett-Packard office.

8-30. Etched Circuits (Printed Circuit Boards)

The etched circuit boards in the Signal Generator have plated-through holes which make a solderable path through to both sides of the insulating material. Soldering can be done from either side of the board with equally good results. When soldering to any circuit board, keep in mind the following recommendations:

1. Avoid unnecessary component substitution. Substitution can result in damage to the circuit board and/or adjacent components.
2. Do not use a high-power soldering iron on etched circuit boards. Excessive heat may lift a conductor or damage the board.
3. Use a suction device or wooden toothpick to remove solder from component mounting holes. DO NOT USE A SHARP METAL OBJECT SUCH AS AN AWL OR TWIST DRILL FOR THIS PURPOSE. SHARP OBJECTS MAY DAMAGE THE PLATED-THROUGH CONDUCTOR. Refer to Table 8-2 for information on available tools for working on etched circuit boards.

8-31. MOS and CMOS Integrated Circuit Replacement

MOS and CMOS integrated circuits are used in this instrument. They are prone to damage from both static and transients and must be handled carefully. When working on the Signal Generator, keep in mind the following recommendations to avoid damaging these sensitive components.

1. Do not remove any board unless the Signal Generator has been unplugged.
2. When removing a socketed MOS or CMOS device from an assembly, be careful not to damage it. Avoid removing devices from these sockets with pullers. Instead, use a small screwdriver to pry the device up from one end, slowly pulling it up one pair of pins at a time.
3. Once a MOS or CMOS device has been removed from an assembly, immediately stick it into a pad of conductive foam or other suitable holding medium.
4. When replacing a MOS or CMOS device, ground the foam on which it resides to the instrument before removing it. If a device requires soldering, make sure that the assembly is lying on a sheet of conductive foam, and that the foam and soldering iron tip are grounded to the assembly. Apply as little heat as possible.
5. Before turning the instrument off, remove any large ac sources which may be driving MOS switches.

8-32. RETROFITTING OPTION 001

Option 001 may be retrofitted to the Signal Generator after taking delivery. Refer to Section I for the descripton and part numbers under the paragraphs entitled Options.

8-33. SCHEMATIC SYMBOLOGY AND OPERATING PRINCIPLES

8-34. Schematic Diagram Notes

Table 8-3, which just precedes the foldouts, summarizes the symbology used for presenting the devices used in the Signal Generator.

8-35. Basic Logic Symbology

The logic symbols used in this manual are based on the American National Standards Institute (ANSI)

Table 8-2. Etched Circuit Soldering Equipment

Item	Use	Specification	Item Recommended	HP Part No.
Soldering Tool	Soldering, Heat Staking	Wattage: 35W Tip Temp.: 390—440°C (735—825°F)	Ungar No. 135 Ungar Division Eldon Ind. Corp. Compton, CA 90220	8690-0167
Soldering Tip	Soldering, Unsoldering	*Shape: Chisel	*Ungar PL113	8690-0007
Soldering Tip	Heat Staking	Shape: Cupped	HP 5020-8160 or modified Ungar PL111 (see Figure 8-2)	5020-8160
De-Soldering Aid	To remove molten solder from connection	Suction Device	Soldapullt by Edsyn Co., Van Nuys, CA 91406	8690-0060
Rosin (flux) Solvent	To remove excess flux from soldered area before application of protective coating	Must not dissolve etched circuit base board	Freon	8500-0232
Solder	Component replacement; Circuit Board repair wiring	Rosin (flux) core, high tin content (63/37 tin/lead), 18 gauge (SWG) 0.048 in. diameter preferred.		8090-0607

*For working on circuit boards; for general purpose work, use No. 555 Handle (8690-0261) and No. 4037 Heating Unit 47-1/2—56-1/2 W (HP 8690-0006); tip temperature of 850—900°F, and Ungar No. PL113 1/8" chisel tip.

Basic Logic Symbology (Cont'd)

Y32.14-1973, "Graphic Symbols for Logic Diagrams (Two State Devices)". A summary of this symbology is provided to aid in interpreting these symbols.

Gates and Qualifiers. This section includes a brief description of the basic logic symbols used on the service sheets (see Figure 8-7), a summary of indicator symbols (see Figure 8-8), a discussion of contiguous blocks, control blocks, and dependency notation, and a summary of symbology for some of the more complex devices.

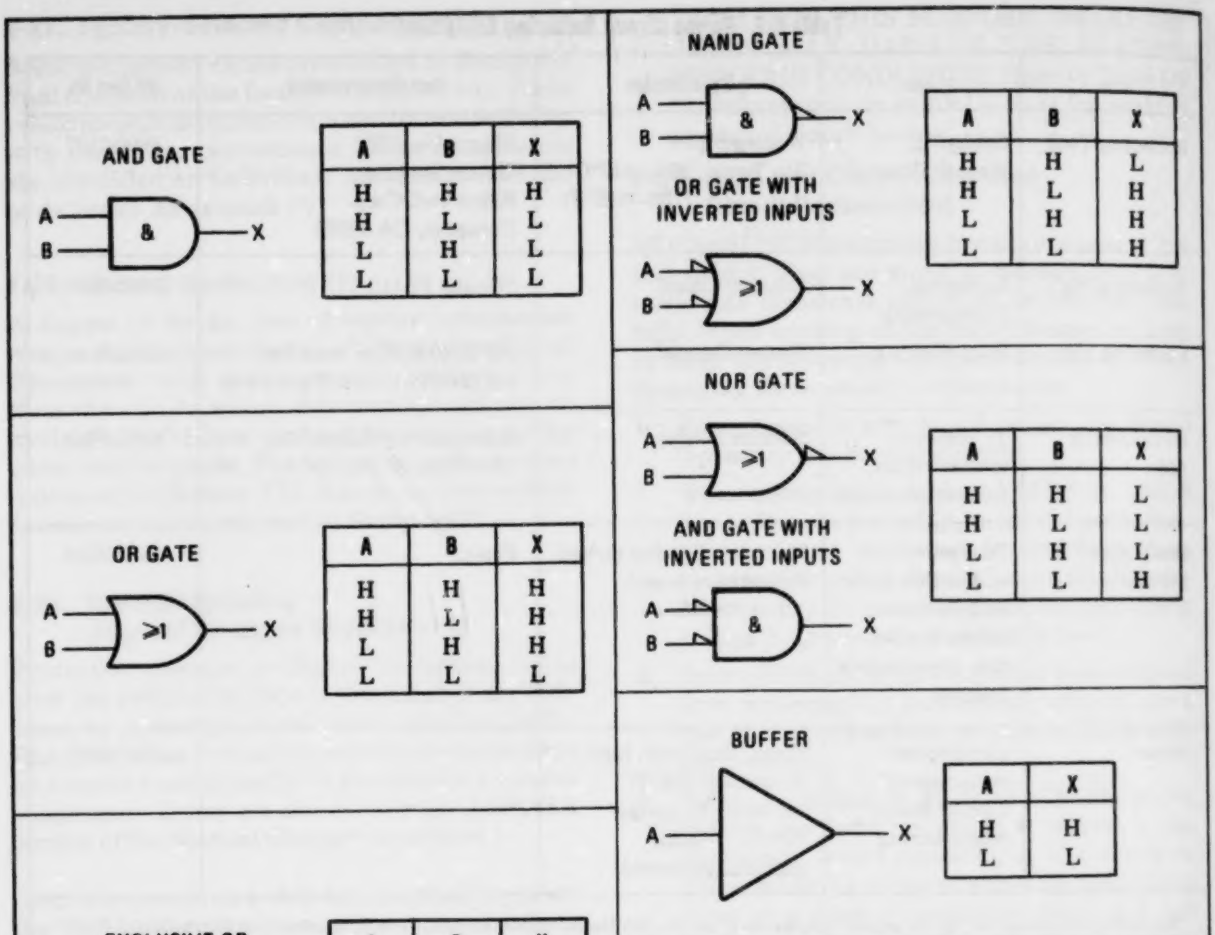
Qualifiers are that portion of a device symbol that denotes the logic function. For example, "&" denotes the AND function. See Figure 8-7 for a summary of the basic logic symbols and their qualifiers.

Power supply and ground connections are not shown on the symbols. This information is tabulated on the right margins of the service sheets.

Indicator Symbols. Indicator symbols identify the active state of a device's input or output, as shown in Figure 8-8.

Contiguous Blocks. Two symbols may share a common boundary parallel or perpendicular to the direction of the signal flow. Note that in the examples shown in Figure 8-9, there is generally no logic connection across a horizontal line, but there is always an implied logic connection across a vertical line. Notable exceptions to this rule are the horizontal lines beneath control blocks and between sections of shift registers and counters (dividers).

Dependency Notation. Dependency Notation simplifies symbols for complex integrated circuit ele-


A
B
&
X
≥1
=1
A
X
INPUTS
&
+V
EXTERNAL
PULL-UP
RESISTOR
ECL
EXTERNAL
PULL-DOWN
RESISTOR
-V

AND GATE

A	B	X
H	H	H
H	L	L
L	H	L
L	L	L

OR GATE

A	B	X
H	H	H
H	L	H
L	H	H
L	L	L

EXCLUSIVE-OR GATE

A	B	X
H	H	L
H	L	H
L	H	H
L	L	L

OPEN COLLECTOR OUTPUTS (TTL)

NAND GATE

OR GATE WITH INVERTED INPUTS

A	B	X
H	H	L
H	L	H
L	H	H
L	L	H

NOR GATE

AND GATE WITH INVERTED INPUTS

A	B	X
H	H	L
H	L	L
L	H	L
L	L	H

BUFFER

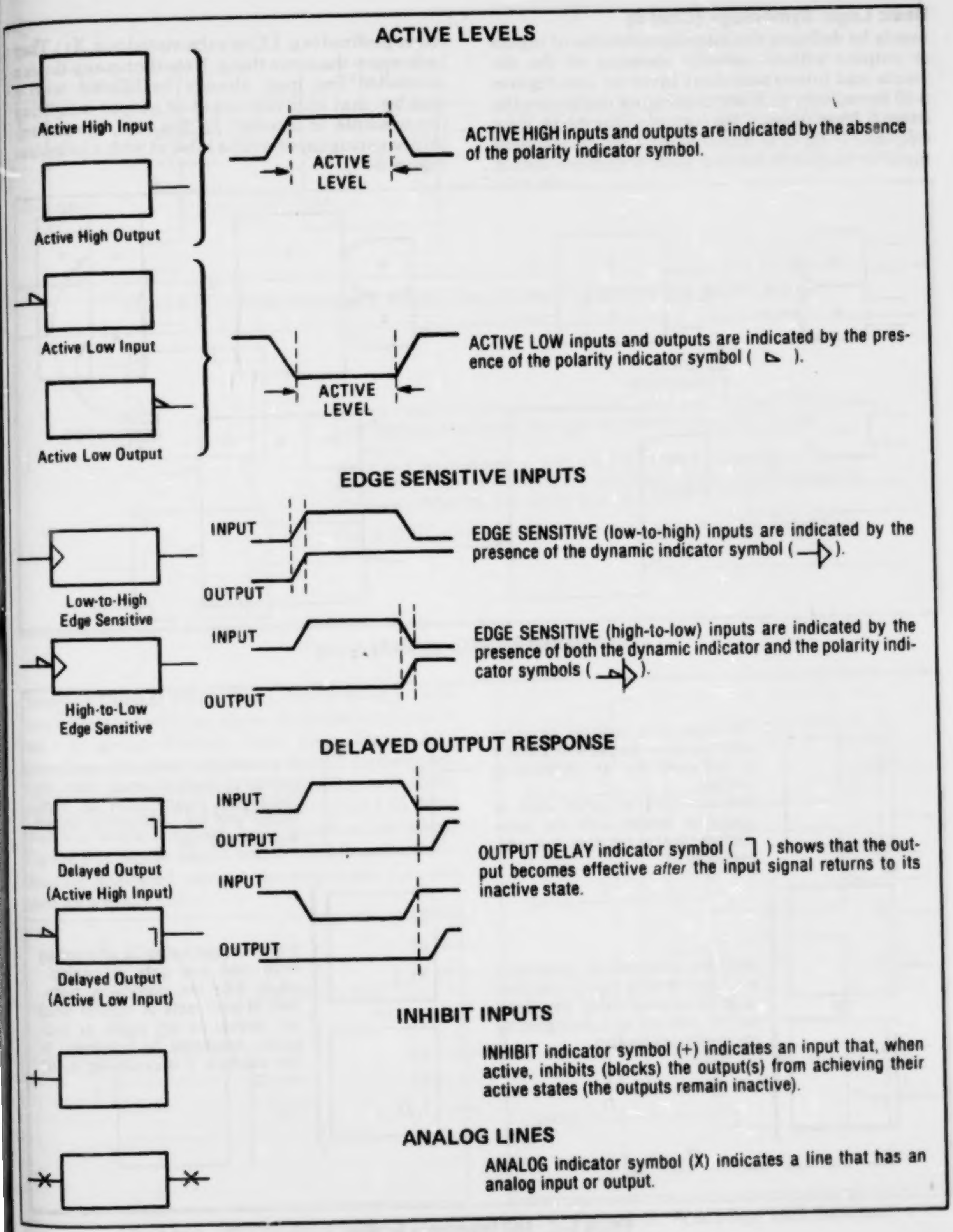
A	X
H	H
L	L

INVERTER

A	X
H	L
L	H

OPEN EMITTER OUTPUTS (ECL)

Figure 8-7. Basic Logic Symbols and Qualifiers


Active High Input
Active High Output
ACTIVE LEVEL
Active Low Input
Active Low Output
ACTIVE LEVEL
INPUT
OUTPUT
Low-to-High Edge Sensitive
INPUT
OUTPUT
High-to-Low Edge Sensitive
INPUT
OUTPUT
Delayed Output (Active High Input)
INPUT
OUTPUT
Delayed Output (Active Low Input)

ACTIVE LEVELS

ACTIVE HIGH inputs and outputs are indicated by the absence of the polarity indicator symbol.

ACTIVE LOW inputs and outputs are indicated by the presence of the polarity indicator symbol (▻).

EDGE SENSITIVE INPUTS

EDGE SENSITIVE (low-to-high) inputs are indicated by the presence of the dynamic indicator symbol (—▷).

EDGE SENSITIVE (high-to-low) inputs are indicated by the presence of both the dynamic indicator and the polarity indicator symbols (▻▷).

DELAYED OUTPUT RESPONSE

OUTPUT DELAY indicator symbol (⌉) shows that the output becomes effective *after* the input signal returns to its inactive state.

INHIBIT INPUTS

INHIBIT indicator symbol (+) indicates an input that, when active, inhibits (blocks) the output(s) from achieving their active states (the outputs remain inactive).

ANALOG LINES

ANALOG indicator symbol (X) indicates a line that has an analog input or output.

Figure 8-8. Indicator Symbols

Basic Logic Symbology (Cont'd)

ments by defining the interdependencies of inputs or outputs without actually showing all the elements and interconnections involved (see Figures 8-10 through 8-12). The following examples use the letter A for address, C for control, G for AND, V for OR, and F for free dependencies. The dependent input or output is labeled with a number that is either prefixed (e.g. 1X) or subscripted (e.g. X_1). They both mean the same thing. Note that many times a controlled line may already be labeled with a number that indicates input or output weighting (for example, in a coder). In this case, the controlling or gating input will be labeled with a letter (see Figure 8-11).

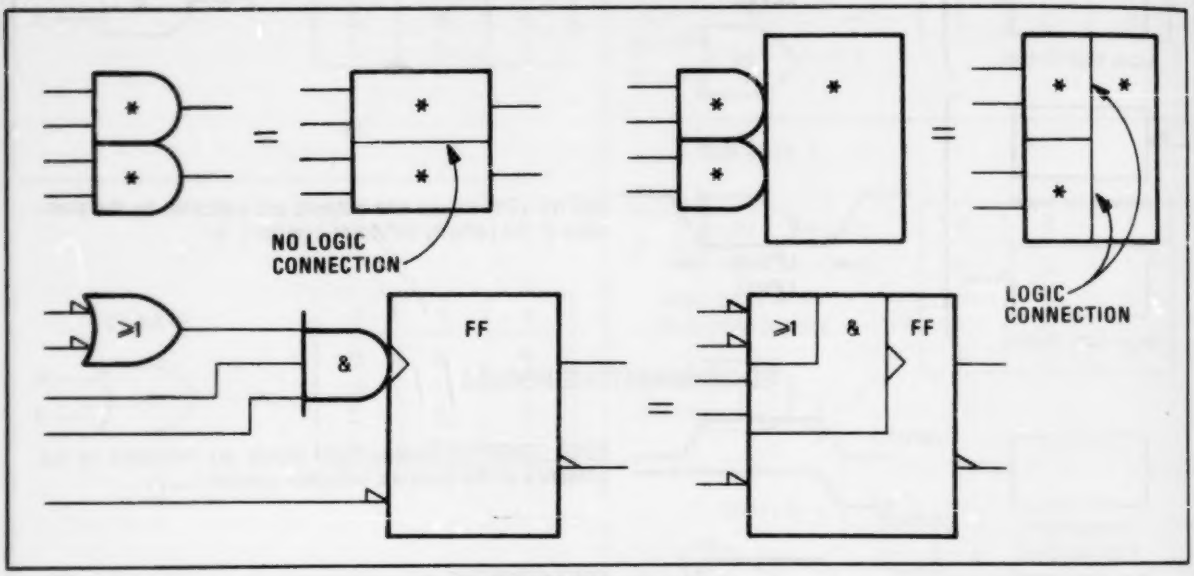
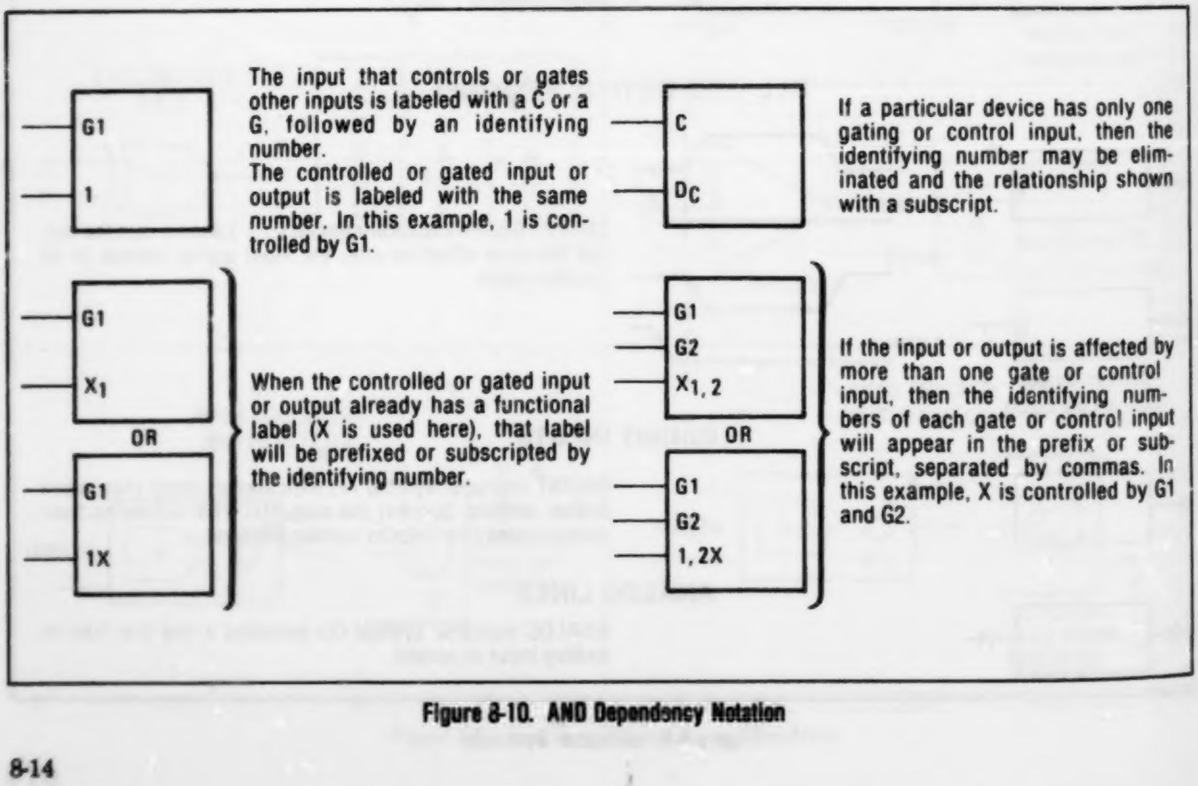


Figure 8-9. Contiguous Blocks



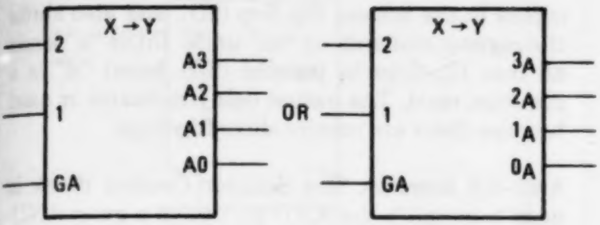
The input that controls or gates other inputs is labeled with a C or a G, followed by an identifying number. The controlled or gated input or output is labeled with the same number. In this example, 1 is controlled by G1.

If a particular device has only one gating or control input, then the identifying number may be eliminated and the relationship shown with a subscript.

When the controlled or gated input or output already has a functional label (X is used here), that label will be prefixed or subscripted by the identifying number.

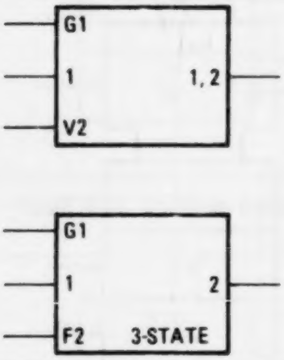
If the input or output is affected by more than one gate or control input, then the identifying numbers of each gate or control input will appear in the prefix or subscript, separated by commas. In this example, X is controlled by G1 and G2.

Figure 8-10. AND Dependency Notation



When GA is active, the active address line (0 through 3) is the decoded value of the 1 and 2 binary inputs. When the controlled address lines have a functional value, that value will be prefixed or subscripted by the identifying letter.

Figure 8-11. Address Dependency Notation: Coder Example Using Alpha Characters (Letters)



When a V input is active, the output will be in its active state. With the V input inactive, the device functions as if the V input doesn't exist.

When an F input is active, the output is enabled to function normally. When an F input is inactive, the output becomes a high impedance, effectively removing that device from the circuit.

The 3-STATE label is sometimes used with the free dependency notion.

Figure 8-12. OR and Free Dependency Notation

Common Control Block. The Control block is used in conjunction with an array of related symbols in order to group common logic lines. Figure 8-13 shows how the Control block is usually represented. Figure 8-14 shows a quad D-type flip-flop with reset. This can be redrawn as shown in Figure 8-15. Note that the more complex representation shown in Figure 8-14 can be used when the flip-flops are functionally scattered around the schematic (i.e., not used as a quad unit).

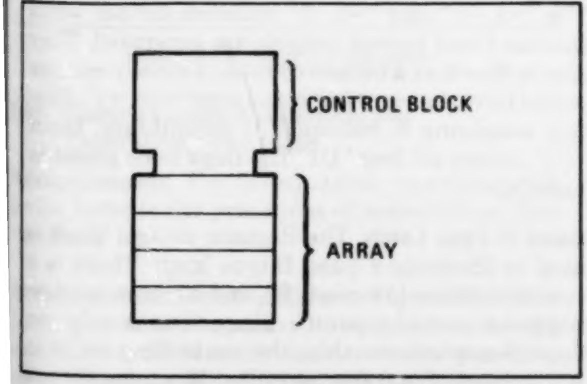


Figure 8-13. Common Control Block

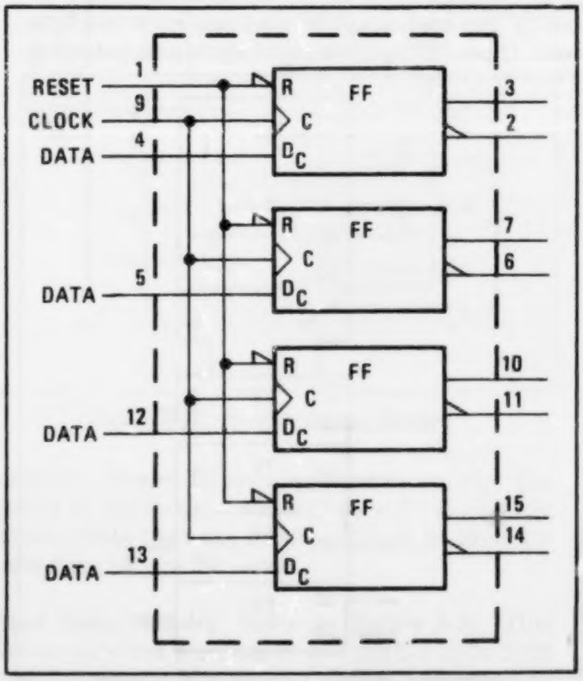


Figure 8-14. Quad D-Type Latch (Individual)

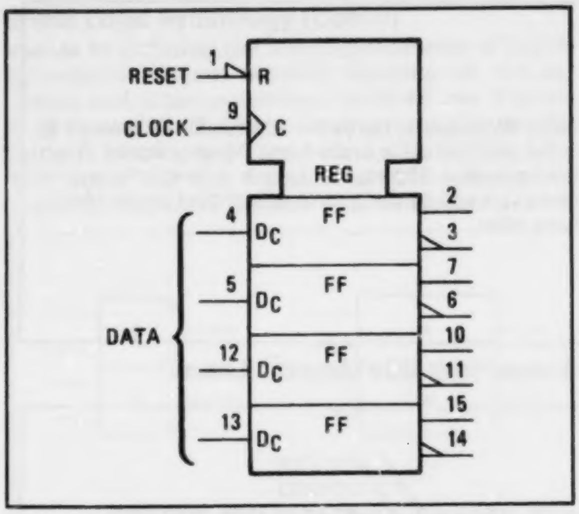


Figure 8-15. Quad D-Type Latch (Combined)

Complex Device Symbology. Figures 8-16 through 8-19 show how the basic symbols can be combined to illustrate behavior of fairly complex devices.

Shift Register. The Shift Register Control Block is used to show common inputs to a bidirectional shift register. Notice that "→ m" means shift the contents to the right or down by "m" units. And "← m" means shift the contents to the left or up by "m" units. Note: If m = 1, it may be omitted. Inputs "a" and "b" are each single IC pins that have two functions. Input "a" enables one of the inputs to the top D-type flip-flop (1D) and also shifts the register contents down "m" units. Input "b" enables one of the inputs to the bottom flip-flop (2D), and also shifts the register contents up "m" units. Input "c" loads all four flip-flops in parallel (3D). Input "d" is a common reset. The output delay indicator is used because these are master-slave flip-flops.

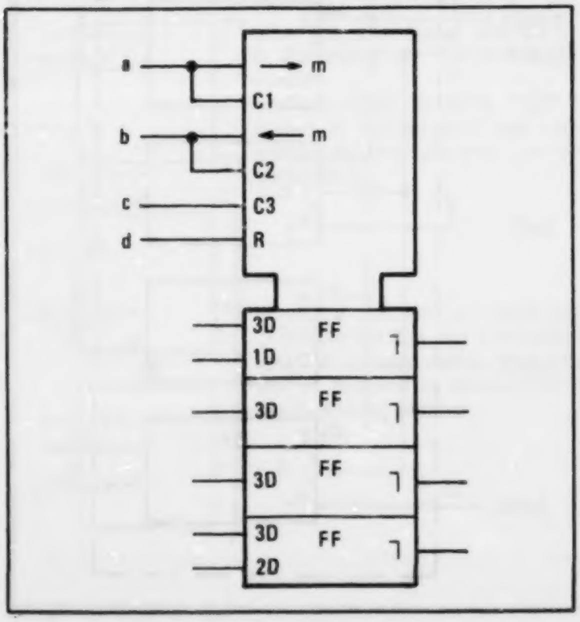


Figure 8-16. Shift Register

AND-OR Selector. The Selector Control Block is used to simplify the AND portion of a quad AND-OR select gate. When G1 is high, the data presented at the "1" inputs will be gated through. When G2 is high, the data presented at the "2" inputs will be gated through.

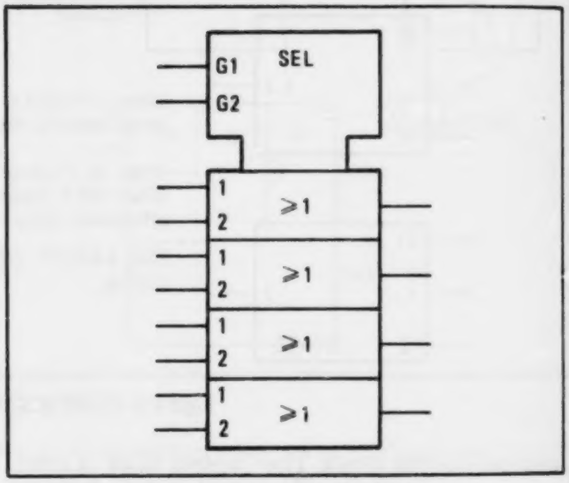


Figure 8-17. AND-OR Selector

Up/Down Counter. The Counter Control Block is used to show common inputs to a Presettable Decade UP/Down Counter. Notice that "+m" means count up (increment the count) by "m"; "–m" means count down by "m". Note: if m = 1, it may be omitted. Since the D-type flip-flops are master-slave, the output delay indicator is used. The "=9, +1" and "=0, –1" notation defines when the carry and borrow outputs are generated. They also define it as a decade counter; a binary counter would have the carry indicated with "=15, +1". Flip-flop weighting is indicated in parentheses. Input "C1" allows all four "D1" flip-flops to be preset in parallel.

Quad D-Type Latch. The Register control block is used to illustrate a quad D-type latch. There is a common active-low reset (R), and a common edge-triggered control input (C). Since there is only one dependency relationship, the controlling input is not numbered and the controlled functions (D) are subscripted with a C.

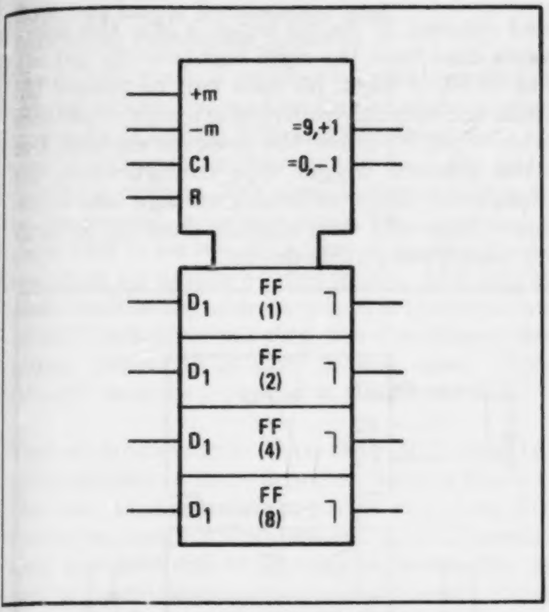

+m
−m
C1
R
=9,+1
=0,−1
D1
FF (1)
D1
FF (2)
D1
FF (4)
D1
FF (8)

Figure 8-18. Up/Down Counter

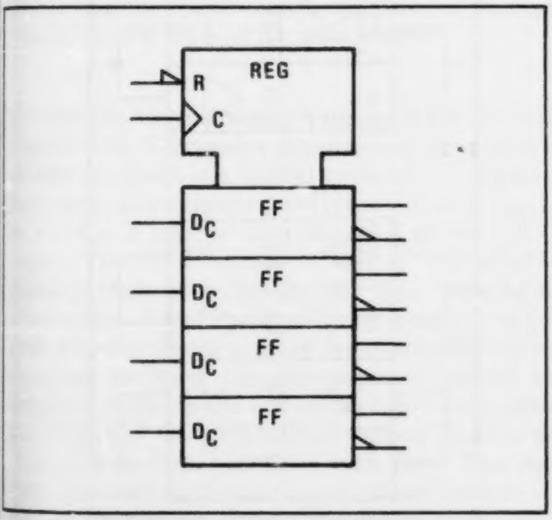

R
REG
C
DC
FF
DC
FF
DC
FF
DC
FF

Figure 8-19. Quad D-Type Latch

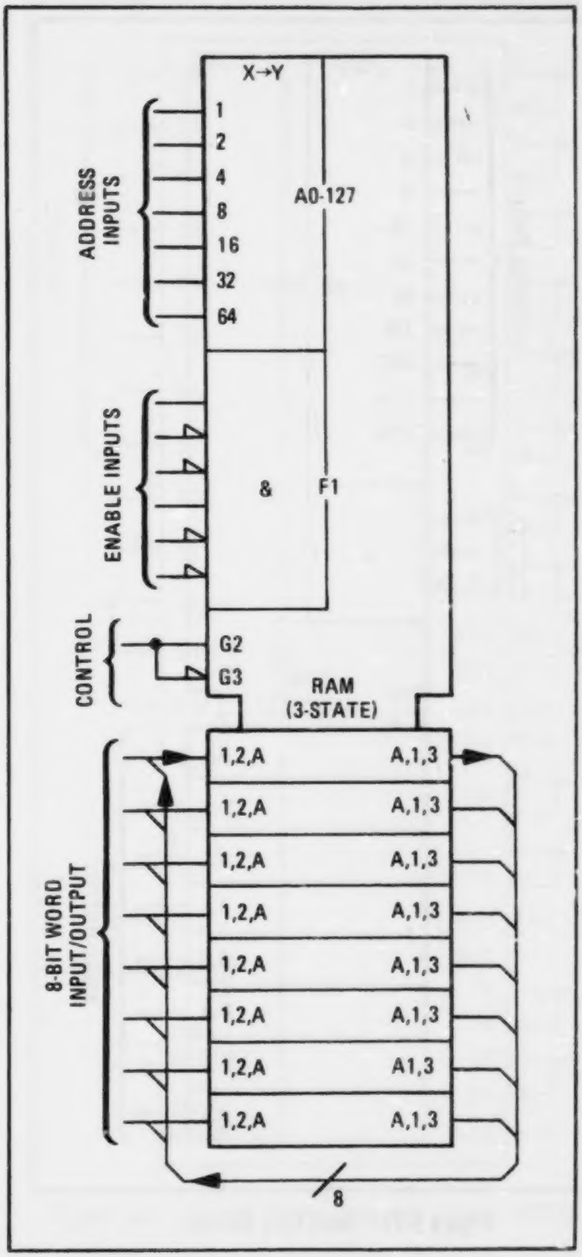

X→Y
ADDRESS INPUTS
1
2
4
8
16
32
64
A0-127
ENABLE INPUTS
&
F1
CONTROL
G2
G3
RAM (3-STATE)
8-BIT WORD INPUT/OUTPUT
1,2,A
A,1,3
1,2,A
A,1,3
1,2,A
A,1,3
1,2,A
A,1,3
1,2,A
A,1,3
1,2,A
A,1,3
1,2,A
A1,3
1,2,A
A,1,3
8

Figure 8-20. Random Access Memory

8-36. Complex Logic Symbology and Operating Principles

Microprocessor. For information regarding this device, refer to the principles of operation on Service Sheet 14.

Random Access Memory. Refer to Figure 8-20. This device provides temporary storage for up to 128 eight-bit words. Memory words are addressed on the address bus. When G2 is high, data is written into memory; when G3 is low, data is read from memory. G2 and G3 are connected internally. The device is active only when the six F1 inputs are active. Note that the input and output lines for each data bit are the same.

Read Only Memory. Refer to Figure 8-21. This device provides permanent storage for up to 2048 eight-bit words. Memory words are addressed by the address bus. When all control inputs are

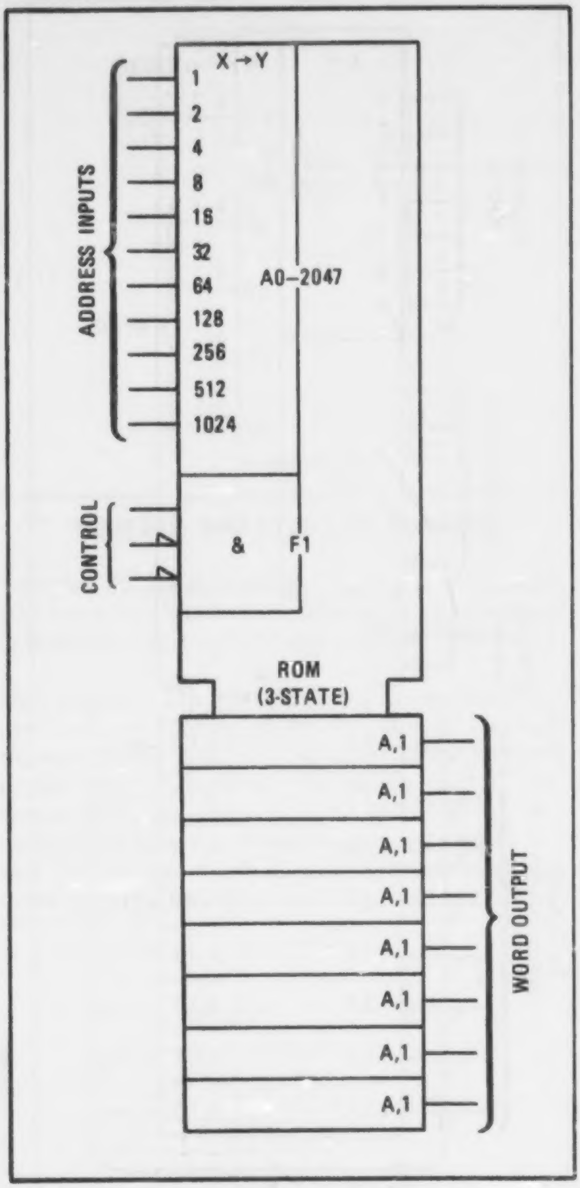

X→Y
ADDRESS INPUTS
1
2
4
8
16
32
64
128
256
512
1024
A0–2047
CONTROL
&
F1
ROM
(3-STATE)
A,1
A,1
A,1
A,1
A,1
A,1
A,1
A,1
WORD OUTPUT

Figure 8-21. Read Only Memory

Complex Logic Symbology and Operating Principles (Cont'd)

active, the output of the ROM is enabled. When any one of the F1 inputs are inactive, the output is forced into an inactive (high-impedance) state.

Multiple Bus Transceivers. Refer to Figure 8-22. This device is used as an interface between the Signal Generator's interface adapter and data bus. If the G2 input is high, the device will allow data to pass from the left-hand inputs to the right-hand outputs. If the G1 input is low, the device passes data from the right inputs to the left outputs. If F3 is high, no data can be passed (all inputs and outputs are driven to a high impedance state). When F3 is low, the device is enabled. Due to the Schmitt trigger type configuration, the propagation delay, switching voltage, and hysteresis voltage will vary slightly from bit to bit as they pass through this device.

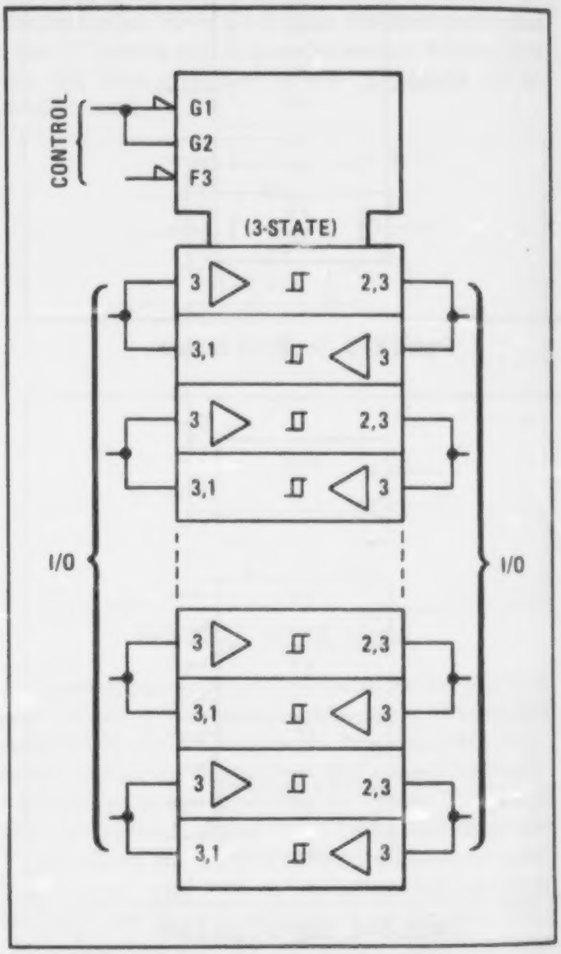

CONTROL
G1
G2
F3
(3-STATE)
3
2,3
3,1
3
3
2,3
3,1
3
I/O
I/O
3
2,3
3,1
3
3
2,3
3,1
3

Figure 8-22. Multiple Bus Transceiver With 3-State Output

General Purpose Interface Adapter (GPIA). Refer to Figure 8-23. The GPIA interfaces a microprocessor through the instrument interface and a computer controller through the HP-IB interface. Data flow between the Signal Generator's microprocessor circuits and the interface bus occurs via the D0—D7 data bus lines and the IB0—IB7 signal lines. Each allows bi-directional data transfer. The signal lines pass ASCII data (7 bits).

Complex Logic Symbology and Operating Principles (Cont'd)

The HP-IB mode is selected by placing a low on chip select CS. The read/write and address (register select) lines RS0, RS1 and RS2 select data and control information flow to and from the microprocessor circuits. The clock is derived from the microprocessor's system clock. The interrupt request IRQ is set low to interrupt microprocessor operation for data or control inputs. ASE address select enables the address output to the data lines. RESET initializes the chip. For this Signal Generator, DMA REQUEST is not used. DMA GRANT must be grounded to enable the chip.

The handshake control lines DAV, RFD and DAC are explained in more detail on Service Sheet 17. The bus management lines ATN attention, SRQ service request, REN remote enable, IFC interface clear and EOI end of information or identify are used to control information to and from the Signal Generator. Refer to Section III, HP-IB Functional Checks for information relating to these lines under various control configurations. In this unit TRIG, T1, T2, R1 and R2 are not used.

Successive Approximation Register (SAR). Refer to Figure 8-24. Successive approximation as used in this instrument is a digital approach to negative feedback. The output signal is converted to digital form and is clocked into the SAR at the DATA input. The SAR output is tied to a Digital-to-Analog Converter (DAC). The DAC acts as an attenuator, thereby controlling the output amplitude directly. Several steps (approximations) are required to bring the output amplitude to the required level. At the end of the conversion cycle, the END OF CONVERSION output inhibits the clock input. This halts the data flow. The data output is maintained at the output just prior to the end of conversion. Start Conversion must be set high to begin the conversion cycle. Feed Forward allows the conversion to be halted before the cycle is complete.

Digital-to-Analog Converter (DAC). Refer to Figure 8-25. The analog output of this Digital-to-Analog Converter is a current flow that is proportional to the maximum current available and to the binary value of the digital input. The voltage output in the formulas is shown in its simplest form and with a minimum of external components. Be aware that other components will affect the actual voltage.

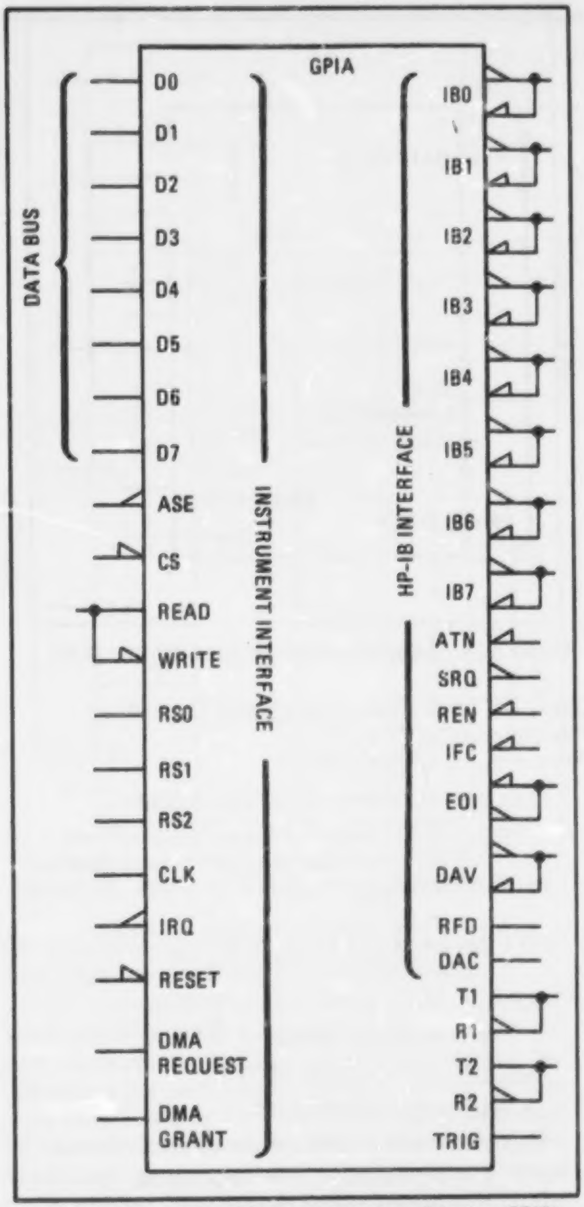


Figure 8-23. General Purpose Interface Adapter (GPIA)

The DAC output for dc voltages is:

$$V_o = V_{MAX}\ (Y/256) + V_{EE}$$

because $V_{MAX} = I_{MAX}\ (R_1)$

and $I_{MAX} = (V_1 - V_{REF(+)})/R_{EXT}$

The DAC output for ac voltages is:

$$V_o = V_i\ (Y/256)$$

Where V_o =output voltage

V_{MAX} =maximum dc output voltage

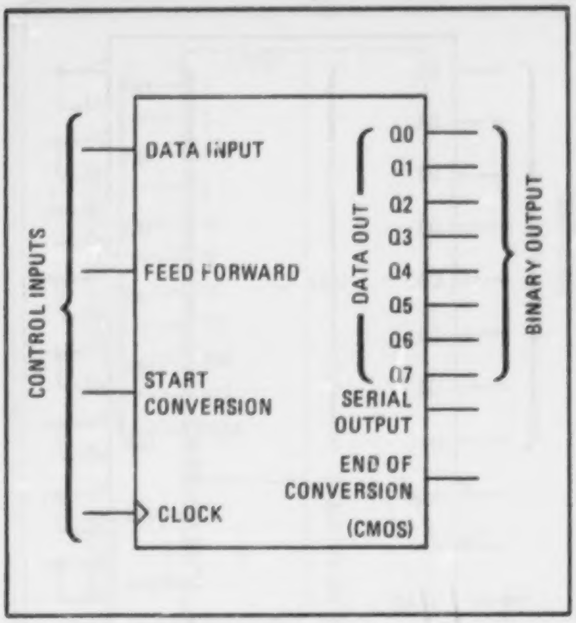


Figure 8-24. Successive Approximation Register (SAR)

Complex Logic Symbology and Operating Principles (Cont'd)

Where V_o = output voltage
V_{MAX} = maximum dc output voltage
V_{EE} = DAC negative bias voltage. (Note: the formulas assume R1 is connected to V_{EE})
V_1 = DAC input dc voltage applied to $V_{REF(+)}$ through R_{EXT}
$V_{REF(+)}$ = DAC positive dc reference
V_i = ac input voltage
I_{MAX} = maximum dc current
R_1 = output resistance
R_{EXT} = resistor that sets maximum current
Y = summation of binary inputs (X) from 1 to 255 in steps of 1

Programmable Interval Timer. Refer to Figure 8-26. This device contains three independent 16-bit down counters which can operate in either binary or BCD count sequences. Each counter is gated and clocked via its own input port. The Data Input pins of the device are bi-directional; data is input to or output from the internal buffer following read or write instructions. Functions of the internal data bus buffers include: programming the modes of the internal counters, pre-setting the count registers, and reading intermediate count values. An active low on the Write line allows the internal counters and mode registers to be loaded; an active low on the Read line allows any one of the counter's immediate count values to be read. The Read/Write inputs are enabled by a low at the Select input which has no effect on any count operation. The A0 and A1 address inputs serve to select one of the three counters and to address the internal control word register for mode selection. A "00" at the A0 and A1 inputs selects counter 0, "01" selects counter 1, "10" selects counter 2, and "11" selects the control word register. Each counter's input, gate, and output functions are controlled through the selection of modes via the data bus. Mode selection is stored in the control word register. The six modes of counter operation are interrupt on terminal count, one-shot operation, rate generation, square wave generation, software triggered strobing and hardware triggered strobing.

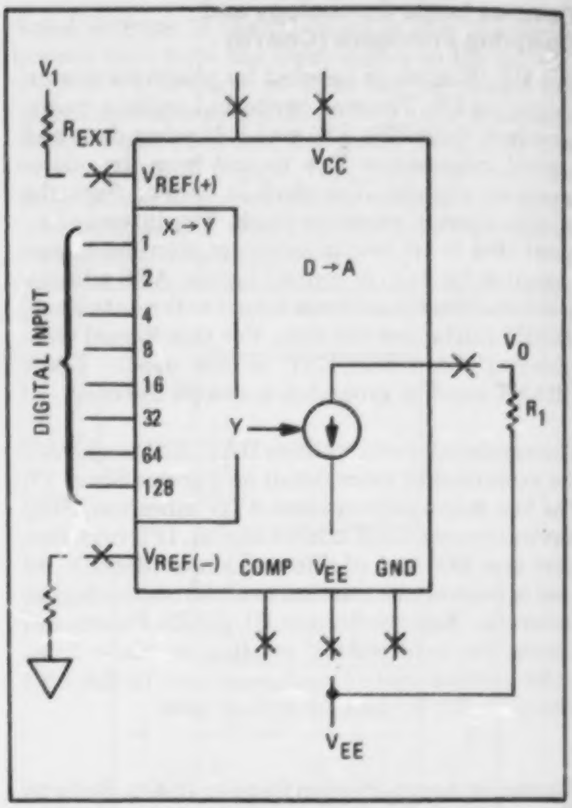


Figure 8-25. Digital-to-Analog Converter (8-bit)

BCD-to-Seven-Segment Latch/Decoder/Divider. Refer to Figure 8-27. This device latches and decodes BCD data to drive the individual segments of a 7-segment common cathode display. The BCD code is latched into the four flip-flops when C2 goes low. The BCD data is converted to a decimal code and then to the seven-segment code.

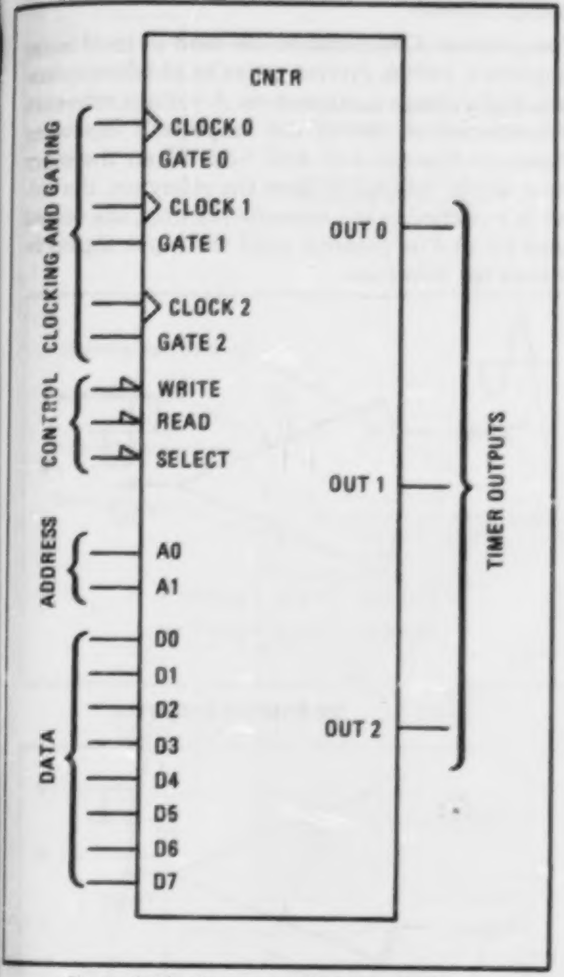

CNTR
CLOCKING AND GATING
CLOCK 0
GATE 0
CLOCK 1
GATE 1
CLOCK 2
GATE 2
CONTROL
WRITE
READ
SELECT
ADDRESS
A0
A1
DATA
D0
D1
D2
D3
D4
D5
D6
D7
OUT 0
OUT 1
OUT 2
TIMER OUTPUTS

Figure 8-26. Programmable Interval Timer

Complex Logic Symbology and Operating Principles (Cont'd)

The seven-segment output is enabled by an active G4 and an active V1. G4 is active when two conditions exist together: 1) when the binary data is equivalent to decimal 0—9 and 2) when G3 is high. When G3 is low, the outputs are disabled and the display is blanked. When V1 is active (low) all seven output lines will be high to test all segments of the display.

8-37. Linear Device Operating Principles

Operational Amplifiers. The source of gain in an operational amplifier can be characterized as an ideal differential voltage amplifier having low output impedance, high input impedance, and very high differential gain. The output of an operational amplifier is proportional to the difference in the voltages applied to the two input terminals. In use, the amplifier output drives the input voltage difference close to zero through a feedback path.

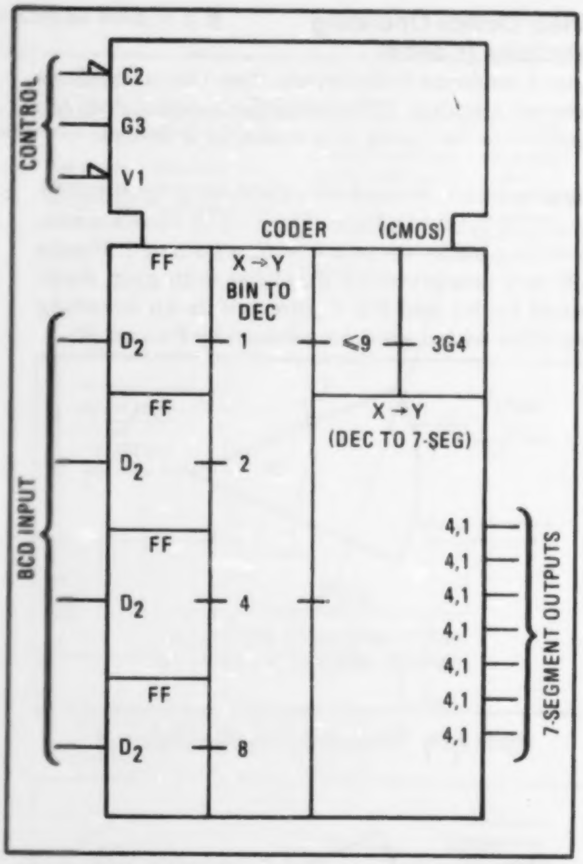

CONTROL
C2
G3
V1
CODER
(CMOS)
FF
X→Y
BIN TO
DEC
BCD INPUT
D_2
1
2
4
8
≤9
3G4
X→Y
(DEC TO 7-SEG)
4,1
4,1
4,1
4,1
4,1
4,1
4,1
7-SEGMENT OUTPUTS

Figure 8-27. BCD-to-Seven-Segment Latch/Decoder/Driver

When troubleshooting an operational amplifier circuit, measure the voltages at the two inputs; the difference between these voltages should be less than 10 mV. (Note: This troubleshooting procedure will not work for operational amplifiers which are configured as comparators.) A difference voltage much greater than 10 mV indicates trouble in the amplifier or its external circuitry. Usually, this difference will be several volts and one of the inputs will be very close to one of the supply voltages (e.g., +15V or −15V).

Next, check the amplifier's output voltage. It will probably also be close to one of the supply voltages (e.g., ground, +15V, or −15V). Check to see that the output conforms to the inputs. For example, if the inverting input is more positive than the non-inverting input, the output should be negative; if the non-inverting input is more positive than the inverting input, the output should be positive. If the

Linear Device Operating Principles (Cont'd)

output conforms to the inputs, check the amplifier's external circuitry. If the amplifier's output does not conform to its inputs, it is probably defective.

Figures 8-28, 8-29 and 8-30 show typical operational amplifier configurations. Figure 8-28 shows a non-inverting buffer amplifier with a gain of 1. Figure 8-29 is a non-inverting amplifier with gain determined by R1 and R2. Figure 8-30 is an inverting amplifier with a gain determined by R1 and R2.

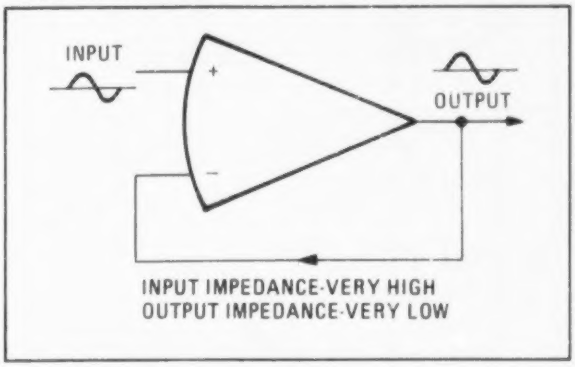

INPUT
+
−
OUTPUT
INPUT IMPEDANCE-VERY HIGH
OUTPUT IMPEDANCE-VERY LOW

Figure 8-28. Non-Inverting Amplifier (Gain = 1)

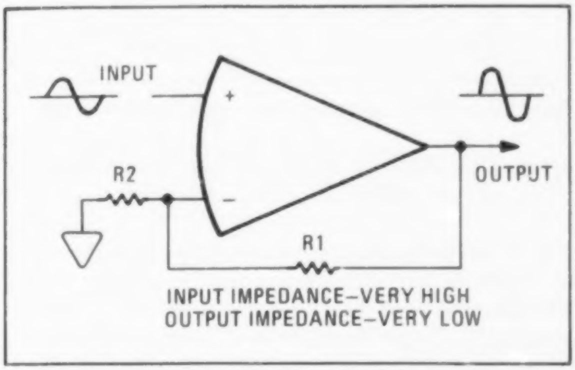

INPUT
+
−
R2
R1
OUTPUT
INPUT IMPEDANCE–VERY HIGH
OUTPUT IMPEDANCE–VERY LOW

Figure 8-29. Non-Inverting Amplifier (Gain = 1 + R_1/R_2)

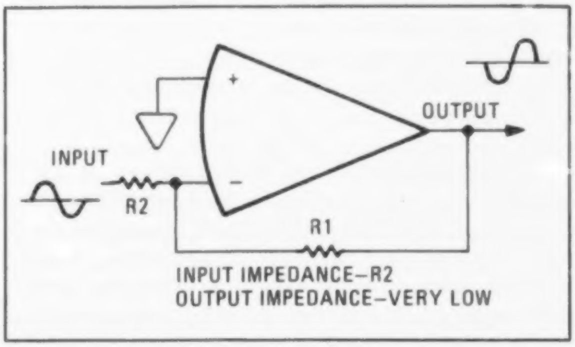

+
−
OUTPUT
INPUT
R2
R1
INPUT IMPEDANCE–R2
OUTPUT IMPEDANCE–VERY LOW

Figure 8-30. Inverting Amplifier (Gain = $-R_1/R_2$)

Comparators. Comparators are used as level sense amplifiers, switch drivers, pulse height discriminators, and voltage comparators. A voltage reference is connected to one of the amplifier's inputs as shown in Figures 8-31 and 8-32. When the other input signal voltage crosses the reference, the output is switched to the opposite polarity; the output remains at this polarity until the input signal re-crosses the reference.

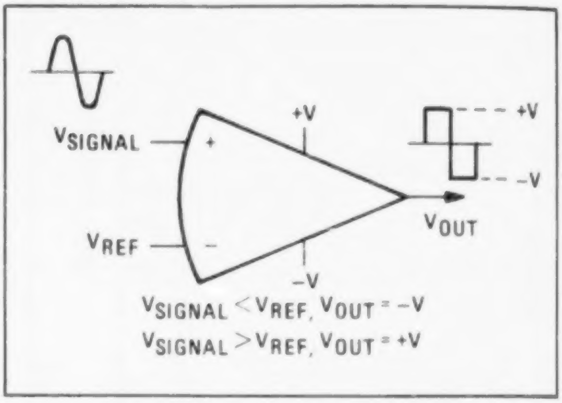

V_{SIGNAL}
V_{REF}
+
−
+V
−V
+V
−V
V_{OUT}
$V_{SIGNAL} < V_{REF}, V_{OUT} = -V$
$V_{SIGNAL} > V_{REF}, V_{OUT} = +V$

Figure 8-31. Non-Inverting Comparator

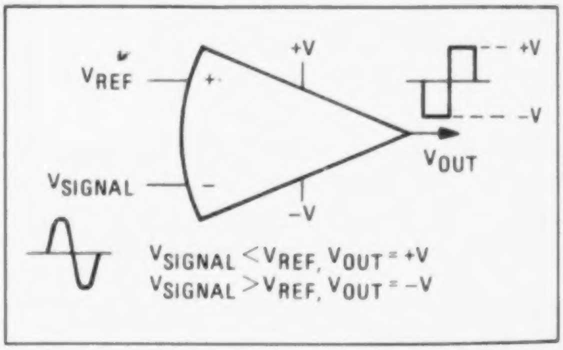
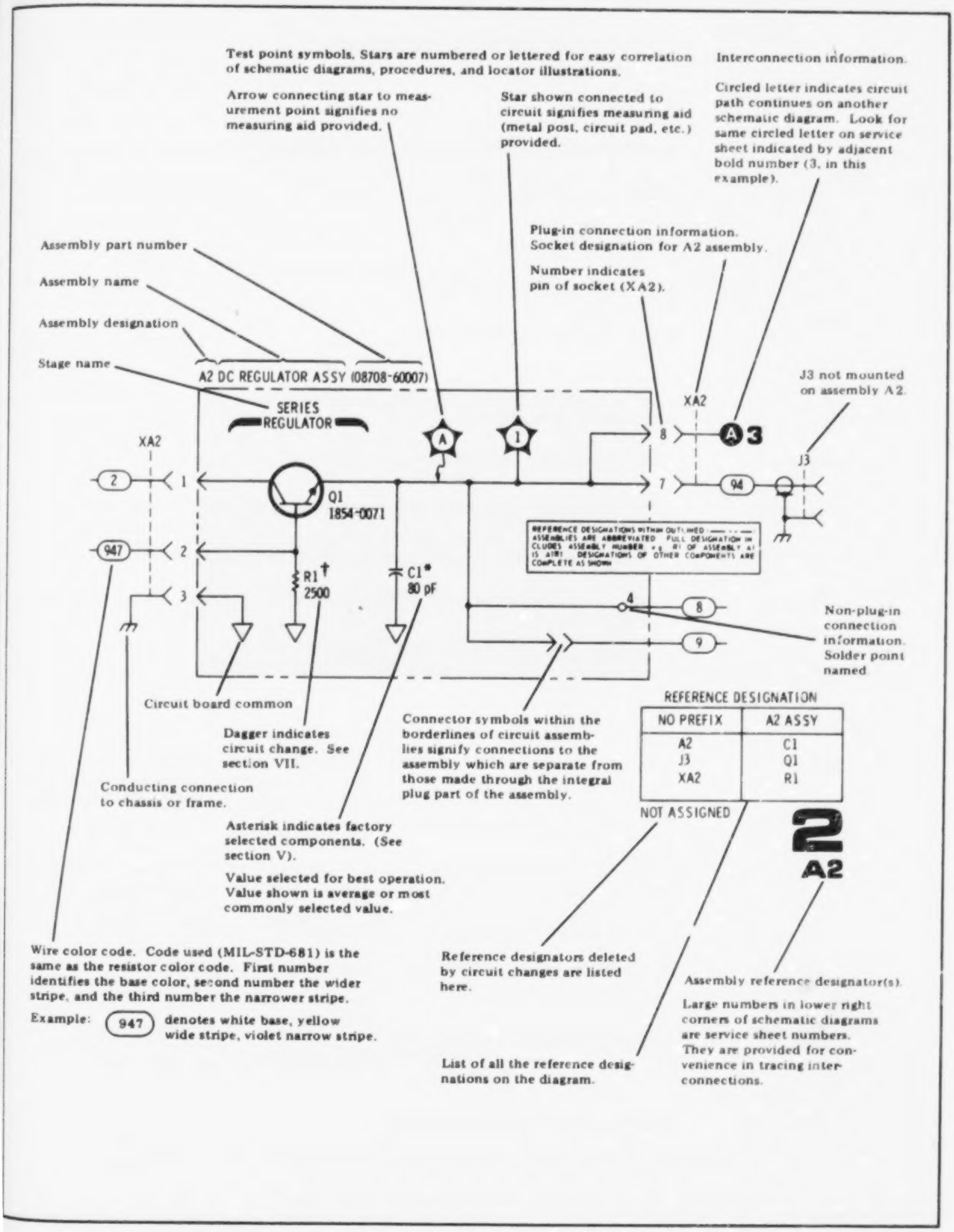

V_{REF}
V_{SIGNAL}
+
−
+V
−V
+V
−V
V_{OUT}
$V_{SIGNAL} < V_{REF}, V_{OUT} = +V$
$V_{SIGNAL} > V_{REF}, V_{OUT} = -V$

Figure 8-32. Inverting Comparator

Table 8-3. Schematic Diagram Notes (1 of 8)


A2 DC REGULATOR ASSY (08708-60007)
SERIES
REGULATOR
XA2
2
947
1
2
3
Q1
1854-0071
R1†
2500
C1*
80 pF
A
1
8
7
4
XA2
A3
94
J3
8
9
REFERENCE DESIGNATIONS WITHIN OUTLINED ASSEMBLIES ARE ABBREVIATED. FULL DESIGNATION INCLUDES ASSEMBLY NUMBER e.g. R1 OF ASSEMBLY A1 IS A1R1. DESIGNATIONS OF OTHER COMPONENTS ARE COMPLETE AS SHOWN
2
A2

REFERENCE DESIGNATION

NO PREFIX	A2 ASSY
A2 J3 XA2	C1 Q1 R1

NOT ASSIGNED

Test point symbols. Stars are numbered or lettered for easy correlation of schematic diagrams, procedures, and locator illustrations.

Arrow connecting star to measurement point signifies no measuring aid provided.

Star shown connected to circuit signifies measuring aid (metal post, circuit pad, etc.) provided.

Interconnection information.

Circled letter indicates circuit path continues on another schematic diagram. Look for same circled letter on service sheet indicated by adjacent bold number (3, in this example).

Plug-in connection information. Socket designation for A2 assembly.

Number indicates pin of socket (XA2).

Assembly part number

Assembly name

Assembly designation

Stage name

J3 not mounted on assembly A2.

Non-plug-in connection information. Solder point named.

Circuit board common

Dagger indicates circuit change. See section VII.

Conducting connection to chassis or frame.

Connector symbols within the borderlines of circuit assemblies signify connections to the assembly which are separate from those made through the integral plug part of the assembly.

Asterisk indicates factory selected components. (See section V).

Value selected for best operation. Value shown is average or most commonly selected value.

Wire color code. Code used (MIL-STD-681) is the same as the resistor color code. First number identifies the base color, second number the wider stripe, and the third number the narrower stripe.

Example: (947) denotes white base, yellow wide stripe, violet narrow stripe.

Reference designators deleted by circuit changes are listed here.

List of all the reference designations on the diagram.

Assembly reference designator(s).

Large numbers in lower right corners of schematic diagrams are service sheet numbers. They are provided for convenience in tracing interconnections.

Table 8-3. Schematic Diagram Notes (2 of 8)

SCHEMATIC DIAGRAM NOTES

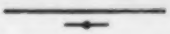
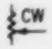
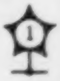
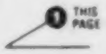
*	Asterisk denotes a factory-selected value. Value shown is typical. See Section V.
†	Dagger indicates circuit change. See Section VII.
⊘	Tool-aided adjustment.
○	Manual control.
▭	Encloses front-panel designation.
⬚	Encloses rear-panel designation.
—— - - ——	Circuit assembly borderline.
- - - - - - -	Other assembly borderline.
━━►━━	Heavy line with arrows indicates path and direction of main signal.
━ ━►━ ━	Heavy dashed line with arrows indicates path and direction of main feedback.
	Indicates stripline (i.e., RF transmission line above ground).
	Wiper moves toward cw with clockwise rotation of control (as viewed from shaft or knob).
	Numbered Test Point measurement aid provided.
⬭	Encloses wire or cable color code. Code used is the same as the resistor color code. First number identifies the base color, second number identifies the wider stripe, and the third number identifies the narrower stripe, e.g., (947) denotes white base, yellow wide stripe, violet narrow stripe.
⏚	A direct conducting connection to earth, or a conducting connection to a structure that has a similar function (e.g., the frame of an air, sea, or land vehicle).
⊥	A conducting connection to a chassis or frame.
▽	Common connections. All like-designation points are connected.
Ⓐ12	Letter = off-page connection, e.g., Ⓐ. Number = Service Sheet number for off-page connection, e.g., **12**.
	Number (only) = on-page connection.

Table 8-3. Schematic Diagram Notes (3 of 8)

SCHEMATIC DIAGRAM NOTES

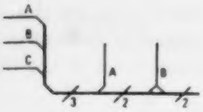
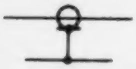
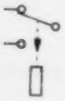
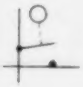
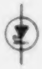
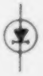
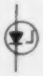
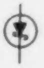
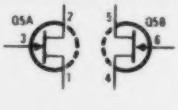
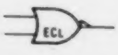
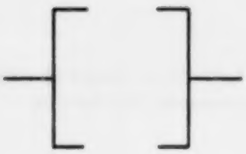
	Indicates multiple paths represented by only one line. Letters or names identify individual paths. Numbers indicate number of paths represented by the line.
	Coaxial or shielded cable.
	Relay. Contact moves in direction of arrow when energized.
	Indicates a pushbutton switch with a momentary (ON) position.
	Indicates a PIN diode.
	Indicates a current regulation diode.
	Indicates a voltage regulation diode.
	Indicates a Schottky (hot-carrier) diode.
	Multiple transistors in a single package—physical location of the pins is shown in package outline on schematic.
	Identification of logic families as shown (in this case, ECL).

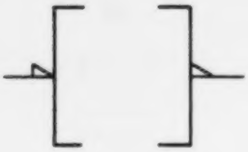
Table 8-3. Schematic Diagram Notes (4 of 8)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

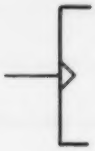
Input and Output Indicators



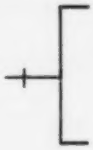
Implied Indicator—Absence of polarity indicator (see below) implies that the active state is a relative high voltage level. Absence of negation indicator (see below) implies that the active state is a relative high voltage level at the input or output.



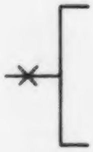
Polarity Indicator—The active state is a relatively low voltage level.



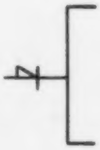
Dynamic Indicator—The active state is a transition from a relative low to a relative high voltage level.



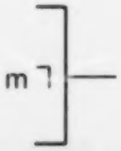
Inhibit Input—Input that, when active, inhibits (blocks) the active state outputs of a digital device.



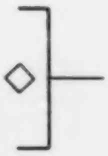
Analog Input—Input that is a continuous signal function (e.g., a sine wave).



Polarity Indicator used with Inhibit Indicator—Indicates that the relatively low level signal inhibits (blocks) the active state outputs of a digital device.



Output Delay—Binary output changes state only after the referenced input (m) returns to its inactive state (m should be replaced by appropriate dependency or function symbols).



Open Collector or Open Emitter Output.

Table 8-3. Schematic Diagram Notes (5 of 8)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

	Input and Output Indicators (Cont'd)
3-STATE	Three-state Output—Indicates outputs that can have a high impedance (disconnect) state in addition to the normal binary logic states.
	Combinational Logic Symbols and Functions
&	AND—All inputs must be active for the output to be active.
≥1	OR—One or more inputs being active will cause the output to be active.
≥m	Logic Threshold—m or more inputs being active will cause the output to be active (replace m with a number).
=1	EXCLUSIVE OR—Output will be active when one (and only one) input is active.
=m	m and only m—Output will be active when m (and only m) inputs are active (replace m with a number).
=	Logic Identity—Output will be active only when all or none of the inputs are active (i.e., when all inputs are identical, output will be active).
▷	Amplifier—The output will be active only when the input is active (can be used with polarity or logic indicator at input or output to signify inversion).
X/Y	Signal Level Converter—Input level(s) are different than output level(s).
⟷	Bilateral Switch—Binary controlled switch which acts as an on/off switch to analog or binary signals flowing in both directions. Dependency notation should be used to indicate affecting/affected inputs and outputs. Note: amplifier symbol (with dependency notation) should be read to indicate unilateral switching.
X→Y	Coder—Input code (X) is converted to output code (Y) per weighted values or a table.
(Functional Labels)	The following labels are to be used as necessary to ensure rapid identification of device function.
MUX	Multiplexer—The output is dependent only on the selected input.
DEMUX	Demultiplexer—Only the selected output is a function of the input.
CPU	Central Processing Unit

Table 8-3. Schematic Diagram Notes (6 of 8)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

Sequential Logic Functions

1 ⎍	Monostable—Single shot multivibrator. Output becomes active when the input becomes active. Output remains active (even if the input becomes inactive) for a period of time that is characteristic of the device and/or circuit.
G ⎍⎍⎍	Oscillator—The output is a uniform repetitive signal which alternates between the high and low state values. If an input is shown, then the output will be active if and only if the input is in the active state.
FF	Flip-Flop—Binary element with two stable states, set and reset. When the flip-flop is set, its outputs will be in their active states. When the flip-flop is reset, its outputs will be in their inactive states.
T	Toggle Input—When active, causes the flip-flop to change states.
S	Set Input—When active, causes the flip-flop to set.
R	Reset Input—When active, causes the flip-flop to reset.
J	J Input—Analogous to set input.
K	K Input—Analogous to reset input.
D	Data Input—Always enabled by another input (generally a C input—see Dependency Notation). When the D input is dependency-enabled, a high level at D will set the flip-flop; a low level will reset the flip-flop. Note: strictly speaking, D inputs have no active or inactive states—they are just enabled or disabled.
+m	Count-Up Input—When active, increments the contents (count) of a counter by "m" counts (m is replaced with a number).
−m	Count-Down Input—When active, decrements the contents (count) of a counter by "m" counts (m is replaced with a number).
→m	Shift Right (Down) Input—When active, causes the contents of a shift register to shift to the right or down "m" places (m is replaced with a number).
←m	Shift Left (Up) Input—When active, causes the contents of a shift register to shift to the left or up "m" places (m is replaced with a number).

NOTE

For the four functions shown above, if m is one, it is omitted.

(Functional Labels)	The following functional labels are to be used as necessary in symbol build-ups to ensure rapid identification of device function.
mCNTR	Counter—Array of flip-flops connected to form a counter with modules m (m is replaced with a number that indicates the number of states: 5 CNTR, 10 CNTR, etc.).

Table 8-3. Schematic Diagram Notes (7 of 8)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

Sequential Logic Functions (Cont'd)

REG	Register—Array of unconnected flip-flops that form a simple register or latch.
SREG	Shift Register—Array of flip-flops that form a register with internal connections that permit shifting the contents from flip-flop to flip-flop.
ROM	Read Only Memory—Addressable memory with read-out capability only.
RAM	Random Access Memory—Addressable memory with read-in and read-out capability.

Dependency Notation

mAm	Address Dependency—Binary affecting inputs of affected outputs. The m prefix is replaced with a number that differentiates between several address inputs, indicates dependency, or indicates demultiplexing and multiplexing of address inputs and outputs. The m suffix indicates the number of cells that can be addressed.
Gm	Gate (AND) Dependency—Binary affecting input with an AND relationship to those inputs or outputs labeled with the same identifier. The m is replaced with a number or letter (the identifier).
Cm	Control Dependency—Binary affecting input used where more than a simple AND relationship exists between the C input and the affected inputs and outputs (used only with D-type flip-flops).
Vm	OR Dependency—Binary affecting input with an OR relationship to those inputs or outputs labeled with the same identifier. The m is replaced with a number or the letter (the identifier).
Fm	Free Dependency—Binary affecting input acting as a connect switch when active and a disconnect when inactive. Used to control the 3-state behavior of a 3-state device.

NOTE

The identifier (m) is omitted if it is one—that is, when there is only one dependency relationship of that kind in a particular device. When this is done, the dependency indicator itself (G, C, F, or V) is used to prefix or suffix the affected (dependent) input or output.

Miscellaneous

⎎	Schmitt Trigger—Input characterized by hysterisis; one threshold for positive going signals and a second threshold for negative going signals.

Table 8-3. Schematic Diagram Notes (8 of 8)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

Miscellaneous (Cont'd)

Active	Active State—A binary physical or logical state that corresponds to the true state of an input, an output, or a function. The opposite of the inactive state.
Enable	Enabled Condition—A logical state that occurs when dependency conditions are satisfied. Although not explicitly stated in the definitions listed above, functions are assumed to be enabled when their behavior is described. A convenient way to think of it is as follows: A function becomes active when: • it is enabled (dependency conditions—if any—are satisfied) • and its external stimulus (e.g., voltage level) enters the active state.

SERVICE SHEET BD1
MODEL 8656A SIGNAL GENERATOR
TROUBLESHOOTING HELP

Section II, Line Voltage and Fuse Selection
Section III, Operator's Checks and Power On Sequence

PRINCIPLES OF OPERATION

General. The Signal Generator can be conceptually broken down into three subsections. The block diagrams of the individual subsections are illustrated on the following Service Sheets:

BD2—High Frequency and Output Section
BD3—Low Frequency and FM Section
BD4—Microprocessor, Keyboard, and Display Section

The Signal Generator uses frequency synthesis to generate a carrier frequency range of 100 kHz to 990 MHz. Its output amplitude is leveled and calibrated from +13 to −127 dBm. AM and/or FM functions can be individually selected. The carrier frequency, output amplitude, and modulation functions can be remotely programmed via the HP-IB.

Frequency synthesis translates a stable, accurate reference into an output signal of a different frequency. The output frequency has a finite number of values within a frequency range. The resolution of the synthesizer determines the spacing between the discrete values that the output frequency can assume. All output frequencies retain the same accuracy and stability as the reference signal.

When using the indirect synthesis method of generating output frequencies, phase lock loops are locked to a signal from a crystal controlled reference oscillator. The two phase lock loops used in the Signal Generator generate signals which are combined to produce the instrument's frequency range (100 kHz to 990 MHz). Every output frequency starts as a signal in the basic oscillator frequency band (494 to 990 MHz) and is divided or heterodyned in the output section if required. The broad frequency range is generated in the following four bands:

1. 100 kHz to 123.5 MHz (Heterodyned)
2. 123.5 to 247 MHz (Divide-by-4)
3. 247 to 494 MHz (Divide-by-2)
4. 494 to 990 MHz (Divide-by-1 or Basic Band)

High Frequency and Output Section. The Frequency Multiplier multiplies the 50 MHz reference signal by 16 to obtain an 800 MHz signal. It also mixes the 800 MHz with the 60 to 110 MHz output of the low frequency loop to provide a frequency between 690 and 740 MHz in steps of 100 or 250 Hz and to phase lock the high frequency loop. As a result, the 50 MHz Reference Oscillator is the only signal whose noise is multiplied and added to the output. By using a narrow band of frequencies (690 to 740 MHz) to phase lock the high frequency loop, the possibility of spurious signals is reduced. The 800 MHz is also sent to the Output Section and mixed with specific frequencies in the basic band (800.1 to 923.5 MHz) to obtain the heterodyne band of frequencies (100 kHz to 123.5 MHz).

The high frequency feedback loop phase locks the 494 to 990 MHz basic band Voltage Controlled Oscillator (VCO). A frequency from the oscillator is mixed with a frequency between 690 and 740 MHz from the Frequency Multiplier. Both the upper and lower sidebands from the Mixer are used to obtain Intermediate (IF) Frequencies in 50 MHz steps from 0 to 250 MHz. Any frequency in the 494 to 990 MHz range can be selected by adding or subtracting the appropriate IF frequency (e.g., 690 to 740 + 250 = 940 to 990 MHz, 694 to 740 − 200 = 494 to 540 MHz). The IF frequency is sampled by the output of the Pulse Generator that is driven by the 50 MHz Reference Oscillator signal. Correction voltage from the sampler tunes the high frequency VCO to correct for frequency error. The VCO is phase locked to an oscillator in the low frequency loop with only a 50 MHz tuning range (60 to 110 MHz) which in turn is phase locked to the 50 MHz reference through a programmable divider. Noise from the high frequency VCO is corrected for in the wideband phase lock loop. Therefore, the main contributor of noise and residual FM is the 60 to 110 MHz low frequency VCO.

The Output Section translates the 494 to 990 MHz basic band frequencies to all other frequencies by dividing (123.5 MHz to 990 MHz) or heterodyning (100 kHz to 123.5 MHz), controls the RF output amplitude, and filters and amplifies the oscillator and dividers output.

Each of the divide by 1, 2, and 4 bands is one octave (i.e., 494 to 990 MHz for the divide-by-1 band, 247 to 494 MHz for the divide by 2 band, and 123.5 to 247 MHz for the divide-by-4 band). Each Voltage Tuned Filter's bandwidth is also one octave and

SERVICE SHEET BD1 (Cont'd)

tuned by a voltage derived from the high frequency VCO's tune voltage. The filters therefore track the oscillator's frequency and are biased on only when that band is selected. This selection of filters provides better isolation and filtering of the out-of-band spurious and harmonic frequencies.

Output level is stepped in 10 dB steps by an electromechanical step attenuator. Output level changes less than 10 dB are controlled by the input to the Automatic Level Control (ALC) Amplifier from the Level Digital-to-Analog Converter (DAC). The ALC Amplifier has two inputs. One is the detected output voltage to level the output. The other is the sum of the amplitude modulation voltage and the level voltage (for level changes less than 10 dB and level correction for frequency response). The output of the ALC Amplifier controls the current through the PIN diode Modulator which controls the fine level attenuation and amplitude modulation of the output.

When triggered, the reverse power protection circuit opens a relay in series with the output. Limiting diodes sense reverse power and provide the voltage to open the relay and protect the output circuits during the time delay until the relay opens.

Internal modulation signals of 400 Hz or 1000 Hz for amplitude and frequency modulation from the Audio Oscillator can be used, or external amplitude and frequency modulation can be selected at the front panel. The internal and external modulation signals are converted to the proper drive levels by the AM% DAC and the FM Dev DAC. The Signal Generator's output can be simultaneously amplitude and frequency modulated by either the 400 Hz or 1000 Hz internal signals and an external signal or any combination thereof. However, only one amplitude modulation and one frequency modulation level can be used. The carrier frequency modulation is generated in the low frequency loop which allows for RF output FM deviation up to 99 kHz for output frequencies that are not divided. These frequencies are the heterodyne band (100 kHz to 123.5 MHz) and the basic band (494 to 990 MHz). The amplitude modulation signal is applied to the ALC Amplifier.

Low Frequency and FM Section. The 50 MHz Reference Oscillator is a crystal oscillator. Its output phase locks the VCOs and is also divided down to provide the 1 MHz time base. The rear panel TIME BASE OUTPUT is a jumper-selectable frequency of 1, 5, or 10 MHz that is divided from the 50 MHz Reference Oscillator and can be used as a stable reference for other instruments.

For Option 001, a 10 MHz temperature-stabilized crystal oscillator is used. The 50 MHz Reference Oscillator is phase locked to the crystal oscillator for greater accuracy and stability. An external reference of 1, 5, or 10 MHz may also be used to phase lock the 50 MHz Reference Oscillator. However, the jumper-selected frequency of 1, 5, or 10 MHz must be the same as the external frequency. With Option 001 instruments, the jumper selection must be 10 MHz. The 50 MHz reference signal is distributed and translated by frequency doublers and mixers to provide reference signals at other frequencies.

The 60 to 110 MHz low frequency VCO is tracked by the high frequency basic band oscillator's frequency. The low frequency VCO is tuned to the correct frequency by the Microprocessor and is locked to the 50 MHz Reference Oscillator. Depending upon the frequency, the Reference Oscillator and the low frequency VCO signals are both divided down to 100 or 250 Hz. This output is used to phase lock the VCO and for the output frequency resolution of 100 Hz or 250 Hz. Any phase difference between the two signals is converted to a voltage, sampled, and applied to the VCO to correct its frequency. The low frequency loop has a narrow bandwidth which enables the VCO to be frequency modulated outside the loop bandwidth. The VCO is tuned over its 50 MHz range in 100 Hz or 250 Hz steps. It therefore steps the 690 to 740 MHz signal, generated by mixing the 60 to 110 MHz with the 800 MHz in the Frequency Multiplier Mixer, in 100 Hz or 250 Hz steps.

Microprocessor, Keyboard, and Display Section. The Microprocessor controls the information on the address bus and data bus, thereby controlling all digital data throughout the instrument. The Microprocessor with its associated Read Only Memory (ROM), Random Access Memory (RAM), Input/Output (I/O), and decoder circuits processes the front panel keyboard inputs, the Hewlett-Packard Interface Bus (HP-IB) inputs, and all displayed information.

Digital data sent to the High Frequency and Output Section performs the following functions:

a. Controls the Voltage Controlled Oscillator (VCO) lock point.

SERVICE SHEET BD1 (Cont'd)

b. Turns off the correct IF notch filter to pass the specified IF frequency and lock the VCO at the correct frequency.

c. Corrects the output level for frequency response.

d. Changes attenuation in 0.1 dB increments.

e. Controls the amplitude modulation of the carrier.

f. Selects the heterodyne frequencies, and the divide by one, two, or four band as required.

g. Sets attenuation in 10 dB steps.

h. Resets the Reverse Power Relay.

Digital data sent to the Low Frequency and FM Section determines the frequency modulation of the carrier and the frequency resolution of the output (100 or 250 Hz).

Two high frequency data words and eight low frequency data words are serially sent to the High Frequency and Output Section and the Low Frequency and FM Section. The serial data is strobed into the correct registers by decoding the address bus bits. Parallel data is also sent to the High Frequency and Output Section to select AM, FM, and level control; to select the frequency bands; and to select the amount of attenuation in the step attenuator.

TROUBLESHOOTING

The troubleshooting checks on this service sheet are used to isolate a malfunction to one of the three major functional assemblies. The checks are easy to perform and provide much key information. In most instances the checks isolate a failure to either a hardware or a software (controller) problem. The comments associated with each procedure summarize the information known as a result of passing or failing the check. The checks should be done in order.

√1 Line Check

Procedure. Remove the Signal Generator's bottom cover. Refer to the Disassembly Procedures under Repair in Section VIII. After the bottom cover is removed, connect the line voltage.

Normal Indications.

1. The fan runs indicating line voltage or Mains (ac) power is present on the power transformer primary.

2. The three green Light Emitting Diodes (LEDs) on the A10 Audio Power Supply Assembly are lighted indicating that the regulated supplies are operating. This does not mean that the supply voltages are within the required tolerance.

3. Set the RESET/STBY/ON Switch to ON. The amplitude is −127 dBm and the increment is 10 dB. Press the amplitude increment key (up arrow). The clicks can be heard as the attenuator solenoid switches are opened and closed. The attenuator latches receive power from the +24 volt unregulated supply.

Abnormal Indications. If an abnormal indication occurs:

1. Check rear-panel line fuse and line voltage selector.

2. Measure individual regulated supplies and unregulated supply. If necessary, go to Service Sheet 22.

√2 Power-Up Check

Procedure. Switch RESET-STBY-ON switch to RESET and back to ON. Check the front panel annunciators (LEDs) and display segments.

Normal Indication. All front panel indicators are lighted for approximately 1.5 seconds to provide a visual inspection of each front panel annunciator and display segment.

1. All the display segments will display the number eight except the least significant FREQUENCY digit will be a five and the most significant AMPLITUDE digit will be a one.

2. When the power up subroutine is completed, the modulation display will be off, frequency set to 100 MHz and amplitude to −127 dBm.

Abnormal Indication. If an abnormal indication occurs, that is:

1. The LEDs stay lighted and display segments remain eights, five and one, go to Service Sheet BD4.

SERVICE SHEET BD1 (Cont'd)

2. The LEDs stay lighted and numerical displays are all zeros except the least significant FREQUENCY digit.

   a) Check for a noisy +5 Vdc power supply. If necessary, go to Service Sheet 22.

   b) Check the Microprocessor clock. Go to Service Sheet 14.

3. An LED or display segment does not show the correct output. Check the display's associated components and drive circuits. Go to Service Sheets 19 or 20 (FREQUENCY display problem) or Service Sheet 19 or 21 (MODULATION or AMPLITUDE display problem).

√3 Frequency and Amplitude

Procedure. Set the amplitude to 0.0 dBm and check the RF OUTPUT frequency and amplitude.

Normal Indication.

1. The RF output is phase locked at 100 MHz; the amplitude is 0.0 dBm ±1.0 dB.

2. The FREQUENCY display is 100 MHz; the AMPLITUDE display is 0.0 dBm.

Abnormal Indication. If an abnormal indication occurs, that is:

1. The AMPLITUDE or FREQUENCY display is not 0.0 dBm or 100 MHz respectively, go to Service Sheet BD4.

2. The output frequency is not phase locked, go to Service Sheets BD2 or BD3.

3. The output frequency is incorrect, go to Service Sheet BD2.

4. The output amplitude is incorrect, go to Service Sheet BD2.

√4 Modulation

Procedure. Set the modulation to INT 1 kHz, AM 50% and FM 50 kHz.

Normal Indications.

1. MODULATION display 1 kHz, INT AM, INT FM, and 50% or 50 kHz (depending on last input).

2. Modulated RF output of 50% AM and 50 kHz FM deviation at 1 kHz rate.

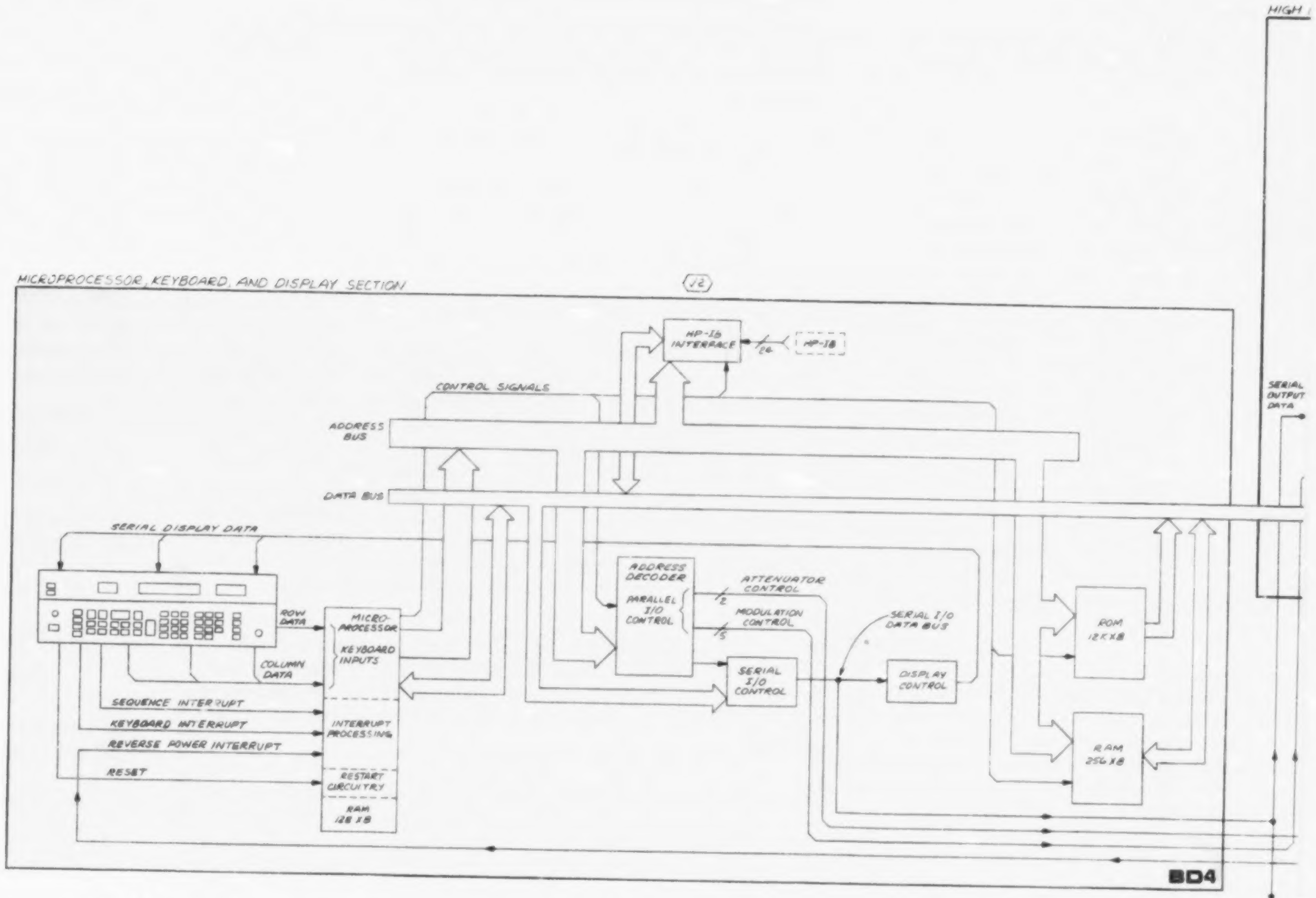
Abnormal Indication. If abnormal indication occurs, that is:

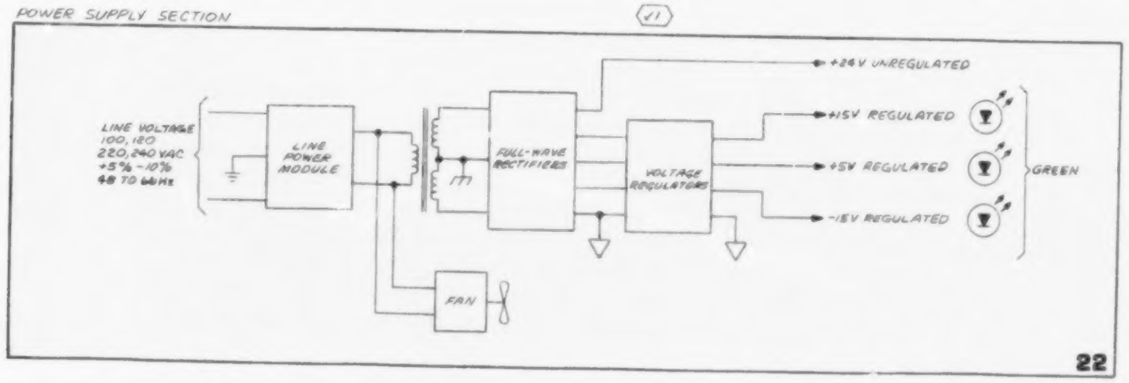
1. The MODULATION display is incorrect, go to Service Sheet BD4.

2. Amplitude modulation level is incorrect, go to Service Sheet BD2.

3. Frequency modulation level is incorrect, go to Service Sheet BD3.

4. Modulation rate is incorrect, go to Service Sheet 6.


HIGH
MICROPROCESSOR, KEYBOARD, AND DISPLAY SECTION
J2
HP-IB INTERFACE
24
HP-IB
CONTROL SIGNALS
ADDRESS BUS
DATA BUS
SERIAL DISPLAY DATA
SERIAL OUTPUT DATA
ROW DATA
COLUMN DATA
MICRO-PROCESSOR
KEYBOARD INPUTS
INTERRUPT PROCESSING
RESTART CIRCUITRY
RAM 128 X 8
SEQUENCE INTERRUPT
KEYBOARD INTERRUPT
REVERSE POWER INTERRUPT
RESET
ADDRESS DECODER
PARALLEL I/O CONTROL
ATTENUATOR CONTROL
2
MODULATION CONTROL
5
SERIAL I/O CONTROL
SERIAL I/O DATA BUS
DISPLAY CONTROL
ROM 12K X 8
RAM 256 X 8
BD4


POWER SUPPLY SECTION
J1
LINE VOLTAGE 100, 120 220, 240 VAC +5% -10% 48 TO 66Hz
LINE POWER MODULE
FULL-WAVE RECTIFIERS
VOLTAGE REGULATORS
FAN
+24V UNREGULATED
+15V REGULATED
+5V REGULATED
-15V REGULATED
GREEN
22

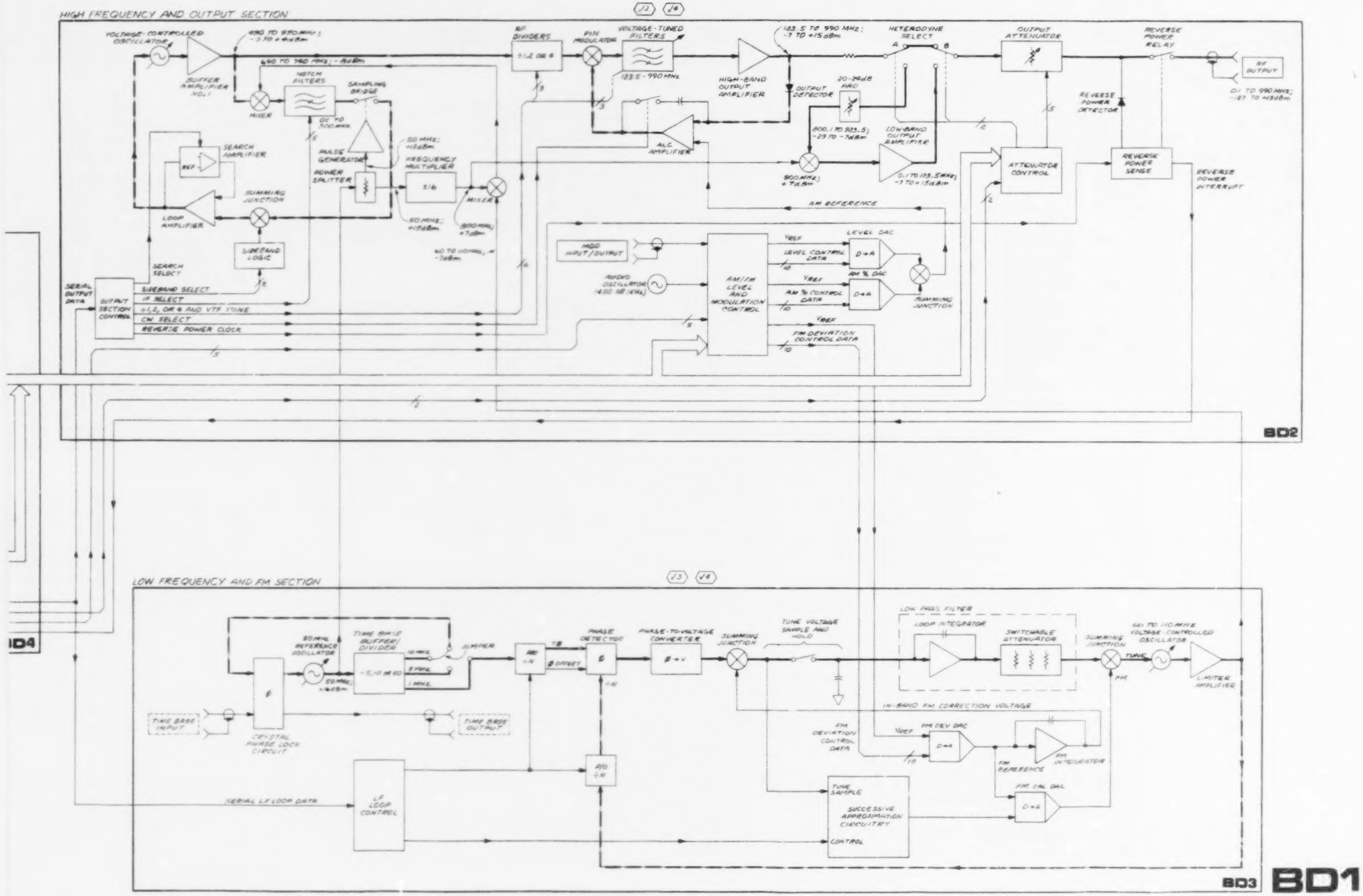

HIGH FREQUENCY AND OUTPUT SECTION
J3
J4
VOLTAGE-CONTROLLED OSCILLATOR
BUFFER AMPLIFIER NO. 1
490 TO 990 MHz; -3 TO +4 dBm
690 TO 740 MHz; -8 dBm
MIXER
NOTCH FILTERS
DC TO 300 MHz
SAMPLING BRIDGE
PULSE GENERATOR
POWER SPLITTER
50 MHz; +13 dBm
50 MHz; +15 dBm
FREQUENCY MULTIPLIER
X16
MIXER
800 MHz; +7 dBm
60 TO 110 MHz; -7 dBm
SEARCH AMPLIFIER
REF
SUMMING JUNCTION
LOOP AMPLIFIER
SIDEBAND LOGIC
SEARCH SELECT
SERIAL OUTPUT DATA
OUTPUT SECTION CONTROL
SIDEBAND SELECT
IF SELECT
÷1, 2, OR 4 AND VTF TUNE
CW SELECT
REVERSE POWER CLOCK
RF DIVIDERS
÷1, 2 OR 4
PIN MODULATOR
VOLTAGE-TUNED FILTERS
123.5 - 990 MHz
ALC AMPLIFIER
HIGH-BAND OUTPUT AMPLIFIER
123.5 TO 990 MHz; -7 TO +15 dBm
OUTPUT DETECTOR
20-24 dB PAD
800.1 TO 923.5; -23 TO -7 dBm
800 MHz; +7 dBm
LOW-BAND OUTPUT AMPLIFIER
0.1 TO 123.5 MHz; -7 TO +15 dBm
HETERODYNE SELECT
A
B
OUTPUT ATTENUATOR
ATTENUATOR CONTROL
REVERSE POWER RELAY
REVERSE POWER DETECTOR
REVERSE POWER SENSE
REVERSE POWER INTERRUPT
RF OUTPUT
0.1 TO 990 MHz; -127 TO +13 dBm
AM REFERENCE
MOD INPUT/OUTPUT
AUDIO OSCILLATOR (400 OR 1 kHz)
AM/FM LEVEL AND MODULATION CONTROL
VREF
LEVEL CONTROL DATA
LEVEL DAC
D→A
AM % CONTROL DATA
AM % DAC
SUMMING JUNCTION
FM DEVIATION CONTROL DATA
BD2
BD4
LOW FREQUENCY AND FM SECTION
J3
J4
50 MHz REFERENCE OSCILLATOR
50 MHz; +1 dBm
TIME BASE BUFFER/DIVIDER
÷5, 10 OR 50
10 MHz
5 MHz
1 MHz
JUMPER
TIME BASE INPUT
CRYSTAL PHASE LOCK CIRCUIT
TIME BASE OUTPUT
RD ÷N
TB
Ø OFFSET
PHASE DETECTOR
÷N
PHASE-TO-VOLTAGE CONVERTER
Ø→V
RO ÷N
SERIAL LF LOOP DATA
LF LOOP CONTROL
SUMMING JUNCTION
TUNE VOLTAGE SAMPLE AND HOLD
LOW PASS FILTER
LOOP INTEGRATOR
SWITCHABLE ATTENUATOR
SUMMING JUNCTION
TUNE
FM
60 TO 110 MHz VOLTAGE-CONTROLLED OSCILLATOR
LIMITER AMPLIFIER
IN-BAND FM CORRECTION VOLTAGE
FM DEVIATION CONTROL DATA
VREF
FM DEV DAC
FM REFERENCE
FM INTEGRATOR
FM CAL DAC
TUNE SAMPLE
SUCCESSIVE APPROXIMATION CIRCUITRY
CONTROL
BD3
BD1

Figure 8-33. Overall Block Diagram

SERVICE SHEET BD2

HIGH FREQUENCY AND OUTPUT SECTION

TROUBLESHOOTING HELP

Service Sheet BD1
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

A8 Frequency Multiplier Assembly. The Frequency Multiplier Assembly multiplies the 50 MHz reference signal by 16 to obtain an 800 MHz signal. The reference signal is doubled four times for frequencies of 100, 200, 400, and 800 MHz. The output of each multiplier is passed through a bandpass filter for the output frequency of that stage to filter out the harmonics and subharmonics generated by the multiplier.

The 800 MHz signal is applied to the A6 Output Assembly and mixed with specific basic band frequencies (800.1 to 923.5 MHz) when output frequencies in the heterodyne band (100 kHz to 123.5 MHz) are selected. It is also applied to the Frequency Multiplier Buffer Amplifier No.1. The signal is amplified and then mixed with the 60 to 110 MHz output from the A3 Low Frequency Loop Assembly (see BD3). The output from the Mixer is a frequency between 690 and 740 MHz that is used to phase lock the high frequency loop. Before a frequency between 690 and 740 MHz is sent to the A4 High Frequency Loop Assembly, it is amplified by two Buffer Amplifiers and filtered by the Bandpass Filter. The 690 to 740 MHz Bandpass Filter filters out the 800 MHz and the Mixer products of 860 to 910 MHz. The Compensation Network is adjusted for a flat frequency response of ±1.5 dB at the input of the A4 High Frequency Loop Assembly.

A4 High Frequency Loop Assembly. The High Frequency Loop Assembly phase locks the 494 to 990 MHz basic band Voltage Controlled Oscillator (VCO) on the A5 High Frequency Oscillator Assembly. The output from this oscillator passes through the 1100 MHz Low-Pass Filter, Buffer Amplifier No.2, and the 450 MHz High-Pass Filter before being mixed with a frequency between 690 and 740 MHz from the A8 Frequency Multiplier Assembly. Both the upper and lower sidebands from the Mixer are used to obtain IF phase lock signals in 50 MHz steps from 0 to 250 MHz. The IF phase lock signal passes throuh the 260 MHz IF Input Filter and is amplified by the IF Buffer Amplifier. The notch filter for the specific IF is not selected which allows that IF signal to pass through the Notch Filters. The IF signal is then sampled at a 50 MHz rate by a pulse from the Pulse Generator that is driven by the 50 MHz Reference Oscillator signal. The output of the Sampling Bridge is a correction voltage proportional to the phase difference of the IF and 50 MHz reference signals. The correction voltage is amplified by the Sampler Amplifier, filtered by the 13 MHz Low-Pass Filter and applied to the Loop Amplifier. It is then fed back to correct the frequency of the VCO on A5.

The dc notch is not selected when the high frequency VCO output is 690 to 740 MHz. The Mixer then functions as a phase detector with both inputs at the same frequency. The Mixer's output is now a voltage proportional to the phase difference of the two inputs. All other circuits function as previously described in the high frequency loop.

SERVICE SHEET BD2 (Cont'd)

The eight bit data word used to control the high frequency loop is clocked serially into the HF Loop Data Storage/Drivers circuit. Five bits control the dc, 50, 100, 150, 200 and 250 MHz notch filters. Of these, the 150 and 200 MHz bits also control the Gain Compensation to compensate for the nonlinearity of the VCO frequency change with voltage. Another bit selects the Search Amplifier reference so the Loop Amplifier ramp will be in the direction required to sweep the VCO and phase lock the loop without sweeping the VCO to one end and then back to the lock frequency. The last two bits are for the Sideband Logic that prevents the VCO from locking at the wrong frequency. This is necessary because both the upper and lower sidebands from the Mixer are used for the IF frequencies of 50, 100, 150, 200 and 250 MHz to phase lock the 494 to 990 MHz VCO frequencies.

A5 High Frequency Oscillator Assembly. The High Frequency Oscillator generates the instrument's 494 to 990 MHz basic band frequencies. The VCO is tuned and locked by the A4 High Frequency Loop Assembly. The output of the VCO is amplified by Buffer Amplifier No. 1 and then applied through a 6 dB Pad to the High Frequency Loop Assembly to phase lock the VCO. It is also applied directly to the A6 Output Assembly.

A6 Output Assembly. The Output Assembly translates the 494 to 990 MHz basic band frequencies by dividing (123.5 to 990 MHz) or heterodyning (100 kHz to 123.5 MHz) the basic band frequencies. Each of the divide by 1, 2, and 4 bands is one octave. The output of the dividers passes through the PIN diode Modulator to the Voltage-Tuned Filters. Each filter's bandwidth is also one octave and tuned by the VCO tune voltage. The filters therefore track the VCO frequency and are biased on only when that band is selected. This selection of filters provides better isolation and filtering of the out-of-band spurious and harmonic frequencies.

The eight-bit data word is clocked serially into the Output Section Data Storage/Drivers circuit. Three bits control the dividers and three bits control the Voltage-Tuned Filters. The other two bits are used to select the CW mode and to clock the Reverse Power Sense circuit.

The output from the Voltage-Tuned Filters is amplified by the High-Band Output Amplifier and applied to the Output Detector and the A9 Attenuator Assembly. Output amplitude changes within the 10 dB range set by the step attenuator are controlled by the input to the Automatic Level Control (ALC) Amplifier from the Digital-to-Analog Converter (DAC) on the A10 Audio/Power Supply Assembly. The ALC amplifier has two inputs. One is the detected output voltage used to level the output. The other is the sum of the amplitude modulation voltage (ac) and the leveling voltage (dc) for amplitude changes within the 10 dB range set by the step attenuator and level

SERVICE SHEET BD2 (Cont'd)

correction for frequency response. The output of the ALC amplifier controls the current through the PIN diodes of the PIN Modulator which controls amplitude modulation and RF level into the output attenuator (−4 to +13 dBm).

When output frequencies from 100 kHz to 123.5 MHz are selected, the first switch (A) of the A9 Attenuator Assembly switches the output back to the A6 Output Assembly where the output frequencies of 800.1 to 923.5 MHz are mixed (heterodyned) with the 800 MHz from the A8 Frequency Multiplier Assembly. The difference frequency of 100 kHz to 123.5 MHz is filtered by a low-pass Diplex Filter, amplified by the Low-Band Output Amplifier, and returned to the A9 Attenuator Assembly through the second switch (B).

A9 Attenuator Assembly. The Attenuator Assembly is an electromechanical step attenuator that steps the output 120 dB in 10 dB steps. The output circuits are reverse power protected for inputs up to 50 watts. A voltage level of 3 volts will trigger the circuit and open the Reverse Power Relay. When a reverse power condition is detected by the Reverse Power Sense circuit, the RPI bit is generated to interrupt the Microprocessor. The AMPLITUDE Display will flash to indicate that a reverse power condition has been detected. The Reverse Power Relay will remain open until the source of reverse power is removed and the AMPTD key is pressed. At that time, the RCL bit, from the Output Data Storage/Drivers circuit on A6, resets the relay.

Ten of the fourteen data bits from the Attenuator Control circuits on the A10 Audio/Power Supply Assembly control the attenuator pads to attenuate the output signal by the amount selected. The remaining four bits control the heterodyne select sections of the Attenuator Assembly.

A10 Audio/Power Supply Assembly. The amplitude modulation and level circuits portion of the Audio/Power Supply Assembly are shown on BD2. The external modulation signal level must be set at the source and the output of the External Modulation Buffer is monitored by the Over and Under Modulation Comparators which control the HI EXT and LOW EXT LEDs (not shown) on the front panel to indicate when the input is too high or low.

The modulation signals are applied to the FM Deviation Summing Amplifier (shown on BD3) and to the AM% Summing Amplifier. The output of the AM% Summing Amplifier is used as a reference voltage by the AM% DAC. The digitally controlled output of the AM% DAC is summed with the dc level voltage from the Level DAC and applied to the input of the AM Reference Summing Amplifier. The AM reference is applied to the ALC Amplifier on A6. The +2 Vdc level is applied to the Level Buffer to produce a reference voltage which is used by the Level DAC before it is summed with the amplitude modulation signal.

Five 8-bit data words are strobed into the Modulation Control Latches each time a front panel or HP-IB modulation entry is made. These data words are used to control all modulation functions, the level of the modulation signals, and the reference level voltage applied to the ALC loop.

SERVICE SHEET BD2 (Cont'd)

TROUBLESHOOTING

General

Procedures for checking the High Frequency and Output Sections of the instrument are given below. The blocks or points to check are marked on the block diagram by a hexagon with a check mark and a number inside, e.g., ⟨√2⟩.

Test Equipment

Spectrum Analyzer	HP 8558B/181T
Modulation Analyzer	HP 8901A
Oscilloscope	HP 1222A

⟨√1⟩ RF Output and Attenuator Check

1. Set the Signal Generator's frequency to 500 MHz and amplitude to 0.0 dBm. Connect the RF OUTPUT to the spectrum analyzer's input.

2. Center the signal on the spectrum analyzer's display. Verify that the signal is locked at 500 MHz with an amplitude of 0.0 dBm.

   a) If signal is unlocked perform ⟨√3⟩.

   b) If no output, perform ⟨√2⟩.

   c) If amplitude is not 0.0 dBm ±3.0 dB, continue with ⟨√1⟩ step 3.

3. Reduce the Signal Generator's amplitude in 10 dB steps to −50 dBm. The amplitude should change 10 dB for each step.

   a) If the amplitude does not change in 10 dB steps, go to Service Sheet 7.

   b) If the amplitude changes in 10 dB steps perform ⟨√2⟩.

4. Set the Signal Generator's frequency to 100 MHz. If there is no output or the output is low, go to Service Sheet 5.

⟨√2⟩ Output Assembly Check

1. Set the Signal Generator's frequency to 50 MHz.

2. Measure the amplitude and frequency at the assembly input A6TP1 and output A6W14 with the spectrum analyzer.

   a) If the input is correct (500 MHz and −3 to +4 dBm), if the output level is low (less than −7 dBm) or if the frequency is incorrect, go to Service Sheet 4.

   b) If the input is low, go to Service Sheet 1.

◀ Overall Troubleshooting SERVICE SHEET BD1

SERVICE SHEET BD2 (Cont'd)

3. Set the Signal Generator's frequency to 300 MHz and then 150 MHz. Measure the output of the assembly with the spectrum analyzer. If the output level is low or the frequency is not 300 or 150 MHz, go to Service Sheet 5.

√3 Frequency Multiplier

1. Set the Signal Generator's frequency to 500 MHz.

2. Measure the 50 MHz input directly from W5 with the spectrum analyzer. If either level (+15 to +13 dBm) or frequency (50 MHz) is incorrect, go to Service Sheet 13.

3. Measure the 60—110 MHz input (100 MHz) directly from W3 with the spectrum analyzer. If the level (-7 to -9 dBm) is incorrect or frequency (100 MHz) is incorrect or unlocked, go to Service Sheet BD3.

4. Measure the output (690 to 740 MHz) of the FL1 Bandpass Filter. If either level (−1.5 to −9.5 dBm) or frequency (700 MHz) is incorrect, go to Service Sheet 3. If level and frequency are correct, go to Service Sheet 1 or Service Sheet 2.

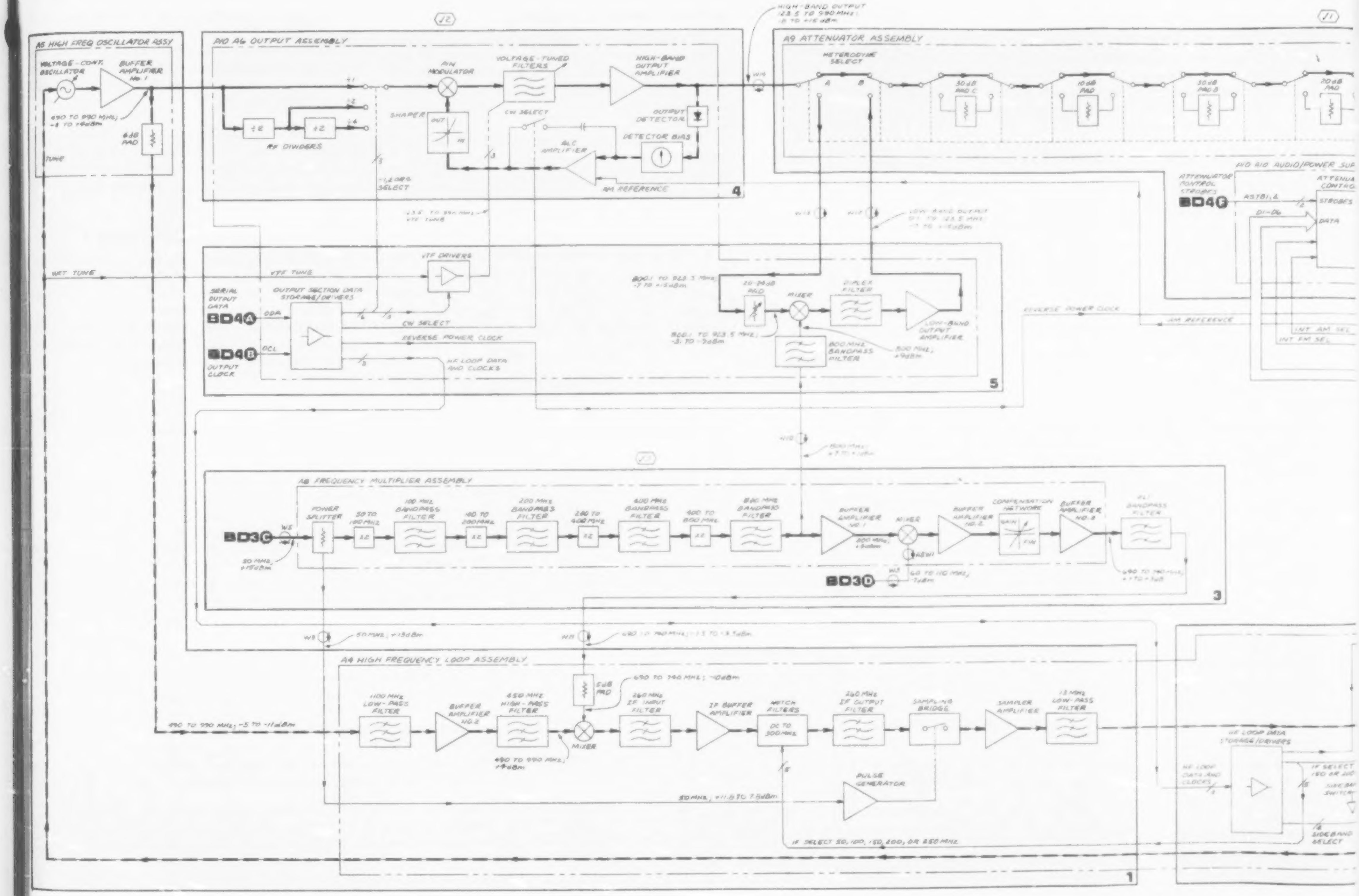
√4 Audio/Power Supply

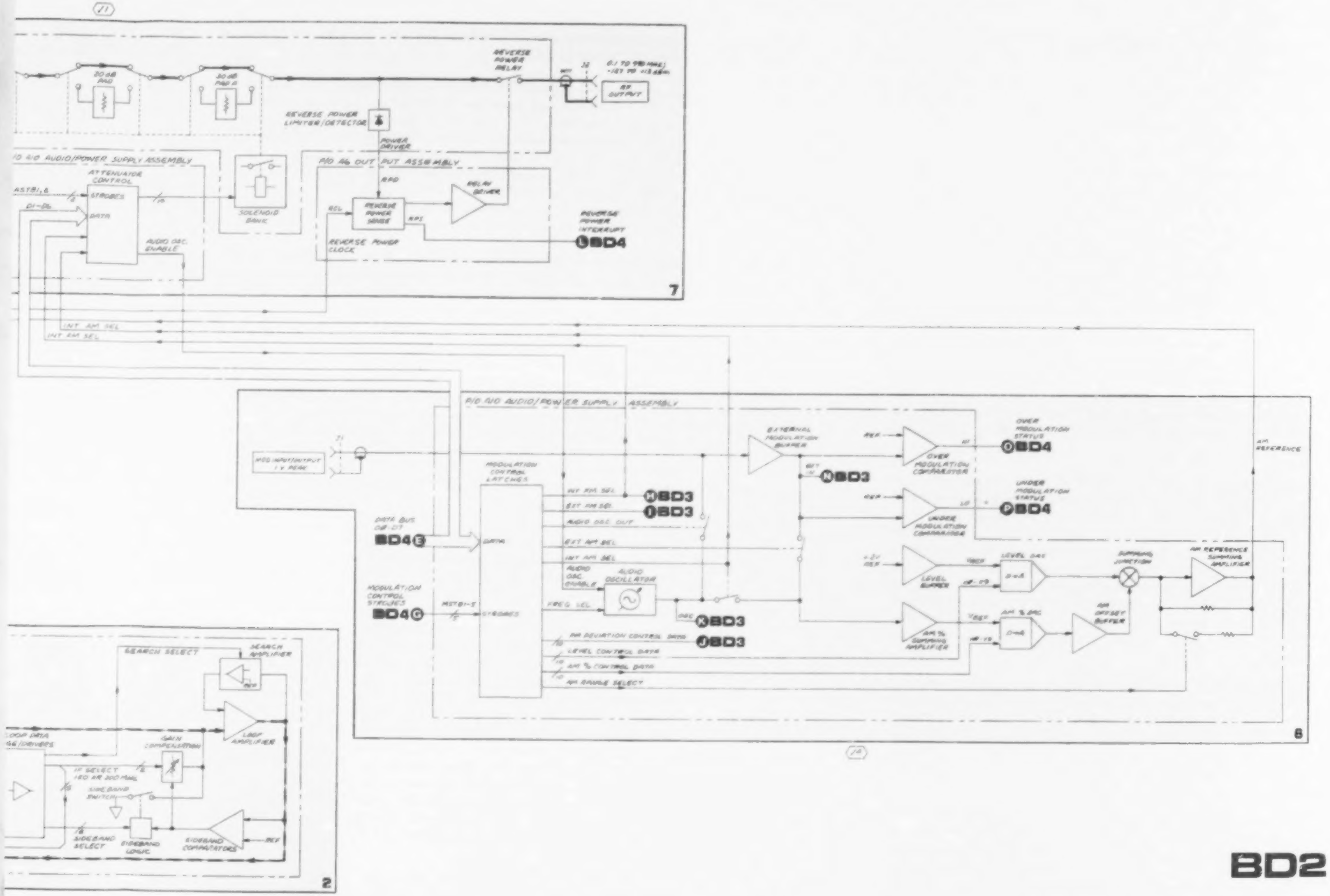
1. Set the Signal Generator's frequency to 500 MHz, amplitude 0.0 dBm, modulation INT 1 kHz, and AM 50%. Connect the RF OUTPUT to the modulation analyzer's input. Connect the modulation analyzer's modulation output to the oscilloscope's input.

2. Measure the amplitude modulation. It should be 50 ±5%. If the modulation level is incorrect, go to Service Sheet 6 (logic control circuits) or Service Sheet 4 (ALC PIN modulator).

3. Set the AM to off and select INT 1 kHz, FM 50 kHz.

4. Measure the frequency modulation. It should be 50 ±2.5 kHz. If the modulation level is incorrect, go to Service Sheet 6 (logic control circuits) or Service Sheet BD3.


J2
A5 HIGH FREQ OSCILLATOR ASSY
VOLTAGE-CONT. OSCILLATOR
BUFFER AMPLIFIER No. 1
490 TO 990 MHz; -8 TO +4dBm
6dB PAD
TUNE
P/O A6 OUTPUT ASSEMBLY
÷1
÷2
÷4
÷2
÷2
RF DIVIDERS
÷1,2 OR 4 SELECT
PIN MODULATOR
SHAPER
OUT
IN
VOLTAGE-TUNED FILTERS
CW SELECT
HIGH-BAND OUTPUT AMPLIFIER
OUTPUT DETECTOR
DETECTOR BIAS
ALC AMPLIFIER
AM REFERENCE
4
123.5 TO 990 MHz VTF TUNE
HIGH-BAND OUTPUT 123.5 TO 990 MHz; -8 TO +15 dBm
W14
J1
A9 ATTENUATOR ASSEMBLY
HETERODYNE SELECT
A
B
30 dB PAD C
10 dB PAD
30 dB PAD B
20 dB PAD
W13
W17
LOW-BAND OUTPUT 0.1 TO 123.5 MHz; -7 TO +15dBm
P/O A10 AUDIO/POWER SUP
ATTENUATOR CONTROL STROBES
BD4F
ASTB1,2
2
D1-D6
ATTENUA CONTRO
STROBES
DATA
REVERSE POWER CLOCK
AM REFERENCE
INT AM SEL
INT FM SEL
VFT TUNE
VTF TUNE
VTF DRIVERS
SERIAL OUTPUT DATA
BD4A
ODA
OUTPUT SECTION DATA STORAGE/DRIVERS
6
3
CW SELECT
REVERSE POWER CLOCK
BD4B
OCL
OUTPUT CLOCK
3
HF LOOP DATA AND CLOCKS
800.1 TO 923.5 MHz; -7 TO +15dBm
20-24 dB PAD
MIXER
DIPLEX FILTER
LOW-BAND OUTPUT AMPLIFIER
800.1 TO 923.5 MHz; -3 TO -9dBm
800 MHz BANDPASS FILTER
800 MHz; +9dBm
5
W10
800 MHz; +7 TO +10dBm
J3
A8 FREQUENCY MULTIPLIER ASSEMBLY
BD3C
W5
50 MHz; +15dBm
POWER SPLITTER
50 TO 100 MHz
×2
100 MHz BANDPASS FILTER
100 TO 200 MHz
×2
200 MHz BANDPASS FILTER
200 TO 400 MHz
×2
400 MHz BANDPASS FILTER
400 TO 800 MHz
×2
800 MHz BANDPASS FILTER
BUFFER AMPLIFIER NO. 1
800 MHz; +9dBm
MIXER
A8W1
BUFFER AMPLIFIER NO. 2
COMPENSATION NETWORK
GAIN
FIN
BUFFER AMPLIFIER NO. 3
RLT BANDPASS FILTER
BD3D
W3
60 TO 110 MHz; -7dBm
690 TO 740 MHz; +1 TO +3dB
3
W9
50 MHz; +13dBm
W11
690 TO 740 MHz; +1.5 TO +3.5dBm
A4 HIGH FREQUENCY LOOP ASSEMBLY
490 TO 990 MHz; -5 TO -11dBm
1100 MHz LOW-PASS FILTER
BUFFER AMPLIFIER NO.2
450 MHz HIGH-PASS FILTER
490 TO 990 MHz; +4dBm
5dB PAD
690 TO 740 MHz; -10dBm
MIXER
260 MHz IF INPUT FILTER
IF BUFFER AMPLIFIER
NOTCH FILTERS
DC TO 300 MHz
5
260 MHz IF OUTPUT FILTER
SAMPLING BRIDGE
SAMPLER AMPLIFIER
13 MHz LOW-PASS FILTER
PULSE GENERATOR
50 MHz; +11.8 TO 7.8dBm
IF SELECT 50, 100, 150, 200, OR 250 MHz
1
HF LOOP DATA STORAGE/DRIVERS
HF LOOP DATA AND CLOCKS
3
IF SELECT
150 OR 200
5
SIDEBAND SWITCH
6
SIDEBAND SELECT


11
20 dB PAD
20 dB PAD A
REVERSE POWER RELAY
W11
J2
0.1 TO 990 MHz; -127 TO +13 dBm
RF OUTPUT
REVERSE POWER LIMITER/DETECTOR
POWER DRIVER
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY
P/O A6 OUTPUT ASSEMBLY
ATTENUATOR CONTROL
ASTB1, 2
STROBES
DATA
D1-D6
AUDIO OSC. ENABLE
SOLENOID BANK
RPD
RELAY DRIVER
RCL
REVERSE POWER SENSE
RPI
REVERSE POWER CLOCK
REVERSE POWER INTERRUPT
L BD4
7
INT AM SEL
INT AM SEL
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY
J1
MOD INPUT/OUTPUT 1 V PEAK
MODULATION CONTROL LATCHES
DATA BUS D0-D7
BD4 E
DATA
MODULATION CONTROL STROBES
BD4 G
MSTB1-5
STROBES
INT AM SEL
H BD3
EXT AM SEL
I BD3
AUDIO OSC OUT
EXT AM SEL
INT AM SEL
AUDIO OSC ENABLE
AUDIO OSCILLATOR
FREQ SEL
OSC
K BD3
AM DEVIATION CONTROL DATA
J BD3
LEVEL CONTROL DATA
AM % CONTROL DATA
AM RANGE SELECT
EXTERNAL MODULATION BUFFER
EXT IN
N BD3
REF
OVER MODULATION COMPARATOR
HI
OVER MODULATION STATUS
O BD4
REF
UNDER MODULATION COMPARATOR
LO
UNDER MODULATION STATUS
P BD4
+2V REF
LEVEL BUFFER
VREF
LEVEL DAC
D-A
AM % SUMMING AMPLIFIER
VREF
AM % DAC
D-A
AM OFFSET BUFFER
SUMMING JUNCTION
AM REFERENCE SUMMING AMPLIFIER
AM REFERENCE
8
14
SEARCH SELECT
SEARCH AMPLIFIER
REF
LOOP DATA
/DRIVERS
LOOP AMPLIFIER
GAIN COMPENSATION
IF SELECT 160 OR 200 MHz
SIDEBAND SWITCH
SIDEBAND SELECT
SIDEBAND LOGIC
SIDEBAND COMPARATORS
REF
2

BD2

Figure 8-34. High Frequency and Output Section Block Diagram

SERVICE SHEET BD3

LOW FREQUENCY AND FM SECTION

TROUBLESHOOTING HELP

Service Sheet BD1
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

A3 Low Frequency Loop Assembly. The 50 MHz Reference Oscillator is a crystal oscillator that is used to phase lock the Voltage Controlled Oscillators (VCOs). Its output is also divided down to provide the 1 MHz time base. The rear panel TIME BASE OUTPUT signal is a jumper selectable frequency of 1, 5, or 10 MHz divided from the 50 MHz Reference Oscillator and coupled through the Crystal Phase Lock Circuit. For Option 001, a 10 MHz temperature-stabilized crystal oscillator is installed in the Signal Generator. The Option 001 oscillator output is available at the rear panel TIME BASE HIGH STABILITY OPTION connector (not shown). When connected to the TIME BASE INPUT connector, a phase lock is established between the high stability oscillator and the 50 MHz Reference Oscillator. The 1 MHz (divided from the 50 MHz Reference) is the clock 1 and 2 signal for counter 1 and 2 of the Triple Programmable Counter. These two counters supply the Time Base (TB) and φOffset signals to phase lock the low frequency (60 to 110 MHz) VCO to the reference.

Digital data is written to the LF Loop Shift Registers almost every time the frequency is changed. The data sets the frequency of the 60 to 110 MHz low frequency VCO. Data is written into Counter No. 1 (100 Hz resolution; divide-by-1 mode) and Counter No. 2 (1600 Hz resolution; divide-by-1 mode). Data is written into the Triple Programmable Counter when the VCO frequency crosses a 25.6 kHz band edge (Counter 0) or when the frequency resolution changes (Counters 1 and 2). Data is written to all counters when the instrument goes through the power-up routine. This occurs when the Signal Generator is connected to line voltage or reset with the front panel switch.

The Tune Sample Monostable circuit in the low frequency loop sets the LF Loop Ready line low. This line is connected to the Serial LF Loop Data input from the Microprocessor and signals the Microprocessor that the low frequency loop is ready to receive data. The Microprocessor will write the data words serially into the LF Loop Shift Registers and then parallel load the data into the applicable counters to correctly configure the instrument.

Counters No. 1 and No. 2 are up counters and the Triple Programmable Counter's counter 0 is a down counter. Counter No.1 is clocked by the signal from the low frequency VCO. The output of each counter then clocks the next counter dividing the low frequency VCO frequency down to 100 or 250 Hz at the Triple Programmable Counter's counter 0 (Out 0). The Out 0 signal is applied to the Terminal Count Flip-Flop to set a 100 Hz or 250 Hz window on the AND gate. One pulse from Counter No. 2 is gated to the terminal count ÷N output during the window duration. The divide-by-

SERVICE SHEET BD3 (Cont'd)

N signal is applied to the Phase-to-Voltage Converter to phase lock the low frequency loop.

The other clock to the Triple Programmable Counter (Clocks 1 and 2) is the 1 MHz derived from the 50 MHz Reference Oscillator. The output of counter 1 (Out 1) is 100 or 250 Hz, depending upon the Signal Generator frequency selected. This is the time base reference (TB) input to the Phase-to-Voltage Converter. The phase of the divide-by-N input is compared to the TB input to lock the low frequency VCO to the 50 MHz Reference Oscillator. The other input to the Phase-to-Voltage Converter is the 20 µs φ Offset pulse from the Triple Programmable Counter.

If a phase or frequency difference exists between the TB and divide-by-N inputs, the Phase-to-Voltage Converter generates a voltage that is proportional to the difference. This voltage is the correction voltage to the low frequency VCO and is applied to the Summing Junction. The Summing Junction output is applied to the Loop Summing Amplifier and then stored on the Tune Voltage Sample and Hold capacitor. The stored voltage is applied to the Loop Integrator. The Loop Integrator output is attenuated, buffered, and summed with the FM signal to tune and frequency modulate the VCO. The VCO's 60 to 110 MHz output is amplified by the Limiter Amplifier before being applied through the VCO Buffer to Counter No.1 and to the 110 MHz Low Pass Filter. The output of the filter is mixed with the 800 MHz on the A6 Frequency Multiplier Assembly (see BD2) to generate the 690 to 740 MHz signal that phase locks the high frequency loop.

On the A10 Audio/Power Supply Assembly, the internal and external frequency modulation signals from BD2 are applied to the FM Deviation Summing Amplifier, converted by the FM Deviation Digital-to-Analog Converter (DAC) programmed by the FM Deviation Control Data from the Microprocessor and amplified by the FM Deviation Amplifier. The FM Deviation Amplifier output is applied to the A3 Low Frequency Loop Assembly Summing Junction and then to the FM Reference Summing Amplifier whose output is the FM Reference input to the FM Cal DAC. The FM Cal DAC output is determined by the data inputs from the Successive Approximation Register (SAR). The output of the SAR is changed when FM Calibration takes place following each frequency change that causes data to be written to Counters 0, 1 or 2 of the Triple Programmable Counter. The calibrated output of the FM Cal DAC is applied to the Current-to-Voltage Converter and then to the DAC Offset Sample and Hold Buffer. This output is then summed with the Tune Voltage in the Summing Junction. The output from the Summing Junction is used to tune and frequency modulate the VCO.

Also included in the low frequency loop is the FM deviation calibration circuitry consisting of the FM Calibration Signal Generator and the Successive Approximation Register and Control Circuitry. Calibration is necessary to ensure that the FM deviation does not vary with oscillator frequency. Calibration is performed by setting

SERVICE SHEET BD3 (Cont'd)

the Successive Approximation Register using the Tune Voltage Sample output from the Loop Summing Amplifier as an input to the Successive Approximation Control Circuitry. A binary search sequence varies the frequency modulation drive signal level until the phase detected deviation of the FM loop signal is nulled by the signal from the FM Integrator.

During calibration the phase lock loop is opened. The frequency of the Voltage Controlled Oscillator (VCO) is fixed by the Tune Voltage Sample and Hold and the VCO is frequency modulated by the FM Calibration Signal Generator signal. The voltage from the phase-to-voltage converter is the detected frequency modulation from the VCO. This voltage is summed with (subtracted from) the In-Band FM Correction Voltage (the FM calibration reference signal) at the first Summing Junction. The resultant voltage is applied to the Loop Summing Amplifier whose output sets the SAR. The Tune Voltage Sample output from the Loop Summing Amplifier is equivalent to phase error. Calibration is complete when this voltage to the SAR is reduced to zero.

TROUBLESHOOTING

General

Procedures for checking the Low Frequency and FM Sections of the instrument are given below. The blocks or points to check are marked on the block diagram by a hexagon with a check mark and a number inside, e.g., √2.

Test Equipment

Digital Multimeter	HP 3465A
Frequency Counter	HP 5328A
Power Meter and Sensor	HP 436A/8482A
Oscilloscope	HP 1222A

√1 50 MHz Reference Oscillator Checks

1. Set the Signal Generator's frequency to 500 MHz, amplitude to 0.0 dBm and modulation off.

2. Connect the TIME BASE INPUT on the rear panel to the frequency counter's OUTPUT. With the jumper in the 10 MHz position check that the frequency is 10 MHz. If frequency is not correct, go to Service Sheet 13.

3. Connect the power meter to the 50 MHz reference output by removing W5. The power level should be +16 to +14 dBm. If the level is not correct, go to Service Sheet 13.

√2 Divider Circuit (Counter) Checks

1. Connect the frequency counter to test point A3J3 pin 5. The frequency should be 1 MHz divided from the 50 MHz reference. If the frequency is not correct, go to Service Sheet 13.

High Frequency
and Output Section
SERVICE SHEET BD2

SERVICE SHEET BD3 (Cont'd)

2. Connect the frequency counter to A3TP4, the buffered output of the LF Loop VCO. With the frequency set to 500 MHz, the VCO frequency should be 100 MHz. If the frequency is incorrect, go to Service Sheet 8.

3. Connect the oscilloscope to test points A3J3 pins 4, 6 and 7. The waveforms at pins 4 and 7 should be a 100 Hz squarewave; at pin 6 a 20 μs pulse at a 100 Hz rate. If any or all of the waveforms are not correct, go to Service Sheet 9.

√3 VCO Tune Voltage and FM Checks

1. Connect the multimeter to A3TP2 and measure the dc voltage. It should be 0.6 ±0.3 Vdc with the frequency set to 500 MHz (LF VCO frequency should be 100 MHz). If voltage is not correct, go to Service Sheet 10.

2. Increment the frequency up and down 5 MHz from 500 MHz. Voltage should change approximately 1.2 volts for each step. Return to 500 MHz. If the voltage change is incorrect, go to Service Sheet 10.

3. Connect the multimeter to feedthrough capacitor C15 (the +13 Vdc power supply for the LF Loop VCO). The voltage should be +13 ±2 Vdc with the noise less than 0.03 Vp-p. If the voltage or noise is incorrect, go to Service Sheet 10 or Service Sheet 22 (+15V power supply).

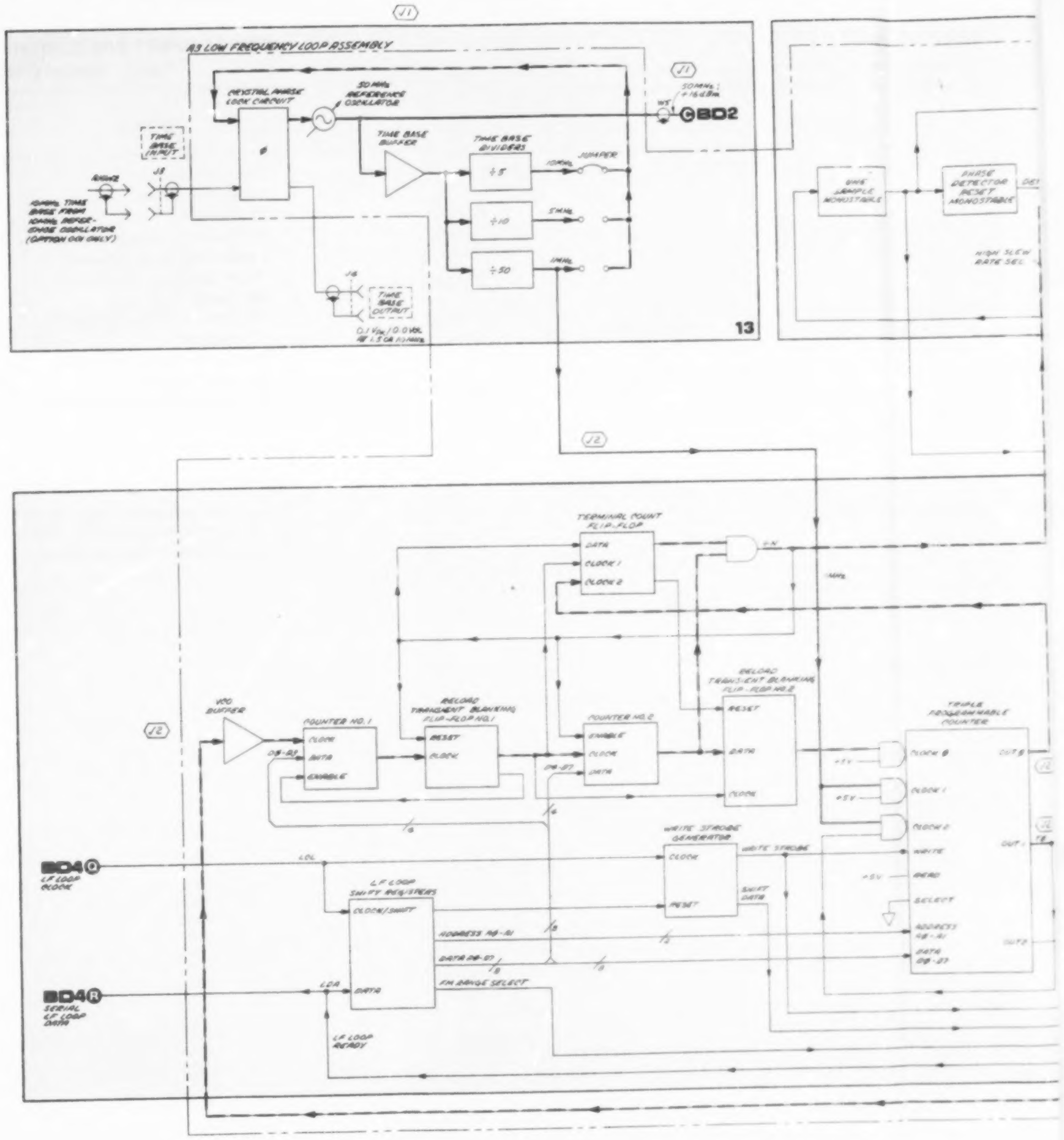
4. Connect the oscilloscope to A3TP2 and set the Signal Generator's modulation to 1 kHz INT. FM, 99 kHz deviation. The waveform should be a 1 kHz modulation signal at approximately 0.05 Vp-p. If incorrect, go to Service Sheet 11.

√4 Frequency Modulation Checks

1. Set the Signal Generator's frequency to 500 MHz, modulation to 1 kHz INT FM at 99 kHz deviation.

2. Connect the oscilloscope to A3J1 pin 7. The waveform should be 1 kHz at approximately 6.5 Vp-p. If incorrect, go to Service Sheet 6.

3. Connect the oscilloscope to test point A3J2 pin 13. The waveform should be a 1 kHz modulation signal of about 7.5 Vp-p. If incorrect, go to Service Sheet 12.



J1
A3 LOW FREQUENCY LOOP ASSEMBLY
J1
50 MHz
+16 dBm
W5
BD2
CRYSTAL PHASE LOCK CIRCUIT
50 MHz REFERENCE OSCILLATOR
TIME BASE INPUT
J3
W4W2
10 MHz TIME BASE FROM 10 MHz REFERENCE OSCILLATOR (OPTION 001 ONLY)
TIME BASE BUFFER
TIME BASE DIVIDERS
÷5
÷10
÷50
10 MHz
5 MHz
1 MHz
JUMPER
J6
TIME BASE OUTPUT
0.1 Vpk / 0.0 Vdc AT 1.5 OR 10 MHz
13
ONE SAMPLE MONOSTABLE
PHASE DETECTOR RESET MONOSTABLE
DET
HIGH SLEW RATE SEL
J2
TERMINAL COUNT FLIP-FLOP
DATA
CLOCK 1
CLOCK 2
÷N
1 MHz
J2
VCO BUFFER
COUNTER NO. 1
CLOCK
DATA
ENABLE
D0-D3
RELOAD TRANSIENT BLANKING FLIP-FLOP NO. 1
RESET
CLOCK
COUNTER NO. 2
ENABLE
CLOCK
DATA
D4-D7
RELOAD TRANSIENT BLANKING FLIP-FLOP NO. 2
RESET
DATA
CLOCK
TRIPLE PROGRAMMABLE COUNTER
+5V
CLOCK 0
CLOCK 1
CLOCK 2
WRITE
READ
SELECT
ADDRESS A0-A1
DATA D0-D7
OUT 0
OUT 1
OUT 2
TB
J2
WRITE STROBE GENERATOR
CLOCK
RESET
WRITE STROBE
SHIFT DATA
LCL
BD4 Q
LF LOOP CLOCK
LF LOOP SHIFT REGISTERS
CLOCK/SHIFT
DATA
ADDRESS A0-A1
DATA D0-D7
FM RANGE SELECT
LDA
BD4 R
SERIAL LF LOOP DATA
LF LOOP READY
8
4
8
2
8
8

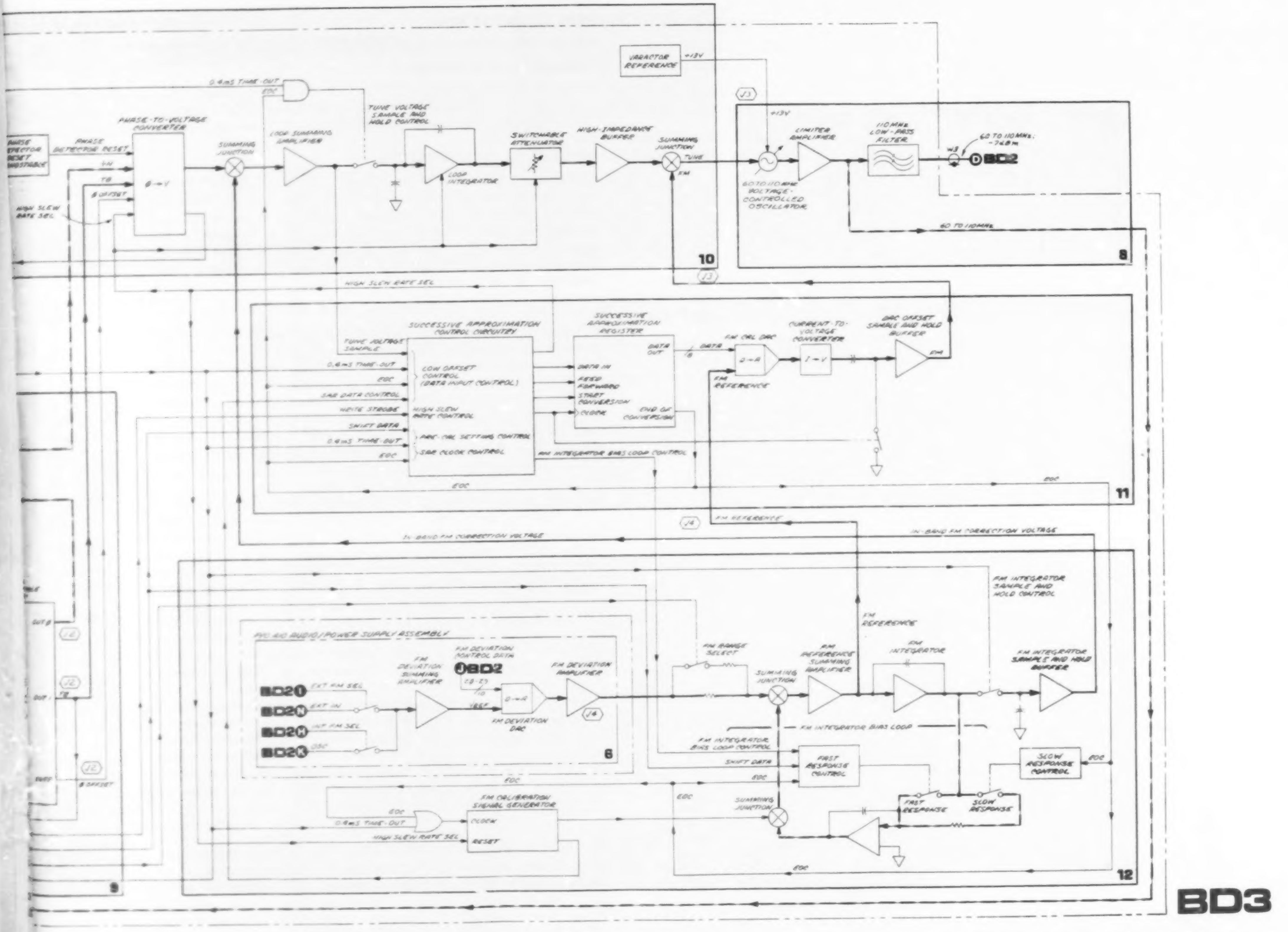

0.4mS TIME-OUT
EOC
VARACTOR REFERENCE
+13V
PHASE DETECTOR RESET MONOSTABLE
PHASE DETECTOR RESET
PHASE-TO-VOLTAGE CONVERTER
÷N
TB
θ OFFSET
HIGH SLEW RATE SEL
θ → V
SUMMING JUNCTION
LOOP SUMMING AMPLIFIER
TUNE VOLTAGE SAMPLE AND HOLD CONTROL
LOOP INTEGRATOR
SWITCHABLE ATTENUATOR
HIGH-IMPEDANCE BUFFER
SUMMING JUNCTION
TUNE
FM
10
J3
+13V
60 TO 110MHz VOLTAGE-CONTROLLED OSCILLATOR
LIMITER AMPLIFIER
110MHz LOW-PASS FILTER
W3
60 TO 110MHz; -7dBm
D BD2
60 TO 110MHz
8
HIGH SLEW RATE SEL
SUCCESSIVE APPROXIMATION CONTROL CIRCUITRY
TUNE VOLTAGE SAMPLE
0.4mS TIME-OUT
EOC
SAR DATA CONTROL
WRITE STROBE
SHIFT DATA
0.4mS TIME-OUT
EOC
LOW OFFSET CONTROL (DATA INPUT CONTROL)
HIGH SLEW RATE CONTROL
ARC-CAL SETTING CONTROL
SAR CLOCK CONTROL
FM INTEGRATOR BIAS LOOP CONTROL
SUCCESSIVE APPROXIMATION REGISTER
DATA IN
FEED FORWARD
START CONVERSION
CLOCK
DATA OUT
END OF CONVERSION
DATA
8
FM CAL DAC
D → A
FM REFERENCE
CURRENT-TO-VOLTAGE CONVERTER
I → V
DAC OFFSET SAMPLE AND HOLD BUFFER
FM
EOC
EOC
11
J4
FM REFERENCE
IN-BAND FM CORRECTION VOLTAGE
IN-BAND FM CORRECTION VOLTAGE
FM INTEGRATOR SAMPLE AND HOLD CONTROL
FM REFERENCE
PVO A10 AUDIO/POWER SUPPLY ASSEMBLY
FM DEVIATION SUMMING AMPLIFIER
FM DEVIATION CONTROL DATA
J BD2
CB-29
10
VREF
D → A
FM DEVIATION DAC
FM DEVIATION AMPLIFIER
J4
BD2 I
EXT FM SEL
BD2 N
EXT IN
BD2 H
INT FM SEL
BD2 K
OSC
6
FM RANGE SELECT
SUMMING JUNCTION
FM REFERENCE SUMMING AMPLIFIER
FM INTEGRATOR
FM INTEGRATOR SAMPLE AND HOLD BUFFER
FM INTEGRATOR BIAS LOOP
FM INTEGRATOR BIAS LOOP CONTROL
SHIFT DATA
EOC
FAST RESPONSE CONTROL
SLOW RESPONSE CONTROL
EOC
EOC
EOC
SUMMING JUNCTION
FAST RESPONSE
SLOW RESPONSE
FM CALIBRATION SIGNAL GENERATOR
EOC
0.4mS TIME-OUT
HIGH SLEW RATE SEL
CLOCK
RESET
EOC
12
OUT B
J2
J2
OUT
TB
SWP
J2
B OFFSET
9
BD3

Figure 8-35. Low Frequency and FM Section Block Diagram

SERVICE SHEET BD4

KEYBOARD, DISPLAY AND MICROPROCESSOR SECTIONS

TROUBLESHOOTING HELP

Service Sheet BD1
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

A1 Keyboard Assembly. The Keyboard Assembly consists of forty-eight pushbuttons or keys hard-wired in an eight-row by six-column matrix. Whenever a key is pressed, a row line is connected to a column line. This causes a keyboard interrupt to be issued to the Microprocessor. When the Microprocessor is interrupted, the row and column data is strobed into the Keyboard Data Latch/Shift Register and then serially shifted over the data bus to the Microprocessor.

A11 Microprocessor, Memory, and HP-IB Assembly. The data bus (D0 through D7) consists of eight bidirectional lines which are used to transfer 8-bit, positive-true data to and from the Microprocessor. The Microprocessor reads data from memory, the keyboard, and the HP-IB interface. Information on the data bus is buffered as it enters or leaves the Microprocessor. The Read/Write signal (R/W) from the Microprocessor is used to control the direction of data transfer on the data bus. This signal is buffered by one of the Microprocessor Control Line Buffers.

The address bus (A0 through A15) consists of sixteen unidirectional lines which are used to transfer the 16-bit, positive-true address from the Microprocessor. These address bits are buffered and then used to enable the ROM Select Decoder and address the Read Only Memory (ROM) and Random Access Memory (RAM) locations. In addition, the buffered address bits are decoded to produce modulation, attenuator, and serial Input/Output (I/O) control strobes. The serial I/O control changes the eight bits of parallel data to serial data and clocks this data to the high frequency loop and output section (see BD2), the low frequency loop (see BD3), and the display. It also clocks serial input data from the keyboard to the Microprocessor.

The Halt input to the Microprocessor halts program execution and the Reset input starts the Microprocessor from a power down condition. This signal sequence is used during initial start up of the instrument, after a power failure has occurred, or after the RESET/STBY/ON switch is momentarily set to the RESET position. When the Microprocessor is reset, it will enter its power-up subroutine to initialize the instrument.

The Maskable Interrupt Request (IRQ) input to the Microprocessor is used to interrupt program execution. Maskable interrupts occur whenever a key on the keyboard is pressed, a reverse power condition is detected, or an active low is on the rear panel connector J5 (SEQ). The three maskable interrupts plus the five status conditions (i.e., ON, Overmodulation, Undermodulation, HP-IB interrupt, and LF Loop Ready) all provide status inputs to the Interrupt Processing circuit which puts the instrument status information on the data bus.

SERVICE SHEET BD4 (Cont'd)

The Signal Generator memory consists of 348 bytes of RAM (128 internal to the Microprocessor and 12K bytes of ROM. The program used to control the operation of the Signal Generator is stored in the ROM.

All HP-IB data input/output, control, and handshake signals are buffered before being applied to the HP-IB General Purpose Interface Adapter.

A2 Display Assembly. Sixteen bits of serial display data (DDA) are sent from the Microprocessor to the Display Address and Data Shift Registers. Six of the bits are decoded to produce the eleven display strobes and two keyboard strobes. The keyboard strobes are used to strobe column and row data from the keyboard while the display strobes are used to strobe modulation, frequency, and amplitude display data into their respective control drivers and latches. The display data is decoded and latched to drive the applicable 7-segment display or LED annunciator.

TROUBLESHOOTING

General

Procedures for checking the Keyboard, Display and Microprocessor sections of the instrument are given below. The blocks or points to check are marked on the block diagram by a hexagon with a check mark and a number inside, e.g. ⟨√3⟩.

Test Equipment

HP-IB Controller	HP 9825A/98034A/98213A
Modulation Analyzer	HP 8901A

⟨√1⟩ Power-On or Reset Sequence

1. Switch the RESET-STBY-ON switch to RESET and back to ON to initiate the internal memory check. This check tests for a failure in ROM (Read Only Memory) and in RAM (Random Access Memory). During this check, all front panel indicators will light for approximately 1.5 seconds to provide a quick visual inspection of each front panel annunciator and display segment. All the display segments will display the number eight except the least significant FREQUENCY digit will be five and the AMPLITUDE most significant digit will be a one. If a memory failure is detected, all front panel annunciators and display segments will remain lit until any front panel key is pressed. If the memory check was successful, the front panel indicators will display a carrier frequency of 100.0000 MHz, an output amplitude of −127.0 dBm, and no modulation. All annunciators (except dBm) will remain off. Table 1 lists the conditions of the Signal Generator as a result of a successful initialization sequence.

◄ Low Frequency
and FM Section
SERVICE SHEET BD3

SERVICE SHEET BD4 (Cont'd)

Table 1. Initialized Conditions

Parameter	Initialized Condition
Carrier Frequency	100.0000 MHz
Output Amplitude	-127.0 dBm
AM Depth	0%
FM Peak Deviation Frequency	0.0 kHz
Carrier Frequency Increment	10.0000 MHz
Output Amplitude Increment	10.0 dB
AM Depth Increment	1%
FM Peak Deviation Frequency Increment	1.0 kHz
Coarse and Fine Tune Pointer	10.0000 MHz
Sequence Counter	0
All 10 Internal Storage Registers	100.0000 MHz and -127.0 dBm with no modulation

If the reset sequence is not completed successfully, see Service Sheets 14 and 16. Perform the signature checks for the two Service Sheets.

√2 Keyboard and HP-IB Checks

1. Connect the Signal Generator's RF Output to the modulation analyzer's input.

2. Connect the HP-IB controller to the Signal Generator's HP-IB input connector.

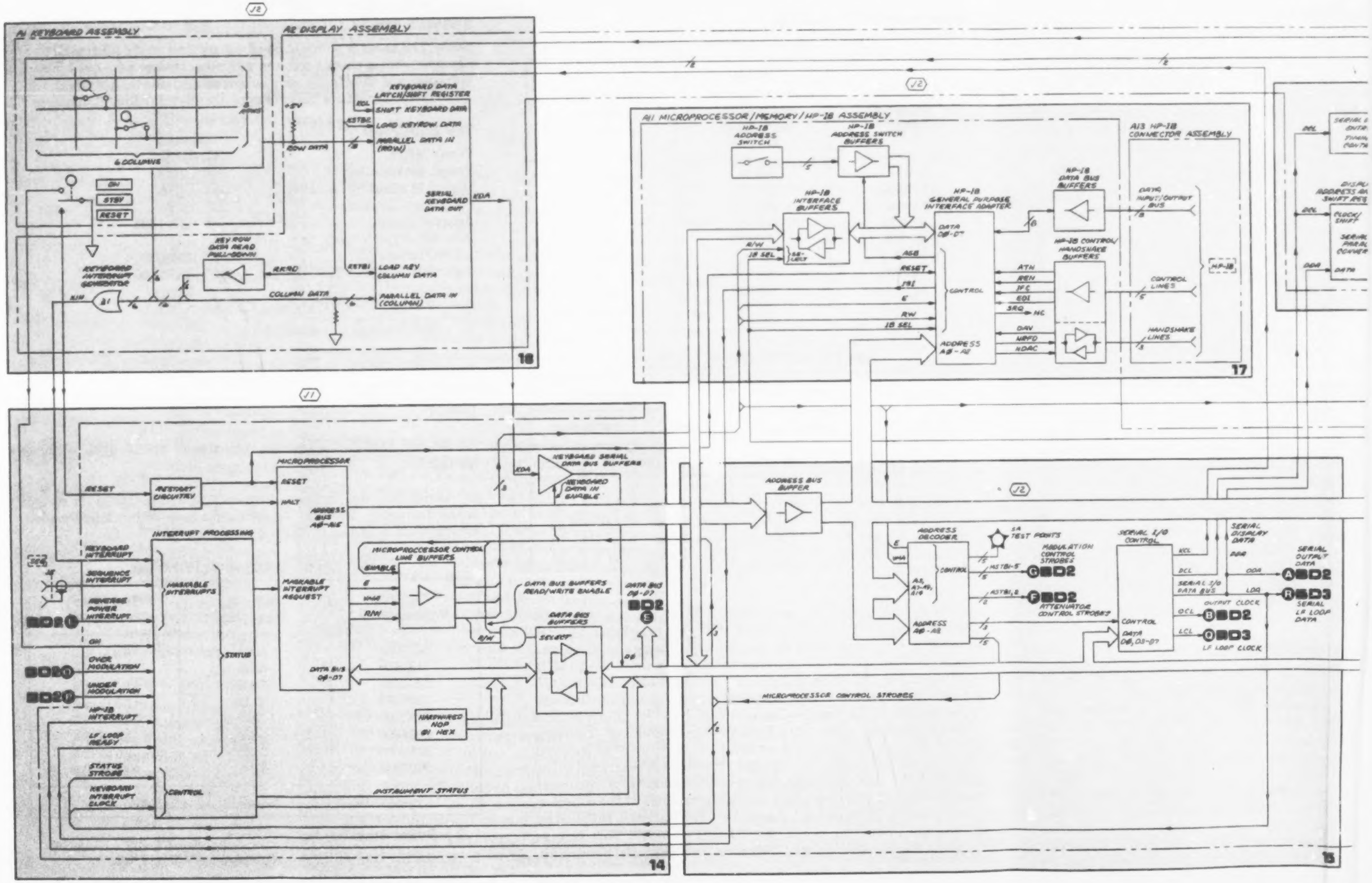
3. Enter modulation, frequency and amplitude data from the keyboard and the controller.

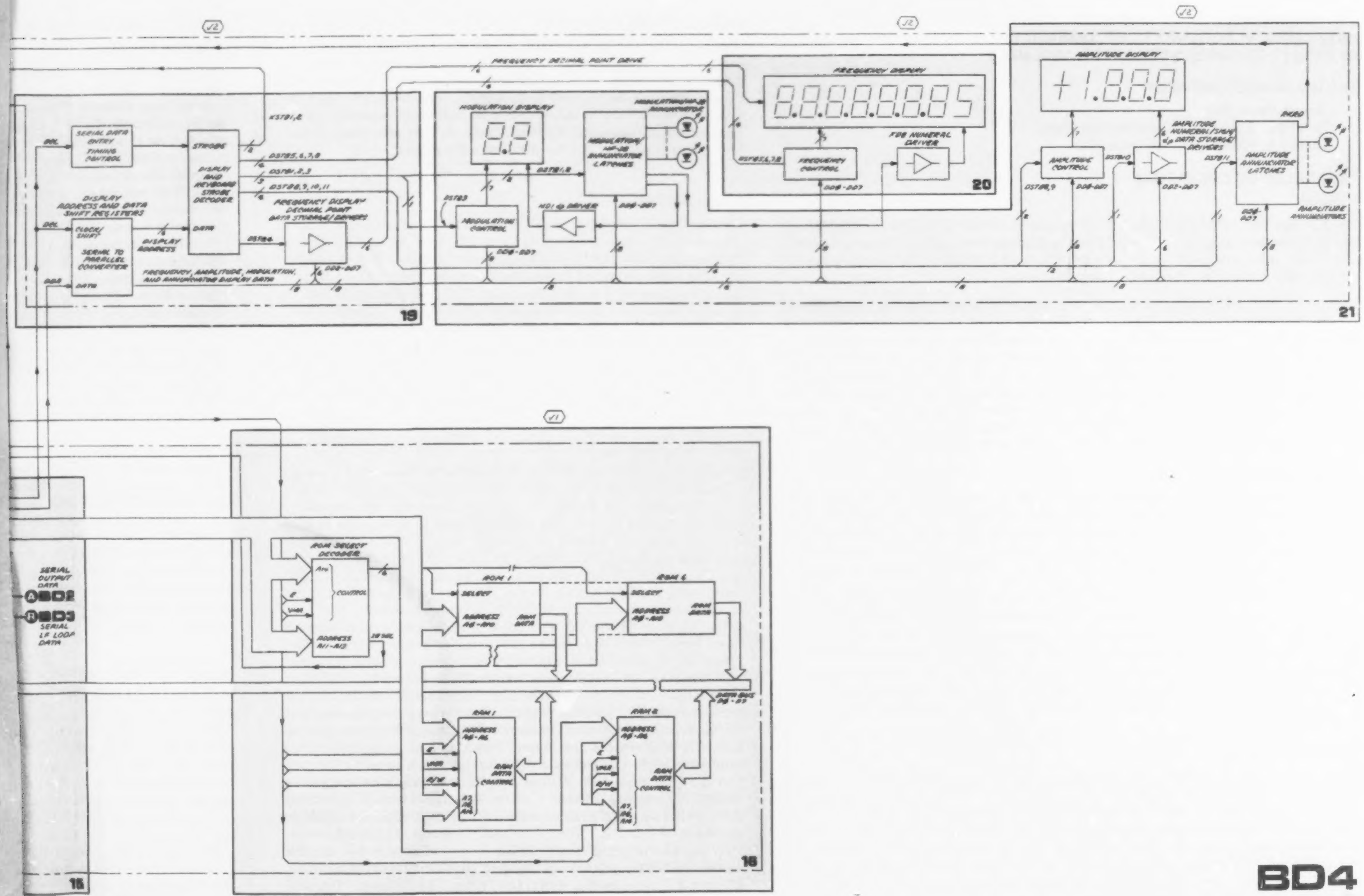
   a) If the RF output modes follow the data entered, but one or more of the displays do not, go to Service Sheets 19 and 20 or 21. Troubleshoot the appropriate strobes, latches, drivers and displays.

   b) If the displays follow the data entered but one or more of the RF output modes do not, go to Service Sheets BD2, BD3, or 15.

   c) If the output modes and displays follow data entered from the keyboard but not the HP-IB controller, go to Service Sheet 17.

   d) If the output and displays follow data entered from the HP-IB controller but not the keyboard, go to Service Sheet 18.


J2
A1 KEYBOARD ASSEMBLY
A2 DISPLAY ASSEMBLY
8 ROWS
6 COLUMNS
ON
STBY
RESET
+5V
ROW DATA
KEYBOARD DATA LATCH/SHIFT REGISTER
KCL
SHIFT KEYBOARD DATA
KSTBC
LOAD KEYROW DATA
PARALLEL DATA IN (ROW)
SERIAL KEYBOARD DATA OUT
KDA
KEY ROW DATA READ PULL-DOWN
RKRD
KSTBI
LOAD KEY COLUMN DATA
KEYBOARD INTERRUPT GENERATOR
KIN
≥1
COLUMN DATA
PARALLEL DATA IN (COLUMN)
18
A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY
HP-IB ADDRESS SWITCH
HP-IB ADDRESS SWITCH BUFFERS
HP-IB INTERFACE BUFFERS
R/W
IB SEL
SE-LECT
HP-IB GENERAL PURPOSE INTERFACE ADAPTER
DATA D0-D7
A0B
RESET
IRQ
E
RW
IB SEL
CONTROL
ADDRESS A0-A2
HP-IB DATA BUS BUFFERS
HP-IB CONTROL/HANDSHAKE BUFFERS
ATN
REN
IFC
EOI
SRQ
NC
DAV
NRFD
NDAC
A13 HP-IB CONNECTOR ASSEMBLY
DATA INPUT/OUTPUT BUS
CONTROL LINES
HANDSHAKE LINES
HP-IB
17
SERIAL OUTPUT TIMING CONTROL
DISPLAY ADDRESS SHIFT REGISTER
DCL
CLOCK/SHIFT
SERIAL PARALLEL CONVERTER
DDA
DATA
J1
RESET
RESTART CIRCUITRY
MICROPROCESSOR
RESET
HALT
ADDRESS BUS A0-A15
KDA
KEYBOARD SERIAL DATA BUS BUFFERS
KEYBOARD DATA IN ENABLE
INTERRUPT PROCESSING
KEYBOARD INTERRUPT
SEQUENCE INTERRUPT
REVERSE POWER INTERRUPT
MASKABLE INTERRUPTS
MASKABLE INTERRUPT REQUEST
ON
OVER MODULATION
UNDER MODULATION
HP-IB INTERRUPT
LF LOOP READY
STATUS STROBE
KEYBOARD INTERRUPT CLOCK
STATUS
CONTROL
BD2
BD2
BD2
MICROPROCESSOR CONTROL LINE BUFFERS
ENABLE
E
VMA
R/W
DATA BUS BUFFERS READ/WRITE ENABLE
DATA BUS D0-D7
DATA BUS BUFFERS
SELECT
R/W
HARDWIRED NOP 01 HEX
DATA BUS D0-D7
BD2 E
D0
INSTRUMENT STATUS
14
ADDRESS BUS BUFFER
J2
ADDRESS DECODER
E
VMA
A5, A7-A13, A14
ADDRESS A0-A2
CONTROL
SA TEST POINTS
MODULATION CONTROL STROBES
MSTB1-5
G BD2
ASTB1, 2
F BD2
ATTENUATOR CONTROL STROBES
SERIAL I/O CONTROL
KCL
DCL
SERIAL I/O DATA BUS
CONTROL
DATA D0, D3-D7
SERIAL DISPLAY DATA
DDA
ODA
SERIAL OUTPUT DATA
A BD2
LDA
R BD3
SERIAL LF LOOP DATA
OUTPUT CLOCK
OCL
B BD2
LCL
O BD3
LF LOOP CLOCK
MICROPROCESSOR CONTROL STROBES
15


J2
KSTB1,2
SERIAL DATA ENTRY TIMING CONTROL
STROBE
DISPLAY AND KEYBOARD STROBE DECODER
DATA
DSTB5,6,7,8
DSTB1,2,3
DSTB8,9,10,11
DSTB4
DISPLAY ADDRESS AND DATA SHIFT REGISTERS
CLOCK/SHIFT
SERIAL TO PARALLEL CONVERTER
DATA
DISPLAY ADDRESS
FREQUENCY DISPLAY DECIMAL POINT DATA STORAGE/DRIVERS
DD2-DD7
FREQUENCY, AMPLITUDE, MODULATION, AND ANNUNCIATOR DISPLAY DATA
19
FREQUENCY DECIMAL POINT DRIVE
MODULATION DISPLAY
MODULATION/HP-IB ANNUNCIATOR
MODULATION/HP-IB ANNUNCIATOR LATCHES
DSTB1,2
DSTB3
MODULATION CONTROL
DD0-DD7
MD1 dp DRIVER
FREQUENCY DISPLAY
FREQUENCY CONTROL
DSTB5,6,7,8
FDB NUMERAL DRIVER
20
AMPLITUDE DISPLAY
+1.888
AMPLITUDE CONTROL
DSTB8,9
DSTB10
AMPLITUDE NUMERAL/SIGN/dp DATA STORAGE/DRIVERS
DD2-DD7
DSTB11
AMPLITUDE ANNUNCIATOR LATCHES
RKBD
AMPLITUDE ANNUNCIATORS
21
J1
SERIAL OUTPUT DATA
A BD2
R BD3
SERIAL LF LOOP DATA
15
ROM SELECT DECODER
A14
CONTROL
E
VMA
ADDRESS A11-A13
ROM 1
SELECT
ADDRESS A0-A10
ROM DATA
ROM 6
RAM 1
ADDRESS A0-A6
R/W
A7, A8, A14
RAM DATA
RAM 2
DATA BUS D0-D7
18

BD4

Figure 8-36. Microprocessor, Keyboard and Display Section Block Diagram

SERVICE SHEET 1
P/O A4 HIGH FREQUENCY LOOP ASSEMBLY
A5 HIGH FREQUENCY OSCILLATOR ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD2
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The Voltage Controlled Oscillator (VCO) oscillates over a range of 494 to 990 MHz. It is tuned over this range by a −7.5 to +12 volt triangular wave signal. The output signal passes through a power splitter and is coupled to the RF Dividers (on the way to the RF Output) and to the High Frequency Loop Assembly.

Within the High Frequency Loop, the VCO signal is mixed with the phase locked signal (690-740 MHz). As the VCO is searching for its lock point, the mixer generated sidebands pass through a bank of selectable notch filters. The appropriate filter is turned off thus allowing the selected IF sideband to pass. The sampling bridge phase-compares the sideband (a multiple of 50 MHz) with a 50 MHz reference signal. When the correct sideband appears at the sampling bridge, the output to the loop with the amplifier (which up to now has been a continuously changing voltage) becomes a dc voltage. This voltage sets the High Frequency Loop Phase lock point. For more information, refer to the Loop and Search Amplifiers in Service Sheet 2.

Voltage Controlled Oscillator

The tune voltage ramp and the phase lock voltage are supplied to the varicaps CR1 and CR2 by the Loop Amplifier in conjunction with the Search Amplifier. This voltage is coupled into the VCO by the Low Pass Filter composed of L5, L6 and C10. The LPF also isolates the VCO. Varicaps CR1 and CR2 tune the tank circuit which includes inductor L8. Capacitors C11, C13 and C14 provide RF ground for the tank circuit. Varicap bias voltage of approximately −7.5 Vdc is obtained from voltage divider R20, R21 and the −15V (F2) supply. The output of the tank circuit is coupled into the VCO transistor Q3 by capacitor C15. Transistor Q3 is dc biased by R20, R21, L10 and R23. Inductor L11 causes a negative resistance to appear at the emitter of Q3 while C18 removes the negative resistance effect of L11 at low frequencies. Resistor R22 and capacitor C20 moderate the negative resistance effect looking into the emitter and reduce the Q of L11. Capacitors C19 and C21 bypass RF frequencies and power supply noise to ground. Power supply noise or other noise will frequency modulate the oscillator output.

Buffer Amplifier No. 1

Output of the VCO is coupled to the base of Q2 through capacitors C1 and C5 and the 6 dB isolation pad R3, R4, and R5. The collector current of Q3 flows through R1 and R2 to dc bias the base of Q1. Since the emitter of Q1 is also connected to the +15V (F4) supply by R6, the emitter voltage will be approximately 0.6 Vdc more positive than the base. The current in resistor R6 is determined by the voltage difference between the +15 volt supply and the voltage at the emitter of Q1. The current through R6 takes two paths. One path for the current is into the emitter of Q1 and out at its collector. This current is multiplied by the common-base current gain of Q1 which is approximately one. This is the base current for Q2. The other path for the current from R6 flows through R8 and L3 and is the collector current for Q2. The actual base and collector currents depend on the DC current gain of Q2. Therefore, the total current from R6 is

SERVICE SHEET 1 (Cont'd)

the sum of the base current and collector current of Q2. This is equal to the emitter current of Q2. The result is that the bias circuit gives accurate and stable control of the emitter current of Q2. Inductor L4 is used to match the collector to the output. Inductor L2, resistor R9, and capacitor C7 are for collector-to-base feedback. Capacitor C9 is a frequency compensation capacitor for Q2 emitter resistors R10 and R11. Capacitors C2, C3, C4, and C6 are filter capacitors.

Power Splitter

Output of Q2 is coupled to the Power Splitter by capacitor C8 and a 2 dB pad which consists of R12, R13, and R14. One output of the Power Splitter goes to the RF Dividers which are located on the A6 Assembly. The other output of Power Divider goes through the 6 dB pad which consists of R16, R17, R19, and C17 to Buffer Amplifier #2 which is located on the A4 Assembly. This output is used to phase lock the VCO. Coupling capacitor C17 passes the RF signal and blocks the +15V (F5) from inductor L12 which also acts to block the RF signal. The RF signal and +15V (F5) are both connected to Buffer Amplifier #2 by the same wire. The Power Splitter also serves to isolate the RF output path from the 690-740 MHz input to Mixer U1.

Buffer Amplifier No. 2

Output of the A5 Assembly is ac coupled to the base of Q2 through 1100 MHz Low Pass Filter composed of L6, L7, L8, L9, C9, C10, and C11. Capacitor C14 blocks the +15 Vdc from the A5 Assembly. Resistors R4 and R5 form the voltage divider to dc bias the base of Q1. The current in resistor R8 is determined by the voltage difference between the +15 Vdc supply and the voltage at the emitter of Q1. The current through R8 takes two paths. One path is into the emitter of Q1 and out at its collector. This current is multiplied by the common-base current gain of Q1 which is approximately one. This is the base current for Q2. The other path for the current from R8 flows through R15 and L3 and is the collector current for Q2. The actual base and collector current depends on the dc current gain of Q2. Therefore, the total current from R8 is the sum of the base current and collector current to Q2. This is equal to the emitter current of Q2. The result is that the bias circuit gives accurate and stable control of the emitter current of Q2. Inductor L14 is used to match the collector to the output. Inductor L12, resistor R16 and capacitor C18 are for collector to base feedback. Capacitor C13 and C15 are filter capacitors. Buffer Amplifier #2 amplifies the VCO's 494-990 MHz signal to about +5 dBm. The signal is then ac coupled through the 450 MHz high-pass filter C21, C22, C23, L17 and L18 to one input of Mixer U1. The other input to Mixer U1 is a 690 to 740 MHz signal of approximately −2 dBm from the Frequency Multiplier Assembly A8. The factory selected pad, that consists of resistors R6, R7, and R10 reduces this signal to −7 dBm. The difference frequencies from Mixer U1 are passed through the IF Input Filter which consists of inductors L19, L21, L26 and capacitors C33, C26, C38, and C41. The output of Mixer U1 is terminated by C30 and R23. C43 and L28 form a notch filter which is tuned to 300 MHz.

IF Buffer Amplifier

One of the IF sideband frequencies from Mixer U1 are phase-compared to the 50 MHz Reference to phase-lock the High Frequency Loop. Refer to Table 1 for a listing of these signals. Table 2 can be used with Table 1 to find the sideband for any frequency selected. At the 0 MHz (dc) frequency, the Mixer acts as a phase dectector. The IF Buffer Amplifier transistors Q3 and Q4 are biased off until one of the Notch Filters is selected (turned off). When a notch filter control line is pulled low by the output of the IF Drivers (See Service Sheet 2), the selected notch filter is turned off by biasing on one of the diodes CR7, CR8, CR9, CR10, or CR11 which shorts out the series capacitor of the notch filter C53, C61, C64, C67, or C70. The notch filter that is turned off then becomes a parallel tuned circuit. It now is a bandpass filter for the selected IF frequency. When the selected diode is biased on, current is drawn from the +15 Vdc supply through resistor R29 which biases on transistor Q4. Transistor Q4 will bias transistors Q3 and Q5 on. Q3 will amplify the IF signal by approximately 6 dB and Q5 will ground any dc voltage from Mixer U1. Resistor R31 provides collector to base feedback in the IF Buffer Amplifier and resistor R39 and capacitor C50 increase the gain at the high IF frequencies to compensate for the increased losses in the input and output filters.

The DC Notch Filter Q5 is used when the VCO's frequency to Mixer U1 is from 690 to 740 MHz (the same as the input from the Frequency Multiplier Assembly A8). The two frequencies will track and the mixer will function as a phase detector. The mixer's dc output voltage is proportional to the phase difference of the two inputs. The output of Mixer U1 looks into a high impedance and not into 50 ohms since the DC Notch Filter and the IF Buffer Amplifier are turned off. Consequently, the voltage level is 6 dB higher in the dc notch range. Since transistors Q3, Q4 and Q5 are all off, Q5 does not ground the dc voltage from Mixer U1. The dc voltage is sampled and fed back to keep the VCO locked.

Sampling Bridge and Pulse Generator

The output of the IF Buffer Amplifier or the DC Notch Filter is the input to be sampled by the Sampling Bridge. The 50, 100, 150, 200 or 250 MHz IF frequency is filtered by the 300 MHz Notch Filter (C85, C86 and L40) and the IF Output Filter (L20, L22, L27, C35, C37, C80, and C81). Resistor R24 and capacitor C79 provide a 50Ω impedance looking into the Sampling Bridge. The 50 MHz Reference Oscillator drives the Sampling Bridge. The 50 MHz, +13 dBm reference signal is applied to transformer T1. Resistors R1, R2 and R3 form a 2 dB pad and inductor L11 and capacitor C12 are used for impedance matching. T1 is the input to the Pulse Generator where 50 MHz pulses are generated by biasing the step recovery diode CR2 on and off. The IF input to the Sampling Bridge is sampled every 20 ns for 1.5 ns. When CR2 is biased off, inductors L15 and L16 will turn the Sampling Bridge on for 1.5 ns. The sampled output is stored in capacitors C28 and C29 and the dc voltage is applied to the 13 MHz Low Pass Filter through R27. When the level of the voltage from the sampler is changing at a rate greater than 80 Hz, the voltage is coupled through C29 and C34 to the 13 MHz Low Pass Filter. FET Q6 provides a high impedance for the sampling bridge to drive and transistor Q7 provides a low impedance output to drive the 13 MHz Low Pass Filter. The Sampler Amplifier, which consists of Q6 and Q7, is a voltage follower feedback amplifier which functions to increase the bandwidth of the sampler. Transistor Q7 and FET Q6 are always turned on. Approximately 5 mA flows through R22 and Q6 providing 0.6 Vdc between the base and emitter to bias Q7 on. The sampled voltage is stored in capacitor C29 and C28 which is connected to the gate of Q6. For a small voltage change on the gate of Q6 more current must go through R26 to produce the voltage change at the collector-source junction of Q6 and Q7. A portion of the current is supplied by Q6 and the remainder is collector current from Q7. This voltage change is also coupled through C16 to increase the sampler bandwidth.

Table 1. Loop and IF Sideband Frequencies

High Frequency VCO Output (MHz)	Difference Frequencies from Mixing LF Loop Output and 800 MHz (MHz)	'Not Selected' IF Sideband (MHz)
494-540	694-740	-200
540-590	690-740	-150
590-640	690-740	-100
640-690	690-740	-50
690-740	690-740	DC
740-790	690-740	+50
790-840	690-740	+100
840-890	690-740	+150
890-940	690-740	+200
940-990	690-740	+250

Table 2. RF OUTPUT versus HF Loop Output

Output Divider Mode	Output Frequency (MHz)		Bandwidth (MHz)			
			Total		IF Sideband	
	RF	HF Loop	RF	HF Loop	RF	HF Loop
÷1/ Heterodyne	0.1-123.5	800.1-923.5	123.4	123.4	50	50
÷4	123.5-247	494-988	123.5	494	12.5	50
÷2	247-494	494-988	247	494	25	50
÷1	494-990	494-990	496	496	50	50

TROUBLESHOOTING

Procedures for checking circuits of the A5 High Frequency Oscillator Assembly and P/O A4 High Frequency Loop Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g., √1. Fixed voltages are shown on the schematic inside a hexagon, e.g. 2V±0.2V. Transistor bias voltages are shown without tolerances.

Test Equipment

Power Meter	HP 436A
Power Sensor	HP 8482A
Digital Multimeter	HP 3465A
Frequency Counter	HP 5328A
Adapter Probe	HP 1250-1598
Adapter, Type-N male to BNC female	HP 1250-0780
Cable-BNC male to SMC female	HP 08662-60080

√1 Voltage Tuned Oscillator Check

1. Check the bias voltage on Q3.

2. Connect counter to TP5 using the cable and adapters.

3. Connect counter time base to the Signal Generator's TIME BASE INPUT.

4. Set the Signal Generator's output level to -10 dBm without modulation.

5. Verify that the oscillator frequency is within ±1000 Hz of the center frequency, and that the tune voltage is within tolerance for each frequency shown in Table 3.

Table 3. VCO Frequency versus Tune Voltage

Oscillator Frequency (MHz)	Typical Tune* Voltage (Vdc)	Tune Voltage* Tolerance (Vdc)
500.0000	-6.715	-6.9 to -6.0
510.0000	-6.528	-6.7 to -5.8
520.0000	-6.327	-6.5 to -5.6
530.0000	-6.112	-6.3 to -5.4
540.0000	-5.888	-6.1 to -5.6
550.0000	-5.650	-5.9 to -5.4
715.0000	-0.905	-3.0 to +2.5
990.0000	+8.945	+2.5 to +12

*Voltage measured at TUNE signal location (white/black/orange wire.)

√2 Buffer Amplifier No. 1

1. Check the bias voltages on transistor A5Q1 and Q2.

2. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

◀ Microprocessor, Keyboard and
Display Section
SERVICE SHEET BD4

SERVICE SHEET 1 (Cont'd)

3. Measure the power at the test points shown in Table 4. Connect the power sensor to the test points using the cable and adapters.

√3 Buffer Amplifier No. 2

1. Check the bias voltages on A6Q1 and Q2.

2. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

3. Measure the power at the test points shown in Table 5. Connect the power sensor to the test points using the cables and adapters.

√4 IF Input Filter

1. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

2. Connect power sensor to test points indicated in Table 6 using cable and adapters. Verify that the power levels are correct.

√5 IF Buffer Amplifier

1. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

2. Measure and verify the voltages shown in Table 7.

3. Disconnect the TUNE voltage to the A5 High Frequency Oscillator Assembly. Measure the voltage at TP8. It should be 0.000 ±0.005 Vdc.

√6 Notch Filters

1. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

2. Connect counter to TP8 using cable and adapters.

3. Measure and verify the IF Filter select voltages in Table 8.

√7 Pulse Generator, Sampling Bridge

1. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

2. Connect power sensor to the test points indicated in Table 9 using cable and adapters. Measure and verify the power levels.

3. Ground TP13 and disconnect the TUNE voltage to the High Frequency Oscillator Assembly A5. Remove the wire to the feedthrough capacitor C44. Verify that the voltage at TP12 is 0.000±0.010 Vdc.

Table 4. Buffer Amplifier No. 1 Power Levels

Test Point	Power Level (dBm)		Circuit Opened By
	Closed Circuit	Open Circuit*	
A5TP1	-4.00 to -10.00	+2.00 to -4.00	Remove jumper to A4
A5TP2	+6.45 to +0.45	+8.00 to +2.00	Remove jumper to A6
A5TP3	+4.45 to -1.55	+7.15 to +1.15	Remove jumper to A4
A5TP5	+3.65 to -2.35	+4.50 to -1.50	Unsolder base of Q2

*To make the open circuit measurements, disconnect the white/black/orange wire. Ground the TUNE input to the Voltage Controlled Oscillator on A5.

Table 5. Buffer Amplifier No. 2 Power Levels

Test Point	Power Level (dBm)		Circuit Opened By
	Closed Circuit	Open Circuit*	
A4TP2	-5.0 to -11.0	-2.0	remove R6 and R7
A4TP3	-1.5 to -9.5		
A4TP4	+5.5 to -0.5		

*To make the open circuit measurements, disconnect the white/black/orange wire. Ground the TUNE input to the Voltage Controlled Oscillator on A5.

SERVICE SHEET 1 (Cont'd)

Table 6. IF Input Filter Power Levels

Test Point	Power Level (dBm)		Circuit Opened By
	Closed Circuit	Open Circuit*	
A4TP5	−15.5 to −19.5	−11.5 to −15.5	Disconnect C30, L19
A4TP6	−18.0 to −22.0	−14.0 to −18.0	Disconnect C47, L30

*To make the open circuit measurements, disconnect the white/black/orange wire. Ground the TUNE input to the Voltage Controlled Oscillator on A5.

Table 7. IF Buffer Amplifiers Biasing

Signal Generator Frequency	Bias Q3 (Vdc)			Bias Q4 (Vdc)			Bias Q5 (Vdc)		
	E	B	C	E	B	C	E	B	C
500 MHz	+0.14	+0.89	+4.82	+10.47	+9.79	+2.27	0.00	+0.74	grd
700 MHz	0.00	0.00	+14.06	+14.06	+14.06	0.00	0.00	0.00	grd

Table 8. IF Filter Select Voltages

Signal Generator Frequency (MHz)	IF Filter Select Voltage* (Vdc) at IF SEL Inputs					Frequency at TP8 (MHz)
	250	200	150	100	50	
500	14.0	0.9	14.0	14.0	14.0	200
550	14.0	14.0	0.9	14.0	14.0	150
600	14.0	14.0	14.0	0.9	14.0	100
650	14.0	14.0	14.0	14.0	0.9	50
940	0.9	14.0	14.0	14.0	14.0	250
700	14.0	14.0	14.0	14.0	14.0	DC

*IF Filter 'not selected' when voltage is 0.9 Vdc.

Table 9. Pulse Generator and Sampling Bridge Power Levels

Test Point	Power Level (dBm)		Circuit Opened By
	Closed Circuit	Open Circuit*	
A4TP8	−9.0 to −13.0		
A4TP9	+11.8 to +7.8	+15.0 to +11.0	Disconnect R1, R2

*To make the open circuit measurements, disconnect and ground the TUNE voltage input to the A5 Voltage Controlled Oscillator.

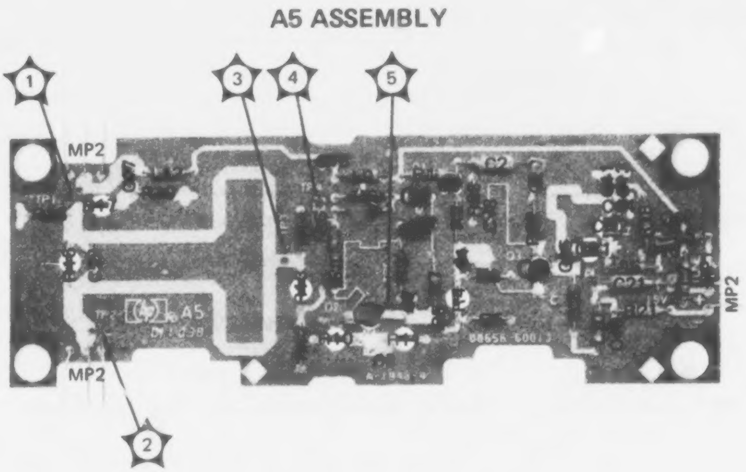

A5 ASSEMBLY
1
3
4
5
MP2
MP2
MP2
2

Figure 8-37. High Frequency Oscillator Component Locations

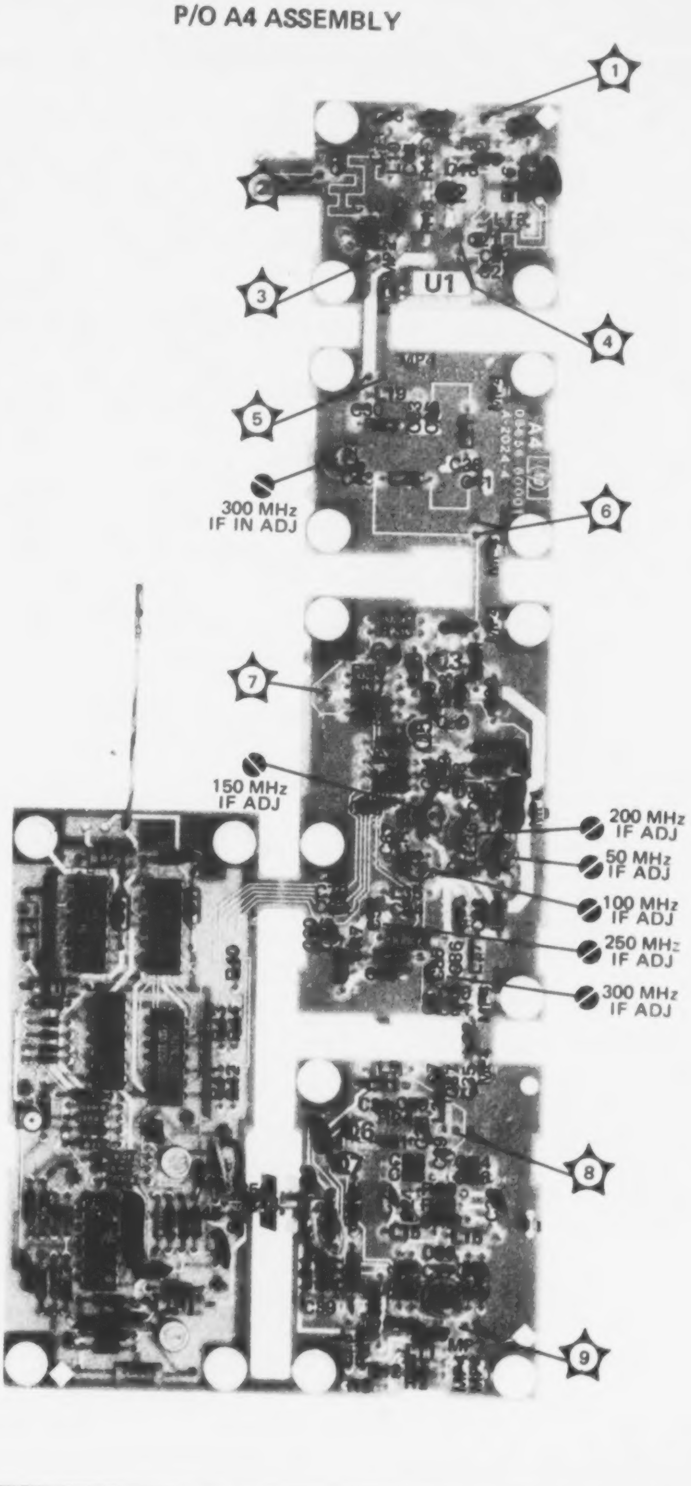

P/O A4 ASSEMBLY
1
2
3
U1
4
5
6
300 MHz IF IN ADJ
7
150 MHz IF ADJ
200 MHz IF ADJ
50 MHz IF ADJ
100 MHz IF ADJ
250 MHz IF ADJ
300 MHz IF ADJ
8
9

Figure 8-38. IF Section (A4 Assembly) Component Locations

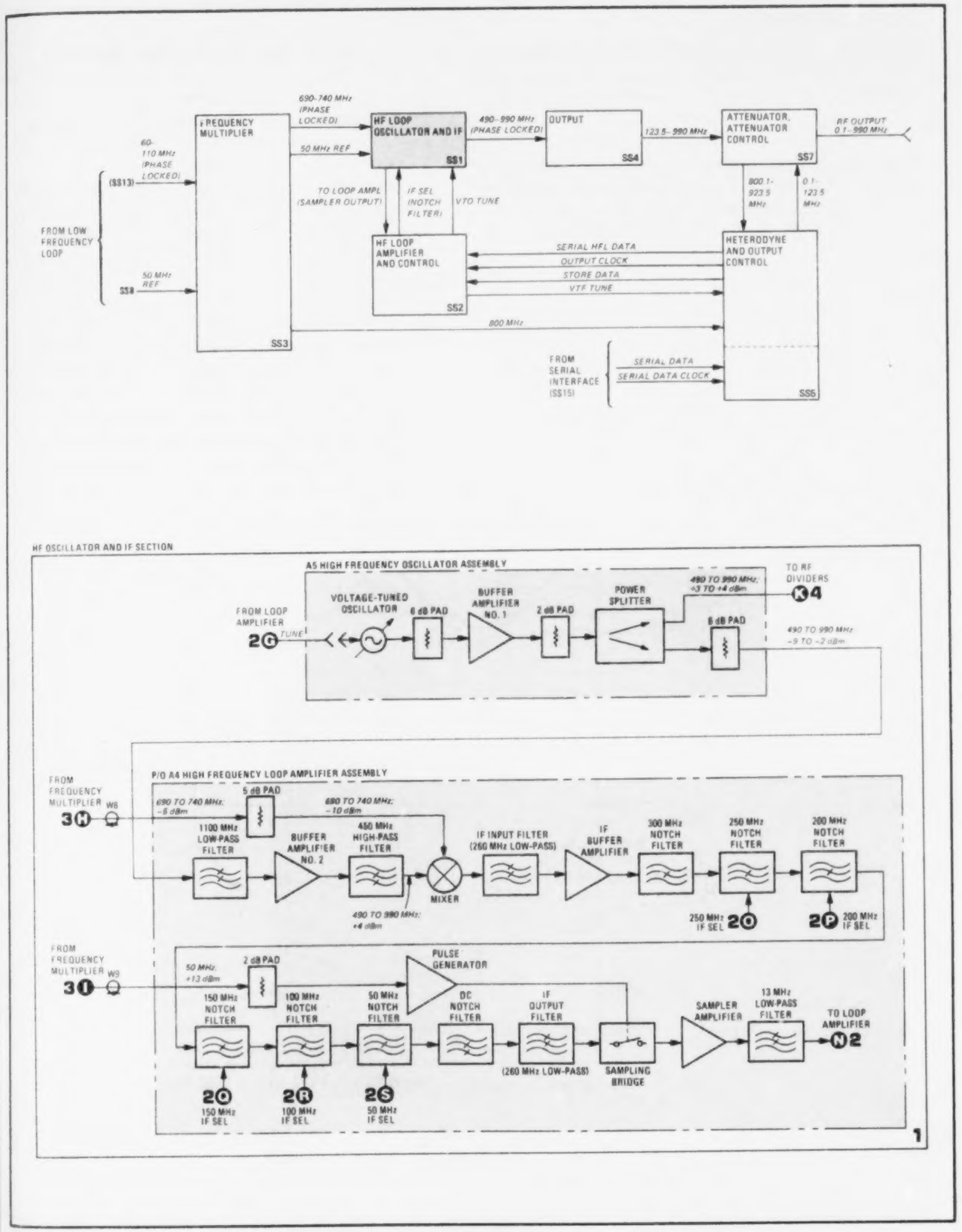
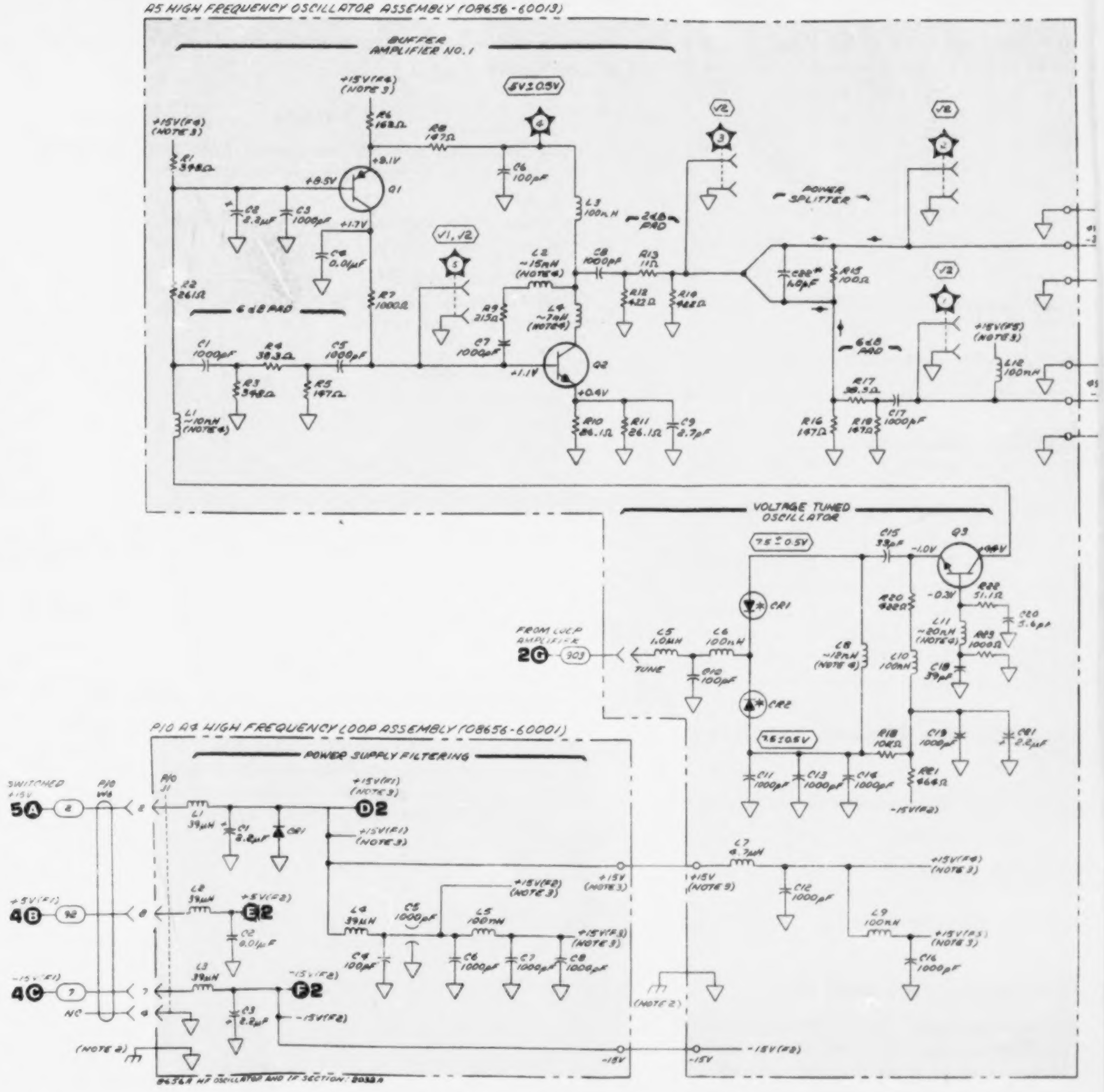
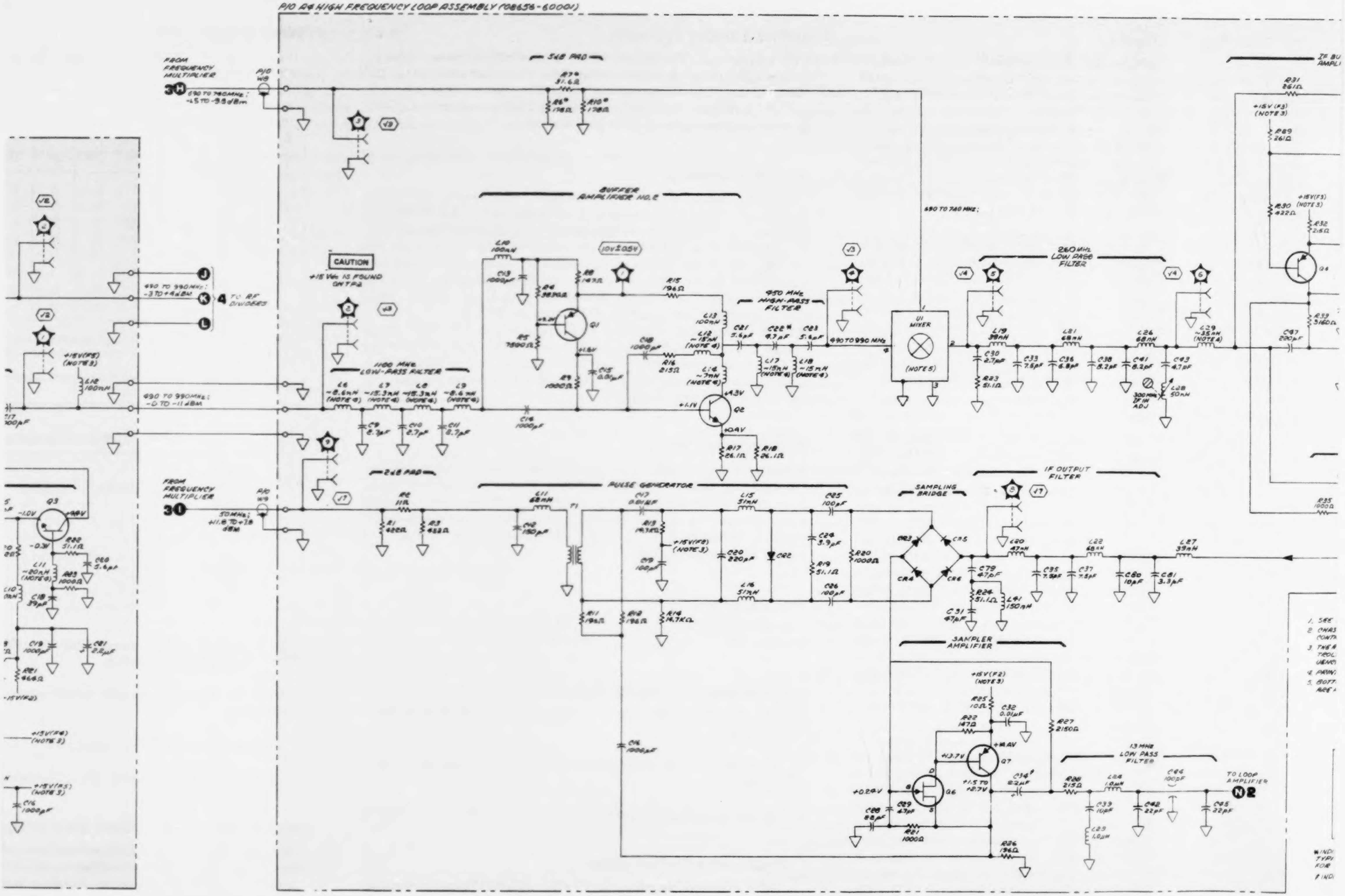
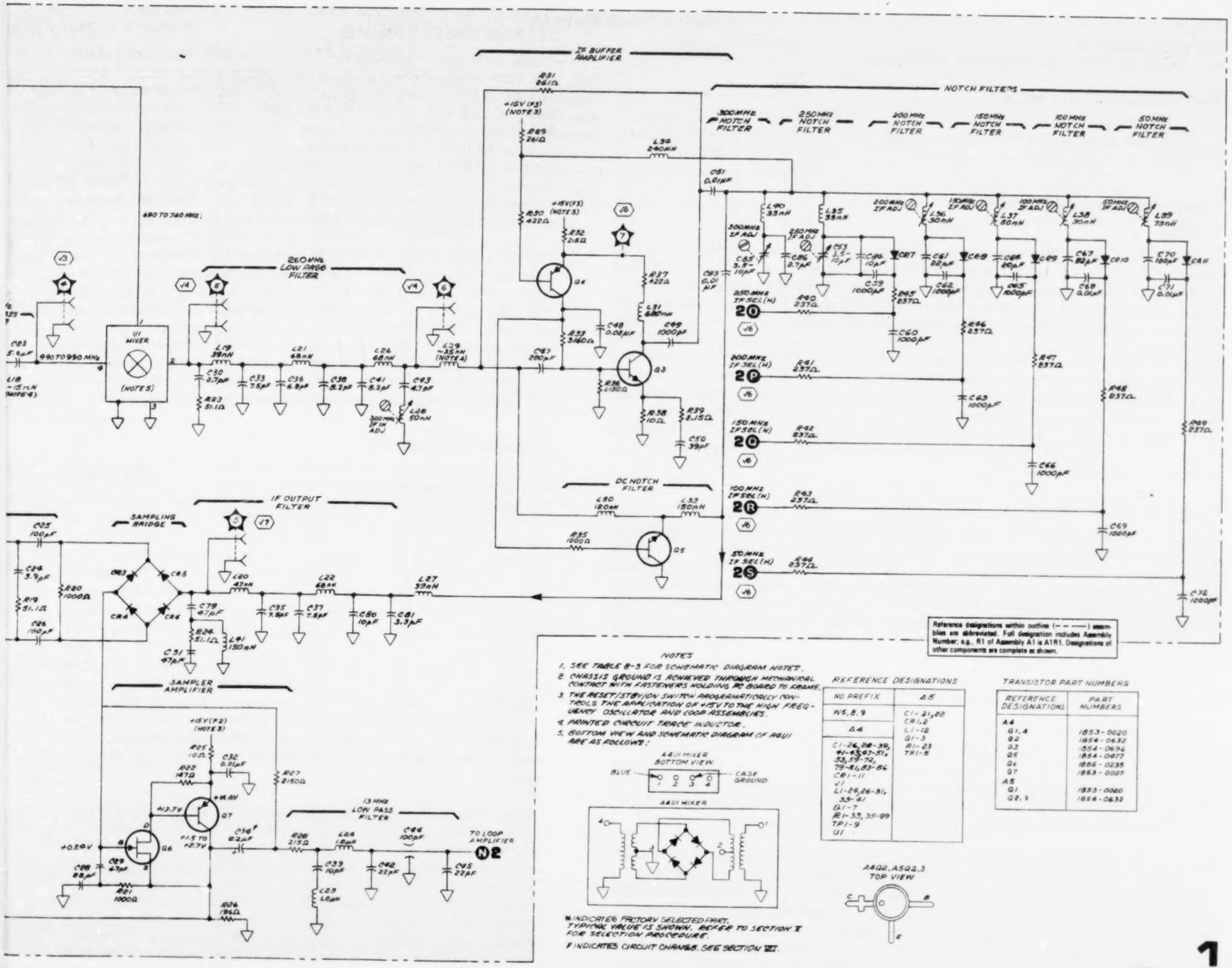

FREQUENCY MULTIPLIER
SS3
60-110 MHz (PHASE LOCKED)
(SS13)
FROM LOW FREQUENCY LOOP
50 MHz REF
SS8
690-740 MHz (PHASE LOCKED)
50 MHz REF
HF LOOP OSCILLATOR AND IF
SS1
490-990 MHz (PHASE LOCKED)
OUTPUT
SS4
123.5-990 MHz
ATTENUATOR, ATTENUATOR CONTROL
SS7
RF OUTPUT 0.1-990 MHz
TO LOOP AMPL (SAMPLER OUTPUT)
IF SEL (NOTCH FILTER)
VTO TUNE
800.1-923.5 MHz
0.1-123.5 MHz
HF LOOP AMPLIFIER AND CONTROL
SS2
SERIAL HFL DATA
OUTPUT CLOCK
STORE DATA
VTF TUNE
HETERODYNE AND OUTPUT CONTROL
SS6
800 MHz
FROM SERIAL INTERFACE (SS15)
SERIAL DATA
SERIAL DATA CLOCK
HF OSCILLATOR AND IF SECTION
A5 HIGH FREQUENCY OSCILLATOR ASSEMBLY
FROM LOOP AMPLIFIER
2G
TUNE
VOLTAGE-TUNED OSCILLATOR
6 dB PAD
BUFFER AMPLIFIER NO. 1
2 dB PAD
POWER SPLITTER
490 TO 990 MHz; +3 TO +4 dBm
TO RF DIVIDERS
K4
6 dB PAD
490 TO 990 MHz -9 TO -2 dBm
P/O A4 HIGH FREQUENCY LOOP AMPLIFIER ASSEMBLY
FROM FREQUENCY MULTIPLIER W8
3H
690 TO 740 MHz; -5 dBm
5 dB PAD
690 TO 740 MHz; -10 dBm
1100 MHz LOW-PASS FILTER
BUFFER AMPLIFIER NO. 2
450 MHz HIGH-PASS FILTER
MIXER
490 TO 990 MHz; +4 dBm
IF INPUT FILTER (260 MHz LOW-PASS)
IF BUFFER AMPLIFIER
300 MHz NOTCH FILTER
250 MHz NOTCH FILTER
200 MHz NOTCH FILTER
250 MHz IF SEL 2O
2P 200 MHz IF SEL
FROM FREQUENCY MULTIPLIER W9
3I
50 MHz; +13 dBm
2 dB PAD
PULSE GENERATOR
150 MHz NOTCH FILTER
100 MHz NOTCH FILTER
50 MHz NOTCH FILTER
DC NOTCH FILTER
IF OUTPUT FILTER (260 MHz LOW-PASS)
SAMPLING BRIDGE
SAMPLER AMPLIFIER
13 MHz LOW-PASS FILTER
TO LOOP AMPLIFIER
N2
2Q 150 MHz IF SEL
2R 100 MHz IF SEL
2S 50 MHz IF SEL
1

Figure 8-39. High Frequency Oscillator and IF Section Block Diagrams


A5 HIGH FREQUENCY OSCILLATOR ASSEMBLY (08656-60013)
BUFFER AMPLIFIER NO. 1
POWER SPLITTER
6 dB PAD
2 dB PAD
VOLTAGE TUNED OSCILLATOR
FROM LOOP AMPLIFIER
2G
TUNE
P/O A4 HIGH FREQUENCY LOOP ASSEMBLY (08656-60001)
POWER SUPPLY FILTERING
SWITCHED +15V
5A
4B
4C
D2
E2
F2
NC
(NOTE 2)
8656A HF OSCILLATOR AND IF SECTION: 2033A


A10 A4 HIGH FREQUENCY LOOP ASSEMBLY (08656-60001)
FROM FREQUENCY MULTIPLIER
3H
690 TO 740MHz; -4.5 TO -9.5dBm
A10 W8
5dB PAD
R7* 31.6Ω
R6* 178Ω
R10* 178Ω
BUFFER AMPLIFIER NO. 2
CAUTION
+15 Vdc IS FOUND ON TP2
10V±0.5V
L10 100nH
C13 1000pF
R4 3830Ω
R8 147Ω
R5 7500Ω
R9 1000Ω
C15 0.01μF
Q1
R15 196Ω
C18 1000pF
R16 215Ω
L13 100nH
L12 ~15nH (NOTE 4)
L14 ~7nH (NOTE 4)
Q2
+4.3V
+1.1V
+0.4V
R17 26.1Ω
R18 26.1Ω
950 MHz HIGH-PASS FILTER
C21 5.6pF
C22* 4.7pF
C23 5.6pF
L17 ~15nH (NOTE 4)
L18 ~15nH (NOTE 4)
490 TO 990 MHz
690 TO 740 MHz;
U1 MIXER
(NOTE 5)
260 MHz LOW PASS FILTER
L19 39nH
L21 68nH
L26 68nH
L29 ~35nH (NOTE 4)
C30 2.7pF
R23 51.1Ω
C33 7.5pF
C36 6.8pF
C38 8.2pF
C41 8.2pF
C43 4.7pF
L28 50nH
300 MHz IF IN ADJ
C87 220pF
IF BU... AMPL...
R31 261Ω
+15V (F3) (NOTE 3)
R89 261Ω
R30 422Ω
R32 215Ω
Q4
R33 3160Ω
R35 1000Ω
490 TO 990MHz; -3 TO +4dBM
J
K
L
4 TO RF DIVIDERS
+15V(F5) (NOTE 3)
L12 100nH
490 TO 990MHz; -0 TO -11dBM
C17 1000pF
1100 MHz LOW-PASS FILTER
L6 ~8.6nH (NOTE 4)
L7 ~15.3nH (NOTE 4)
L8 ~15.3nH (NOTE 4)
L9 ~8.6nH (NOTE 4)
C9 8.7pF
C10 2.7pF
C11 8.7pF
C16 1000pF
FROM FREQUENCY MULTIPLIER
3O
50MHz; +11.8 TO +7.8 dBM
2dB PAD
R2 11Ω
R1 422Ω
R3 422Ω
PULSE GENERATOR
L11 68nH
T1
C12 150pF
C17 0.01μF
R13 14.7KΩ
+15V(F8) (NOTE 3)
C19 100pF
C20 220pF
L15 51nH
L16 51nH
CR2
C24 3.9pF
R19 51.1Ω
C25 100pF
C26 100pF
R20 1000Ω
R11 196Ω
R12 196Ω
R14 14.7KΩ
C16 1000pF
SAMPLING BRIDGE
CR3
CR5
CR4
CR6
IF OUTPUT FILTER
C79 47pF
R24 51.1Ω
L41 150nH
C31 47pF
L20 47nH
L22 68nH
L27 39nH
C35 7.5pF
C37 7.5pF
C80 10pF
C81 3.3pF
SAMPLER AMPLIFIER
+15V(F2) (NOTE 3)
R25 10Ω
C32 0.01μF
R22 147Ω
R27 2150Ω
+14.4V
+13.7V
Q7
+1.5 TO +2.7V
+0.24V
Q6
C28 82pF
C29 47pF
R21 1000Ω
R26 196Ω
C34† 2.2μF
13 MHz LOW PASS FILTER
R28 215Ω
L24 1.0μH
C44 100pF
C39 10pF
L23 1.0μH
C42 22pF
C45 22pF
TO LOOP AMPLIFIER
N2
Q3
-1.0V
-0.3V
+9.8V
R22 51.1Ω
L11 ~20nH (NOTE 4)
R23 1000Ω
C20 5.6pF
C18 39pF
C19 1000pF
C21 2.2μF
R21 464Ω
-15V(F2)
+15V(F4) (NOTE 3)
+15V(F5) (NOTE 3)
C16 1000pF
1. SEE
2. CHAS CONT
3. THE TROL UENO
4. PARN
5. BOTT ARE
WIND TYPI FOR
† IND


IF BUFFER AMPLIFIER
NOTCH FILTERS
300MHz NOTCH FILTER
250MHz NOTCH FILTER
200MHz NOTCH FILTER
150MHz NOTCH FILTER
100MHz NOTCH FILTER
50MHz NOTCH FILTER
250MHz LOW PASS FILTER
U1 MIXER (NOTE 5)
690 TO 990 MHz
DC NOTCH FILTER
SAMPLING BRIDGE
IF OUTPUT FILTER
SAMPLER AMPLIFIER
13 MHz LOW PASS FILTER
TO LOOP AMPLIFIER
N2
+15V (F3) (NOTE 3)
+15V (F2) (NOTE 3)
350 MHz IF SEL (H)
2Q
200 MHz IF SEL (H)
2P
150 MHz IF SEL (H)
2Q
100 MHz IF SEL (H)
2R
50 MHz IF SEL (H)
2S
Q1
Q3
Q4
Q5
Q6
Q7
A4U1 MIXER BOTTOM VIEW
BLUE
CASE GROUND
1 2 3 4
A4U1 MIXER
A4Q2, A5Q2,3 TOP VIEW
C
B
E

Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. THE RESET/STBY/ON SWITCH PROGRAMATICALLY CONTROLS THE APPLICATION OF +15V TO THE HIGH FREQUENCY OSCILLATOR AND LOOP ASSEMBLIES.
4. PRINTED CIRCUIT TRACE INDUCTOR.
5. BOTTOM VIEW AND SCHEMATIC DIAGRAM OF A4U1 ARE AS FOLLOWS:

* INDICATES FACTORY SELECTED PART. TYPICAL VALUE IS SHOWN. REFER TO SECTION V FOR SELECTION PROCEDURE.

‡ INDICATES CIRCUIT CHANGE. SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A5
W6,8,9	C1-21,22 CR1,2 L1-12 Q1-3 R1-23 TP1-5
A4	
C1-26,28-39, 41-45,47-51, 53,59-72, 79-81,83-86 CR1-11 J1 L1-24,26-31, 33-41 Q1-7 R1-33, 35-49 TP1-9 U1	

TRANSISTOR PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
A4	
Q1,4	1853-0020
Q2	1854-0632
Q3	1854-0696
Q5	1854-0477
Q6	1856-0235
Q7	1853-0007
A5	
Q1	1853-0020
Q2,3	1854-0632

1

P/O A4 A5

Figure 8-40. High Frequency Oscillator and IF Section Schematic Diagram

SERVICE SHEET 2
P/O A4 HIGH FREQUENCY LOOP ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD2
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The Loop Amplifier, U5A, functions as an integrator within the loop bandwidth (less than 50 kHz). U5B is a comparator. When the search mode is entered, the input from the sampler (positive input to U5A) begins to change. The comparator input U5B-pin 3 follows the output of U5A. When the reference level (-3.75 Vdc) is reached, the comparator output switches to the opposite polarity which places a voltage differential across C73. C73 begins to discharge and the voltage again approaches the comparator's reference level. This continued action of the comparator and integrator produces a linear triangle waveform. It is used to sweep the voltage controlled oscillator across its frequency range while searching for the loop lock point. When phase lock occurs, the input voltage from the sampler becomes a dc level. The input to the comparator no longer changes, the switching action of U5B stops, and the sweeping output of U5A (the VCO's tune voltage) stops. The VCO output frequency is now essentially fixed and phase locked.

Loop and Search Amplifiers

The Loop Amplifier U5A is a non-inverting unity gain amplifier for frequencies greater than 50 kHz and an integrator for frequencies less than 50 kHz. The phase lock loop does not require additional gain above 50 kHz for phase lock operation. The input signal level from the sampler is at a higher level than necessary for the Voltage Controlled Oscillator's sensitivity. Resistor R72 and capacitor C78 reduce this level by 6 dB. Since the Loop Amplifier does not have any dc feedback the dc gain is open loop. AC feedback is by capacitor C73. The higher frequencies are coupled directly to the VCO tune bus through capacitor C77. The VCO Tune bus applies the TUNE voltage to the Voltage Controlled Oscillator across R70, R71 and R54 and to the positive input of Search Amplifier U5B through resistor R69.

Search Amplifier U5B functions as a comparator. The negative input of U5B is fixed at approximately -3.75 Vdc by resistor R73 and R74. The voltage at pin 1 will be near either -14 Vdc or +14 Vdc. This change in voltage of U5B will be integrated by U5A to generate both a negative and positive "ramp" VCO Tune Voltage to sweep the Voltage Controlled Oscillator. Therefore, U5A and U5B form a triangle wave generator with an output from U5A that will sweep from approximately -7.5V to +12V.

Refer to the waveforms in Figure 1. The loop is unlocked and the positive input to U5B is more positive than -3.75 Vdc. The output of U5B is switched to +12 Vdc. The VCO is swept across its frequency range (990 to 494 MHz). At time T1 the comparator U5B has just changed state. CR16 is biased on and CR17 is biased off. At time T2 the positive input to U5B becomes more negative then the negative input and the output switches to -14V, CR16 is biased off, CR17 is on and the positive input to U5B is pulled to -8.7V. During this time the instrument would normally have locked. At time T3 the positive input to U5B becomes more positive than the negative input and the output changes to +14V, CR16 is biased on, CR17 is biased off and the positive input of U5B is pulled to +6 volts. This cycle is repeated until a locked voltage is received from the sampler.

SERVICE SHEET 2 (Cont'd)

Under normal circumstances, the maximum lock time is one ramp or 1.5 ms. When the lock point is reached the output voltage of the Sampling Bridge and Sampling Amplifier will be a dc voltage to lock the loop and fix the VCO frequency. The Loop and Search Amplifiers stop functioning as a triangle wave generator. The voltage on the VCO bus is fixed except for small changes. The positive input to U5B is fixed and the output will stay at -14 or +14 Vdc and the negative input to U5B has an offset voltage of 20 mVdc from the current flow through R62, R59, R58, and R55. The offset voltage prevents the loop from locking at invalid lock points.

The SEARCH SELECT logic control from the Microprocessor is connected to the negative input of U5B. This reference input sets the output of Search Amplifier to either +14 or -14 volts. Thus the Loop Amplifier integrator "ramp" will be in the right direction for phase lock in the minimum time (1.5 ms maximum). For example, the VCO frequency is 500 MHz and is changed to 600 MHz. The sweep should go up in frequency from 500 MHz to 600 MHz. The logic level of SEARCH SEL will be high which sets the output of U5B to -14 volts and causes the tune voltage to sweep the VCO up in frequency.

Sideband Comparators

Sideband comparator U5D and exclusive-OR gates U6 determine if the instrument will lock at a frequency above or below 715 MHz. The 715 MHz adjustment sets the reference voltage equal to the positive input of U5D with the instrument set to 715 MHz. Lets look at an example where an input frequency of 900 MHz is selected. The Low Frequency Loop oscillator is tuned to 100 MHz. The 200 MHz Notch Filter is 'not selected'. This action passes only the 200 MHz IF sideband. All the other sidebands are 'selected' which effectively filters them out. The input frequency to the mixer A4U1 (refer to Service Sheet 1) will be 700 MHz. The VCO frequency is being swept since the loop is not locked. At the previous frequency, the VCO was tuned to 494 MHz. As the VCO sweeps through 500 MHz, the IF is 200 MHz and the loop wants to lock. SIDEBAND C SEL is set to logic level one, which passes the sideband above 715 MHz. This prevents the loop from locking below 715 MHz. As the VCO sweeps up to 900 MHz, the 700 MHz input is subtracted from the VCO frequency to yield the 200 MHz intermediate frequency and the loop locks.

Under the preceding conditions, both inputs to Nor gate U6D will be high so the output is low. Both inputs to U6A will be low so the output is low. Both inputs to U6B will then be low (output of U6A and U6D) so the output will be low. CR18 will be on and TP16 is approximately +0.6 Volts so CR19 will be off. The VCO sweep voltage will be in a positive direction so the negative input to sideband comparator U5D is also swept in the positive direction. The 715 MHz adjustment is adjusted so at 715 MHz both inputs to U5D are equal. Therefore, with CR19 off, the positive input to U5D is fixed by divider R51, R52, R53 between +15 and -15 volts. So below 715 MHz the positive input will be more positive than negative input of U5D. Output of U5D will be approximately +12 volts and the corresponding input to nor gate U6C will be high. The output will be high which turns on Q10 and grounds the phase detector output. The VCO can not lock at 500 MHz. As the VCO sweeps through 715 MHz, the output of comparator U5D switches, the output of Nor gate U6C goes low and Q10 is turned off allowing the loop to lock.

Gain Compensation

Frequency change of the VCO is not linear with respect to voltage. Transistors Q8 and Q9 are used to compensate for this non-linear relationship. The collector of Q9 is low (0 volts dc) when the 200 MHz IF Notch Filter is 'not selected'; the collector of Q8 is low when the 150 MHz IF Notch Filter is 'not selected'. Both the base-emitter junctions of Q8 and Q9 will be forward biased when the VCO frequency is below 715 MHz; the output of U5D will be +12 Vdc. Resistors R56 and R57 are a voltage divider for the dc bias voltage to the base of Q8 and Q9. When the VCO frequency is 500 MHz, Q9 is biased on and resistor R67 and C75 increase the attenuation of the VCO tune voltage. When the VCO frequency is 550 MHz, Q8 is biased on and resistor R68 and capacitor C76 increase the attenuation of the VCO tune voltage.

TROUBLESHOOTING

Procedures for checking part of the circuits of the A4 High Frequency Loop Assembly are given below. The area or points to check are marked on the schematic by a hexagon with a check mark and a number inside, e.g. √1. Fixed voltages are shown on the schematic inside a hexagon, e.g. 2V±0.2V. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Oscilloscope	HP 1222A

√1 HF Loop Data Storage/Drivers

1. Set the Signal Generator to -10 dBm at 100 kHz without modulation.

2. Enter frequencies in the order listed in Table 1 beginning with 500 MHz.

3. Check the voltages at the Outputs of U2, U3 and U4 as indicated.

√2 Exclusive-Or Gate A4U6

1. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

2. Check the voltages listed in Table 2.

SERVICE SHEET 2 (Cont'd)

Table 1. IF Filter Notch Filter Select*

Signal Generator Frequency (MHz)	Digital Level**							
	SEARCH SEL(H)	IF SEL(H) Notch Filters					SIDEBAND	
		250	200	150	100	50	C SEL	B SEL
500	L	H	L	H	H	H	L	H
550	H	H	H	L	H	H	L	H
600	H	H	H	H	L	H	L	H
650	H	H	H	H	H	L	L	H
700	H	H	H	H	H	H	L	L
900	H	H	L	H	H	H	H	L
950	H	L	H	H	H	H	H	L
800	L	H	H	H	L	H	H	L

*A notch filter that is selected "filters out" that IF sideband. Therefore, the required IF sideband filter is 'not selected' in order to pass the required frequency.

**Digital Levels are as follows: A4U4 H>+2 Vdc L<+0.5 Vdc, A4U2 H>+3.5 Vdc L<+1.5 Vdc and A4U3 H>+13 Vdc L<+0.5 Vdc.

Table 2. A4U6 Digital Voltage Levels

Signal Generator Frequency (MHz)	U6A-Pin			U6B-Pin			U6C-Pin			U6D-Pin		
	1	2	3	4	5	6	8	9	10	11	12	13
500	H	L	H	H	H	L	L	H	H	H	L	H
900	L	L	L	L	L	L	L	L	L	L	H	H
715	L	L	L	L	H	H	L	H	H	H	L	H

√3 Search Amplifier, Loop Amplifier, Sideband Comparator, and Sideband Switch

1. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

2. Disconnect the TUNE voltage to the VCO.

3. Verify that the waveforms of Figure 1 are correct.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

This is an alternate method of troubleshooting Service Sheet 2 circuits. Service Sheet BD4 and Service Sheet 5 (which both refer to this service sheet) are used primarily to troubleshoot from the digital (control) standpoint. Note that digital information from the Microprocessor and related circuits must pass through the circuits shown on Service Sheet 5 before they get to circuits on Service Sheet 2. Be sure that the Service Sheet 5 signatures are correct before trying to isolate an incorrect signature in these circuits. If the signatures on these circuits are correct, the problem may be in the controlled circuits. In this case continue with the troubleshooting information preceding this paragragh or refer to the troubleshooting information found on Service Sheet BD2.

Purpose. Verify correct data transfer from the Microprocessor to the High Frequency Loop.

NOTE

Signatures are not valid for Signal Generators with serial number prefixes 2009A through 2018A.

Setup. Connect the signature analyzer as follows:

1) GND to GND A11TP2
2) CLK to SA4 A11TP7
3) START to SA5 A11TP9
4) STOP to SA5 A11TP9.

Set the controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN.

Set up the Signal Generator as follows:

1) Set the LOGIC/RAM switch P/O A11S1 to LOGIC.
2) On the A6 Output Assembly board, short TP5 to TP4 (GND); short TP6 to TP4 (refer to Service Sheet 5).

Initialize. Briefly short A11TP3 NMI to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

◀ High Frequency Oscillator and IF
P/O A4, A5
SERVICE SHEET 1

SERVICE SHEET 2

Probe. Connect the probe to the node indicated in Table 3. Verify that each signature is correct and stable.

Disconnect the jumpers between the test points and between the test point and ground. Reset the LOGIC/RAM switch to RAM. Reset the Signal Generator with the front panel RESET-STBY-ON switch.

Table 3. High Frequency Loop Signatures

Node	Correct Signature	Comments
+5V	F84P	
* U4 #3	F84P	SIPO CLK
U4 #2	744F	HF DATA
U4#4 U2#2	HA4C	SRCH SEL
U4#5 U2#4	PH25	250 MHZ
U4#6 U2#6	U692	200 MHZ
U4#7 U2#10	UC49	150 MHZ
U4#14 U2#15	UHA4	100 MHZ
U4#13 U2#12	7PH2	50 MHZ
U4 #11	13C0	SIDEBAND B
U4 #12	CU69	SIDEBAND C

*This signature is the same as the +5V signature; the probe should blink.

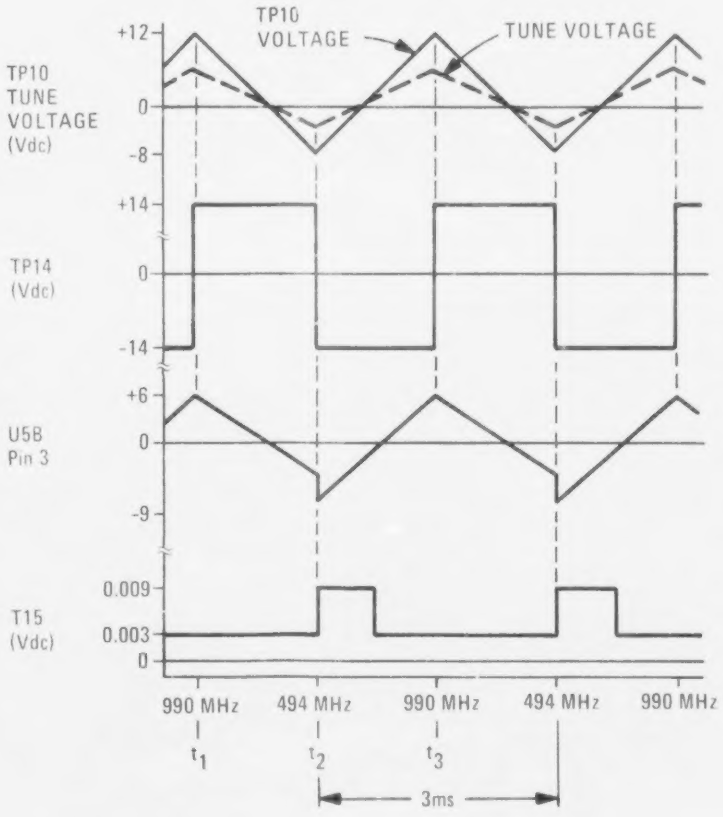


Figure 1. Unlocked High Frequency Loop Waveforms

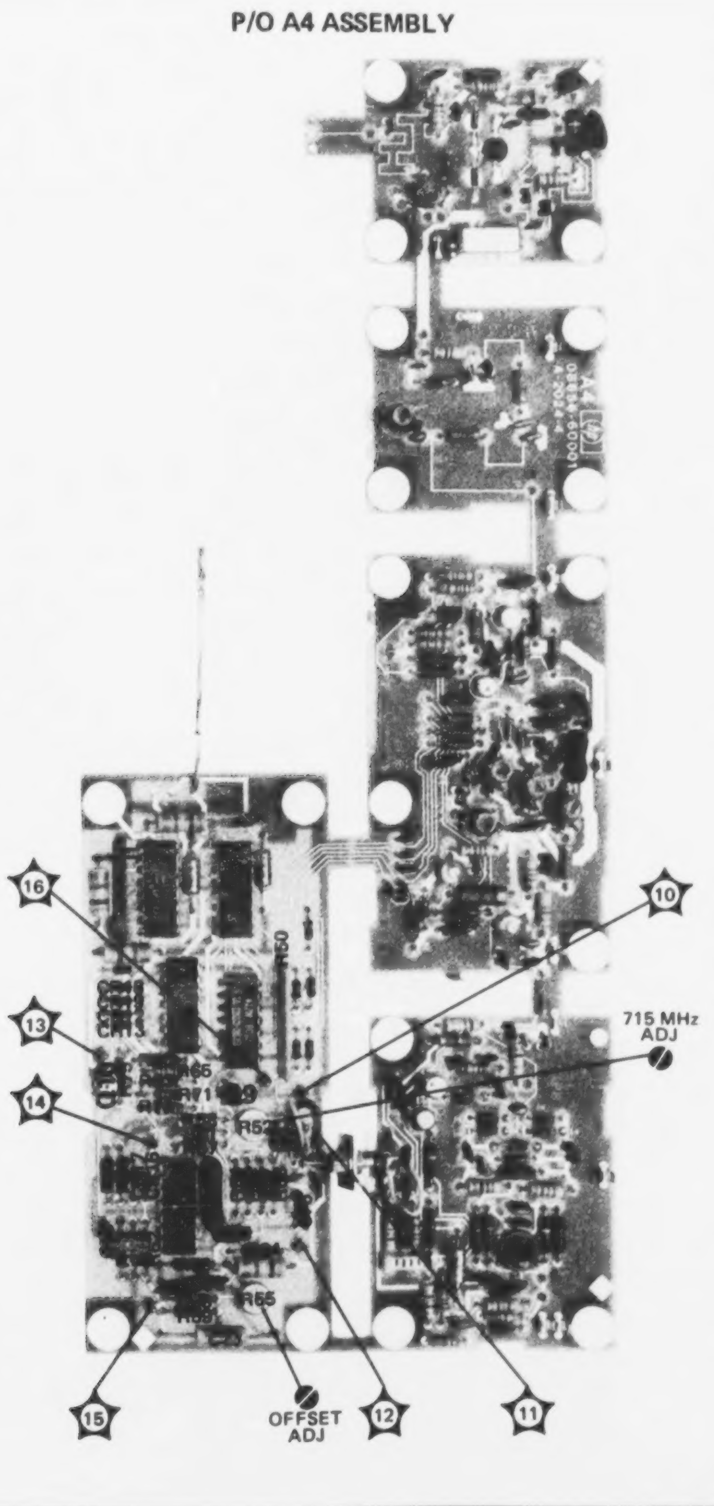
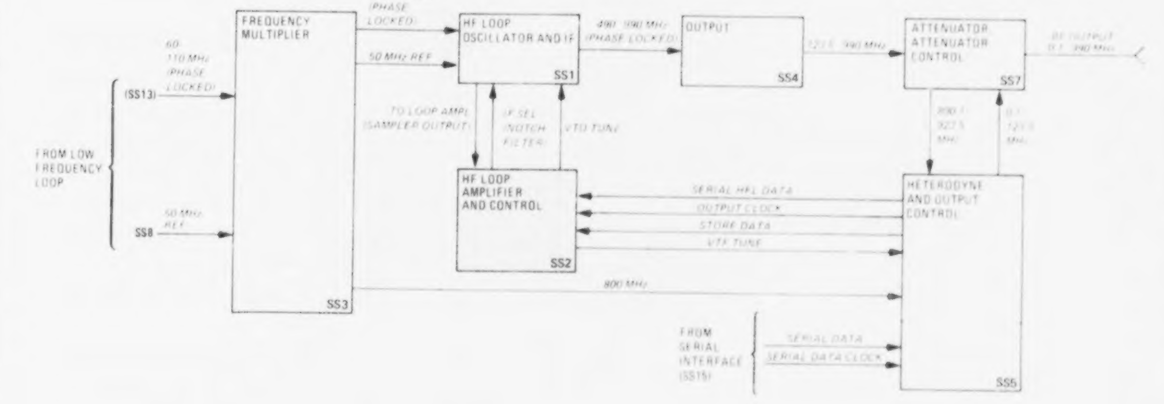

P/O A4 ASSEMBLY
16
13
14
10
715 MHz ADJ
R65
R71
R52
R50
R55
15
OFFSET ADJ
12
11

Figure 8-41. High Frequency Loop Amplifier and Control Component Locations


FREQUENCY MULTIPLIER
SS3
60-110 MHz (PHASE LOCKED)
(SS13)
FROM LOW FREQUENCY LOOP
50 MHz REF
SS8
690-740 MHz (PHASE LOCKED)
50 MHz REF
HF LOOP OSCILLATOR AND IF
SS1
TO LOOP AMPL (SAMPLER OUTPUT)
IF SEL (NOTCH FILTER)
VTO TUNE
HF LOOP AMPLIFIER AND CONTROL
SS2
490-990 MHz (PHASE LOCKED)
OUTPUT
SS4
123.5-990 MHz
ATTENUATOR ATTENUATOR CONTROL
SS7
RF OUTPUT 0.1-990 MHz
800.1-923.5 MHz
0.1-123.5 MHz
HETERODYNE AND OUTPUT CONTROL
SS5
SERIAL HFL DATA
OUTPUT CLOCK
STORE DATA
VTF TUNE
800 MHz
FROM SERIAL INTERFACE (SS15)
SERIAL DATA
SERIAL DATA CLOCK

HF LOOP AMPLIFIER AND CONTROL

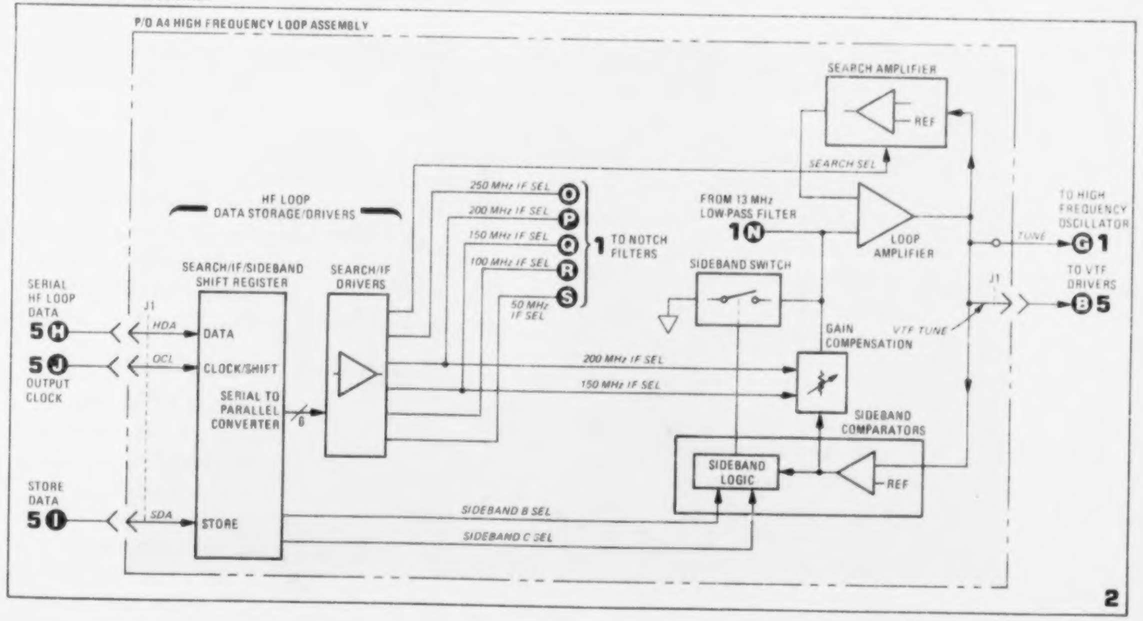
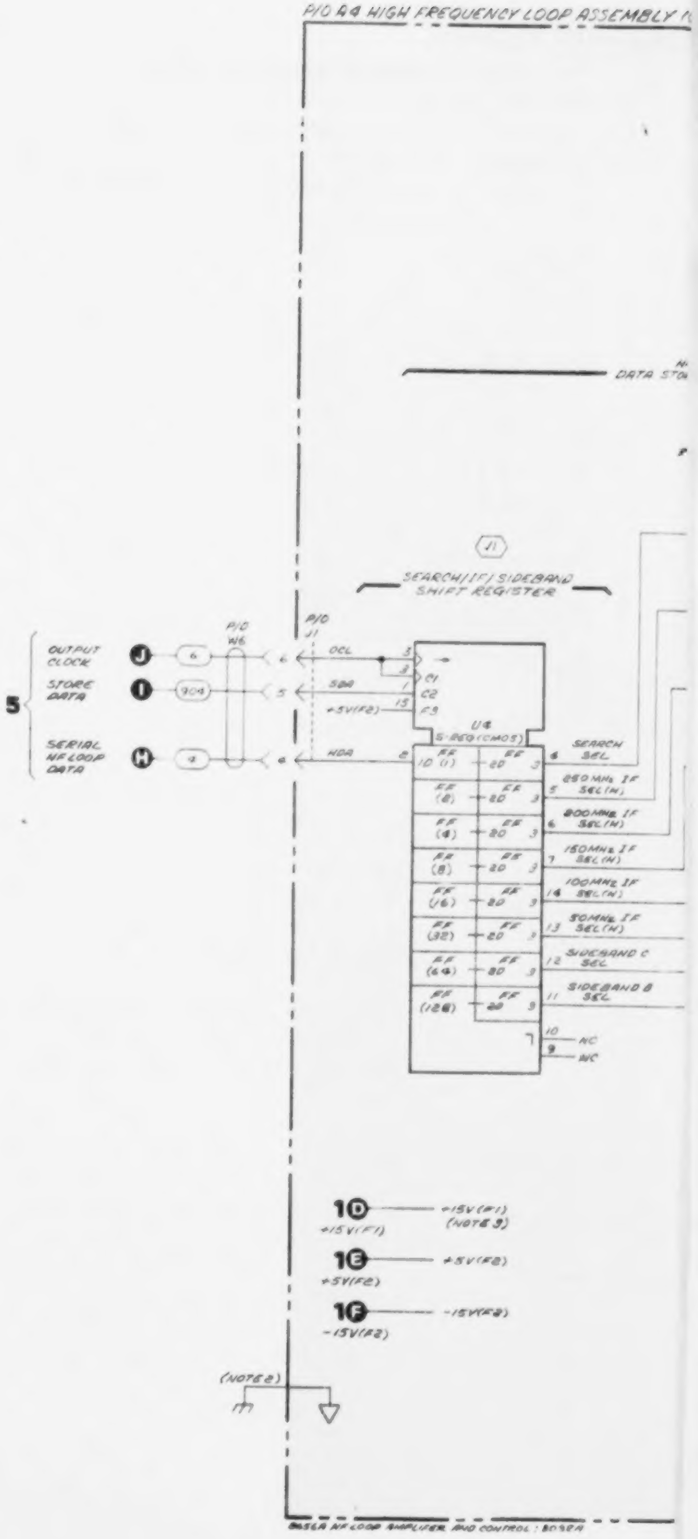
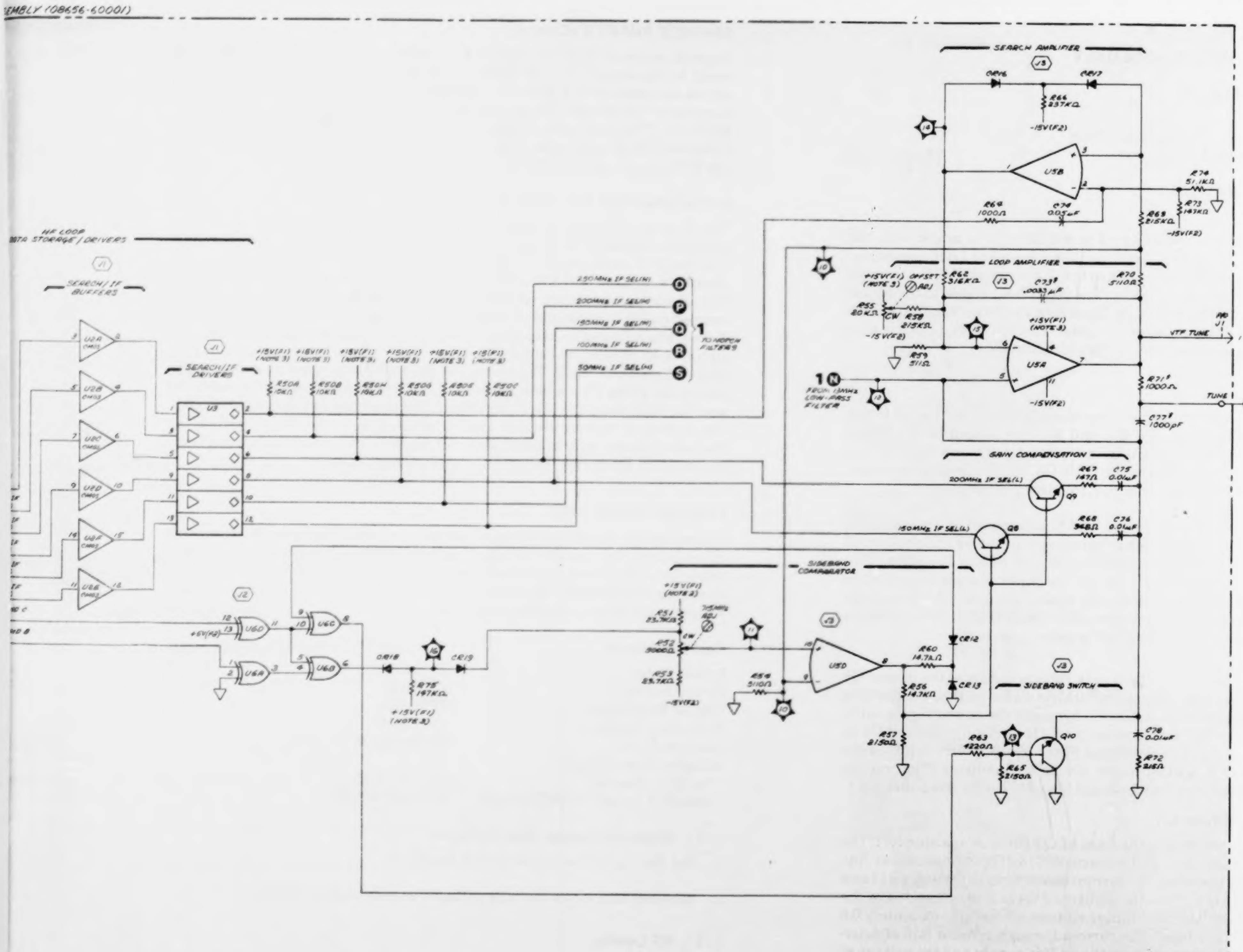

P/O A4 HIGH FREQUENCY LOOP ASSEMBLY
SERIAL HF LOOP DATA
5 H
5 J
OUTPUT CLOCK
STORE DATA
5 I
J1
HDA
OCL
SDA
HF LOOP DATA STORAGE/DRIVERS
SEARCH/IF/SIDEBAND SHIFT REGISTER
DATA
CLOCK/SHIFT
SERIAL TO PARALLEL CONVERTER
6
STORE
SEARCH/IF DRIVERS
250 MHz IF SEL
200 MHz IF SEL
150 MHz IF SEL
100 MHz IF SEL
50 MHz IF SEL
O
P
Q
R
S
1 TO NOTCH FILTERS
SEARCH AMPLIFIER
REF
SEARCH SEL
FROM 13 MHz LOW-PASS FILTER
1 N
LOOP AMPLIFIER
SIDEBAND SWITCH
GAIN COMPENSATION
200 MHz IF SEL
150 MHz IF SEL
SIDEBAND COMPARATORS
SIDEBAND LOGIC
REF
SIDEBAND B SEL
SIDEBAND C SEL
TO HIGH FREQUENCY OSCILLATOR
TUNE
G 1
J1
TO VTF DRIVERS
VTF TUNE
B 5
2

Figure 8-42. High Frequency Loop Amplifier and Control Block Diagrams


P/O A4 HIGH FREQUENCY LOOP ASSEMBLY (
DATA STO
J1
SEARCH/IF/SIDEBAND SHIFT REGISTER
5
OUTPUT CLOCK
STORE DATA
SERIAL HF LOOP DATA
J
I
H
6
904
4
P/O W6
P/O J1
OCL
SDA
+5V(F2)
HDA
U4
S-REG (CMOS)
C1
C2
F3
FF (1)
FF (2)
FF (4)
FF (8)
FF (16)
FF (32)
FF (64)
FF (128)
2D
SEARCH SEL
250MHz IF SEL(H)
200MHz IF SEL(H)
150MHz IF SEL(H)
100MHz IF SEL(H)
50MHz IF SEL(H)
SIDEBAND C SEL
SIDEBAND B SEL
NC
NC
1D
+15V(F1)
+15V(F1) (NOTE 3)
1E
+5V(F2)
+5V(F2)
1F
-15V(F2)
-15V(F2)
(NOTE 2)
8656A HF LOOP AMPLIFIER AND CONTROL : 8032A


EMBLY (08656-60001)
HF LOOP
DATA STORAGE / DRIVERS
J1
SEARCH/IF BUFFERS
U2A CMOS
U2B CMOS
U2C CMOS
U2D CMOS
U2F CMOS
U2E CMOS
J1
SEARCH/IF DRIVERS
U3
+15V(F1) (NOTE 3)
R50A 10KΩ
R50B 10KΩ
R50H 10KΩ
R50G 10KΩ
R50E 10KΩ
R50C 10KΩ
250MHz IF SEL(H)
200MHz IF SEL(H)
150MHz IF SEL(H)
100MHz IF SEL(H)
50MHz IF SEL(H)
O
P
Q
R
S
1
TO NOTCH FILTERS
J2
U6D
U6C
U6A
U6B
+5V(F2)
CR18
CR19
R75 197KΩ
+15V(F1) (NOTE 3)
SEARCH AMPLIFIER
J3
CR16
CR17
R66 237KΩ
-15V(F2)
U5B
R74 51.1KΩ
R73 147KΩ
R64 1000Ω
C74 0.05μF
R69 215KΩ
-15V(F2)
LOOP AMPLIFIER
J3
+15V(F1) (NOTE 3)
OFFSET ADJ
R62 316KΩ
C73 .0033μF
R70 5110Ω
R55 20KΩ
CW
R58 215KΩ
-15V(F2)
+15V(F1) (NOTE 3)
R59 511Ω
U5A
-15V(F2)
1 N
FROM 13MHz LOW-PASS FILTER
R71 1000Ω
C77 1000pF
VTF TUNE
A10 J1
A10 W6
906
B5
TO VTF DRIVERS
TUNE
903
G1
TO HIGH FREQUENCY OSCILLATOR
GAIN COMPENSATION
200MHz IF SEL(L)
R67 147Ω
C75 0.01μF
Q9
150MHz IF SEL(L)
R68 348Ω
C76 0.01μF
Q8
SIDEBAND COMPARATOR
+15V(F1) (NOTE 2)
R51 23.7KΩ
7.5MHz ADJ
CW
R52 5000Ω
R53 23.7KΩ
-15V(F2)
J3
U5D
R54 5110Ω
R60 14.7KΩ
CR12
CR13
R56 14.7KΩ
R57 2150Ω
SIDEBAND SWITCH
J3
R63 4220Ω
R65 2150Ω
Q10
C78 0.01μF
R72 316Ω
10
11
12
13
14
15
16

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. THE RESET/STBY/ON SWITCH PROGRAMATICALLY CONTROLS THE APPLICATION OF +15V TO THE HIGH FREQUENCY OSCILLATOR AND LOOP ASSEMBLIES.

* INDICATES CIRCUIT CHANGE - SEE SECTION VII.

NO PREFIX	A4 CONT.
W6	CR12,13,16,19 J1 Q8-10 R50-60,62-75 TP10-16 U2-6
A4	
C73-78	

LOGIC LEVELS

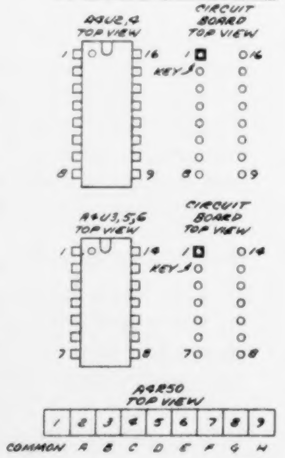
	TTL	CMOS
HIGH	>2V	>3.5V
LOW	<0.8V	<1.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	UNDEF
GROUND	LOW	LOW

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q8,9	1854-0071
Q10	1854-0477
U2	1820-1976
U3	1820-0618
U4	1820-1662
U5	1826-0323
U6	1820-1211

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2	+5V(F2) -1 ▽ -8
U3,6	+5V(F2) -14 ▽ -7
U4	+5V(F2) -16 ▽ -8


A4U2,4
TOP VIEW
1
16
8
9
CIRCUIT BOARD TOP VIEW
KEY
A4U3,5,6
TOP VIEW
1
14
7
8
CIRCUIT BOARD TOP VIEW
KEY
A4R50
TOP VIEW
1 2 3 4 5 6 7 8 9
COMMON A B C D E F G H

2
P/OA4

Figure 8-43. High Frequency Loop Amplifier and Control Schematic Diagram

SERVICE SHEET 3
A8 FREQUENCY MULTIPLIER ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD2
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The 50 MHz reference is multiplied by 16 to 800 MHz. It is mixed with the phase locked 60 to 110 MHz signal from the Low Frequency Loop Assembly. The Mixer's output is amplified and applied to a Bandpass Filter that passes the difference frequency 690 to 740 MHz. The input frequencies to the Mixer are phase locked to the 50 MHz reference. Therefore, the Mixer's output serves as a reference to lock the High Frequency Loop. The 800 MHz output is also applied to the Output Assembly (refer to Service Sheet 5).

Frequency Multiplier

The 50 MHz +15 dBm input from the Reference Oscillator is applied to the Power Splitter consisting of R1, R2, R3, and R4. One output of the Power Splitter goes to the Sampler of the High Frequency Loop (shown on Service Sheet 1). The other output is ac coupled by C2 to Q8, the first multiplier stage. Here, the 50 MHz is doubled four times to a frequency of 800 MHz.

Each of the four multiplier stages (Q8, 7, 6, and 5) is dc biased so the transistor operates in its non-linear region thus generating harmonics. The output of each stage is filtered by a bandpass filter at 100, 200, 400, or 800 MHz. This passes the doubled frequency and filters out the input frequency and other harmonics. Since the stages are electrically equivalent, only the first stage will be discussed in detail. Note, however, that the 800 MHz filter ultilizes printed circuit trace capacitors instead of discrete capacitors.

Resistors R5 and R6 divide the +5 Vdc supply voltage to dc bias the base of Q8 at approximately +1.0 Volts dc without the 50 MHz signal connected. Resistor R7 is the emitter bias resistor. Capacitor C6 bypasses the ac emitter signal to ground. Inductor L2 is an RF choke, capacitor C3 is an RF bypass and C4 ac couples the output to the 100 MHz Bandpass Filter. The 800 MHz output of the last multiplier stage Q5 is applied to the 800 MHz Bandpass Filter on the output Assembly A6 (shown on Service Sheet 5) and to Buffer Amplifier No. 1.

Buffer Amplifier No. 1/Mixer U1

The 800 MHz signal is coupled to the base of Q3 through resistor R11, the circuit board transmission line and capacitor C13. The transmission line serves to isolate Q3 from the input. DC current flows through resistors R14 and 15 to dc bias the base of Q4. Since the emitter of Q4 is also connected to the +5V(F) supply by resistor R18, the emitter voltage will be approximately 0.6 Vdc more positive than the base. The current through resistor R18 is determined by the voltage difference between the +5 Vdc supply and the voltage at the emitter of Q4. The current through R18 takes two paths. One path is into the emitter of Q4 and out at its collector. This current minus the base current of Q4 is the base current of Q3. The other path for the current from R18 flows through L12 and into the collector of Q3. The base to collector current ratio depends on the dc current gain of Q3. Therefore, the total current from R18 is equal to the emitter current of Q3. Inductor L11 is an RF choke while L12 serves as a matching element. Capacitors C15, C20, and C21 are RF by-pass capacitors. Capacitor C24 ac couples the output of the Buffer Amplifier to Mixer U1. The other input to Mixer U1 is the 60 to 110 MHz from the Voltage Controlled Oscillator (refer to Service Sheet 8). The difference output of 690 to 740 MHz is ac coupled to Buffer Amplifier No. 2.

Buffer Amplifiers No. 2 and 3

The dc current flowing through resistors R25 and R26 dc bias the base of Q2 at approximately 2.0 Vdc. Resistor R27 is the emitter bias resistor and capacitors C36 and C37 are the emitter resistor bypass to ground. Inductor L24 is an RF choke while capacitors C38 and C39 are RF bypass capacitors. L23, L25 and C41 all serve as matching elements. The output of Buffer Amplifier No. 2 is ac coupled to the Compensation Network by capacitor C41. The Compensation Network is adjusted to keep the 690 to 740 MHz flatness within ±1.5 dB. The signal is ac coupled to Buffer Amplifier No. 3 which functions the same as Buffer Amplifier No. 2. The output of the buffer amplifier passes through Bandpass Filter FL1 which passes the difference frequencies (between 690 and 740 MHz) from the Mixer and filters and eliminates all the other frequencies. A frequency between 690 and 740 MHz goes to the Mixer in the High Frequency Loop (refer to Service Sheet 1) to serve as a phase locked reference for the High Frequency Voltage Controlled Oscillator.

TROUBLESHOOTING

Procedures for checking circuits of the A8 Frequency Multiplier Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a check mark and a number inside, e.g. ⟨√3⟩. Fixed voltages are shown on the schematic inside a hexagon, e.g. ⟨2V±0.2V⟩ Transistor bias voltages are shown without tolerances.

Test Equipment

Power Meter	HP 436A
Power Sensor	HP 8482A
Digital Multimeter	HP 3456A
Frequency Counter	HP 5328A
Adapter-Probe	HP 1250-1598
Adapter-Type N(male) to BNC (female)	HP 1250-0780
Cable-BNC(male) to SMC(female)	HP 08662-60080

⟨√1⟩ Multiplier Stages Bias Voltages

1. Set the Signal Generator to any frequency.

2. Measure and verify the bias voltages as indicated in Table 1.

⟨√2⟩ RF Levels

1. Set the Signal Generator to any frequency.

2. Check 50 MHz Reference Oscillator input to Frequency Multiplier Assembly at W5 with W5 disconnected. The level should be +15 dBm ±4.0 dB.

3. Reconnect

4. Check 60 t
Assembly at V

5. Reconnect

6. Table 2 sh
surement. Ver

Condi
All Cables (
W10 Not C
Jumper R
Filter Not (

EET 3 (Cont'd)

Table 1. Multiplier Stages Bias Voltages

Transistor	50 MHz Input Signal (Vdc)	
	Connected	Not Connected
Q8-E (J2-Pin 2) Q8-B Q8-C	+0.8 +1.0 +5.0	+0.23 to 0.47 +1.0 +5.0
Q7-E (J2-Pin 4) Q7-B Q7-C	+0.35 +1.0 +5.0	+0.23 to 0.47 +1.0 +5.0
Q6-E (J2-Pin 6) Q6B	+0.8 +1.0	+0.23 to 0.47 +1.0
Q5-E (J2-Pin 8) Q5-B Q5-C	+0.8 +1.0 +5.0	+0.23 to 0.47 +1.0 +5.0

W5.

o 110 MHz Low Frequency Loop input to Frequency Multiplier
V3 with W3 disconnected. The level should be −7 dBm ±2.0 dB

W3.

ows power levels at various points and the conditions for mea-
ify that each level is within the required range.

Table 2. RF Power Levels

ions	RF Power Levels (dBm) at Measurement Locations				
	W10	TP3	TP2	TP1	Filter Output
Connected	+7 to +1	+8 to +2	+8 to +2	−20 to −14	+8 to +2
onnected	+9 to +5	+9 to +5	+9 to +5	–	–
emoved		–	–	−14 to −10	–
Connected	–	–	–	–	+7 to +3

High Frequency Loop Amplifier and Control
P/O A4
SERVICE SHEET 2

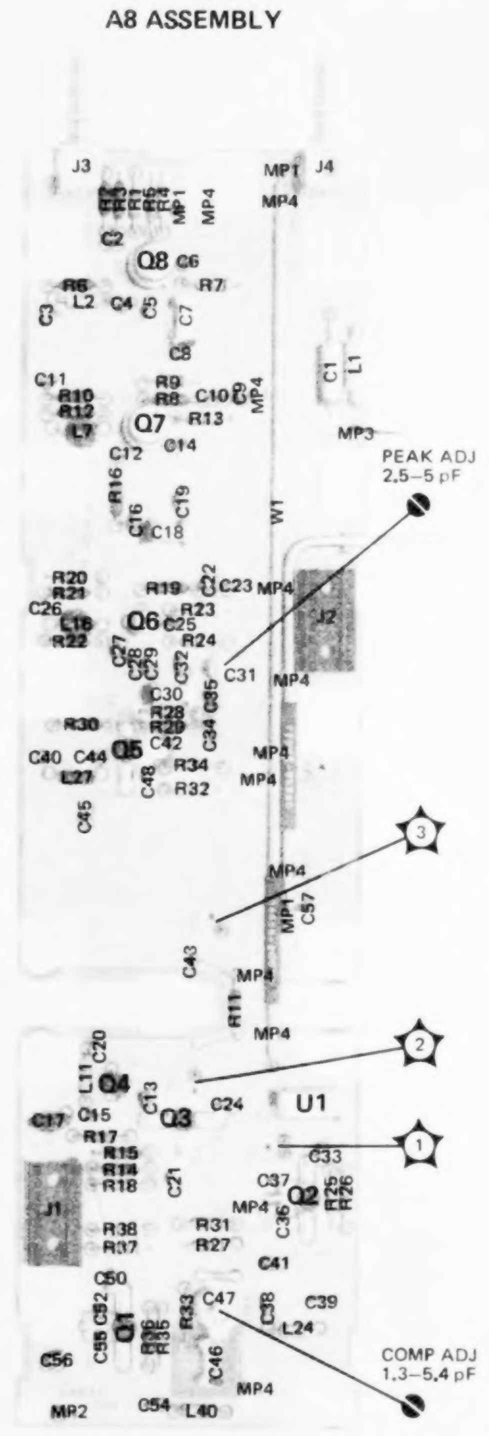
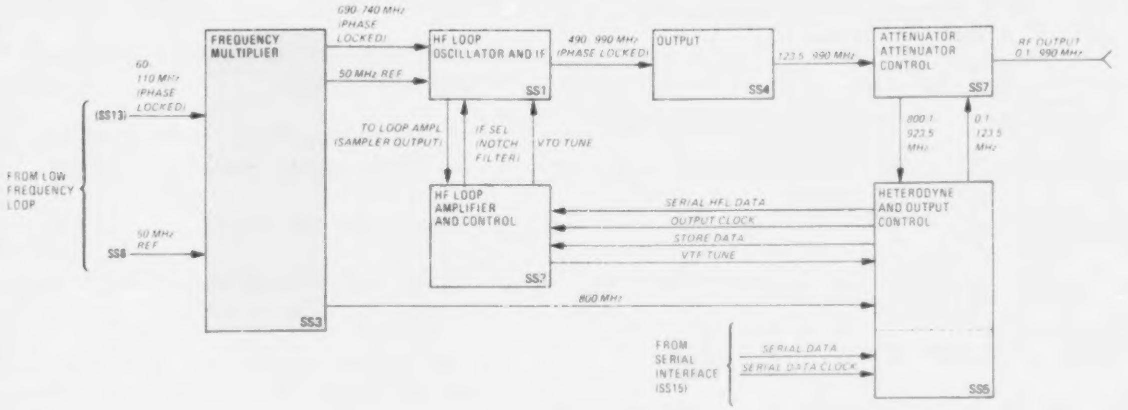

A8 ASSEMBLY
J3
J4
MP1
MP4
R1
R2
R3
R4
R5
C2
Q8
C6
R6
L2
C4
C5
R7
C3
C7
C8
C1
L1
C11
R9
R8
C10
C9
R10
R12
Q7
R13
L7
C12
C14
MP3
PEAK ADJ
2.5–5 pF
R16
C19
W1
C16
C18
R20
R21
R19
C22
C23
C26
R23
L16
Q6
C25
J2
R22
R24
C27
C28
C29
C32
C31
C30
C35
R28
R29
R30
C42
C34
C40
C44
Q5
L27
C48
R34
R32
C45
3
C57
C43
R11
MP4
C20
2
L11
Q4
C13
C24
U1
C17
C15
Q3
R17
1
R15
C33
R14
R18
C21
C37
Q2
R25
R26
J1
C36
R38
R31
R37
R27
C41
C50
C47
C38
C39
C52
Q1
R36
R35
R33
L24
C55
C56
C46
COMP ADJ
1.3–5.4 pF
MP2
C54
L40

Figure 8-44. Frequency Multiplier Component Locations


FREQUENCY MULTIPLIER
SS3
FROM LOW FREQUENCY LOOP
(SS13)
60-110 MHz (PHASE LOCKED)
SS8
50 MHz REF
690-740 MHz (PHASE LOCKED)
50 MHz REF
HF LOOP OSCILLATOR AND IF
SS1
490-990 MHz (PHASE LOCKED)
OUTPUT
SS4
123.5-990 MHz
ATTENUATOR ATTENUATOR CONTROL
SS7
RF OUTPUT 0.1-990 MHz
TO LOOP AMPL (SAMPLER OUTPUT)
IF SEL (NOTCH FILTER)
VTO TUNE
800.1-923.5 MHz
0.1-123.5 MHz
HF LOOP AMPLIFIER AND CONTROL
SS2
SERIAL HFL DATA
OUTPUT CLOCK
STORE DATA
VTF TUNE
HETERODYNE AND OUTPUT CONTROL
800 MHz
FROM SERIAL INTERFACE (SS15)
SERIAL DATA
SERIAL DATA CLOCK
SS5

FREQUENCY MULTIPLIER

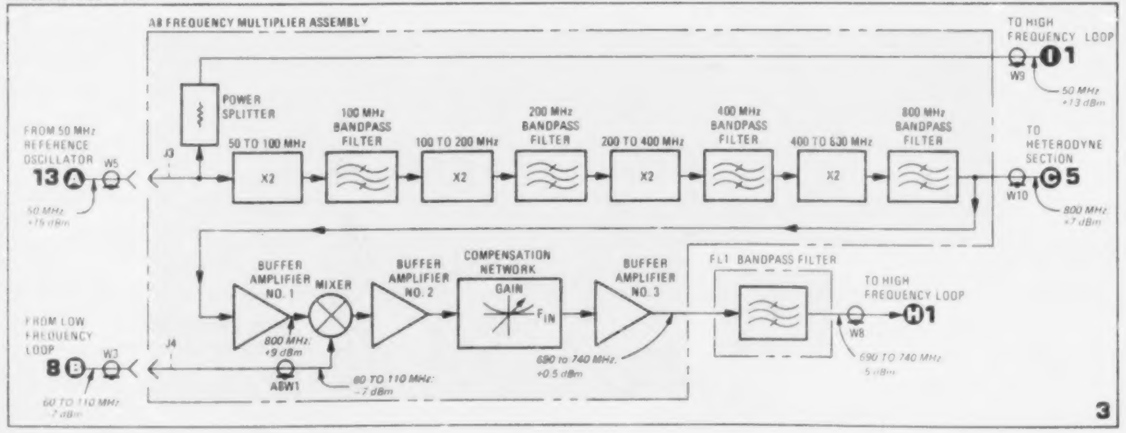
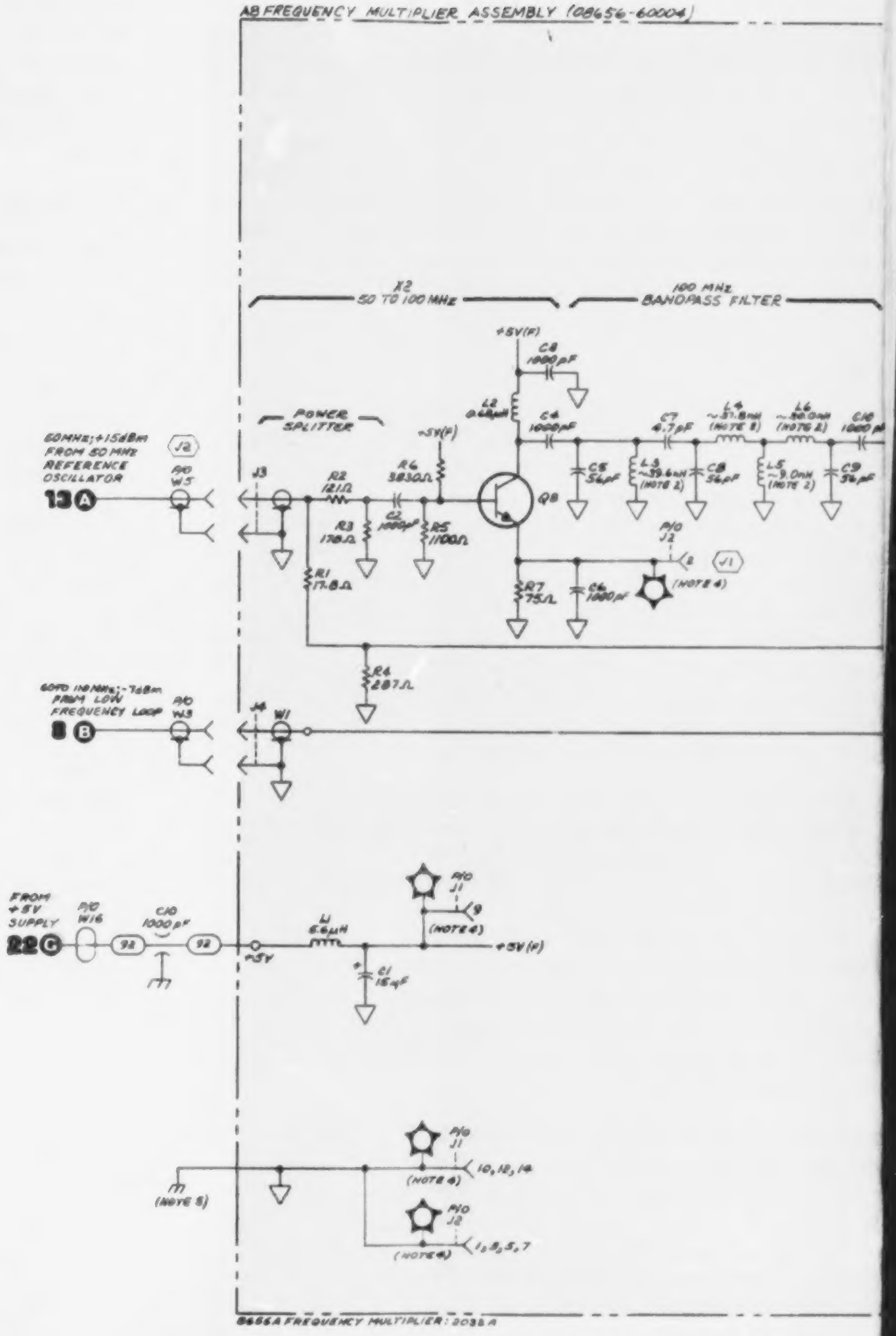
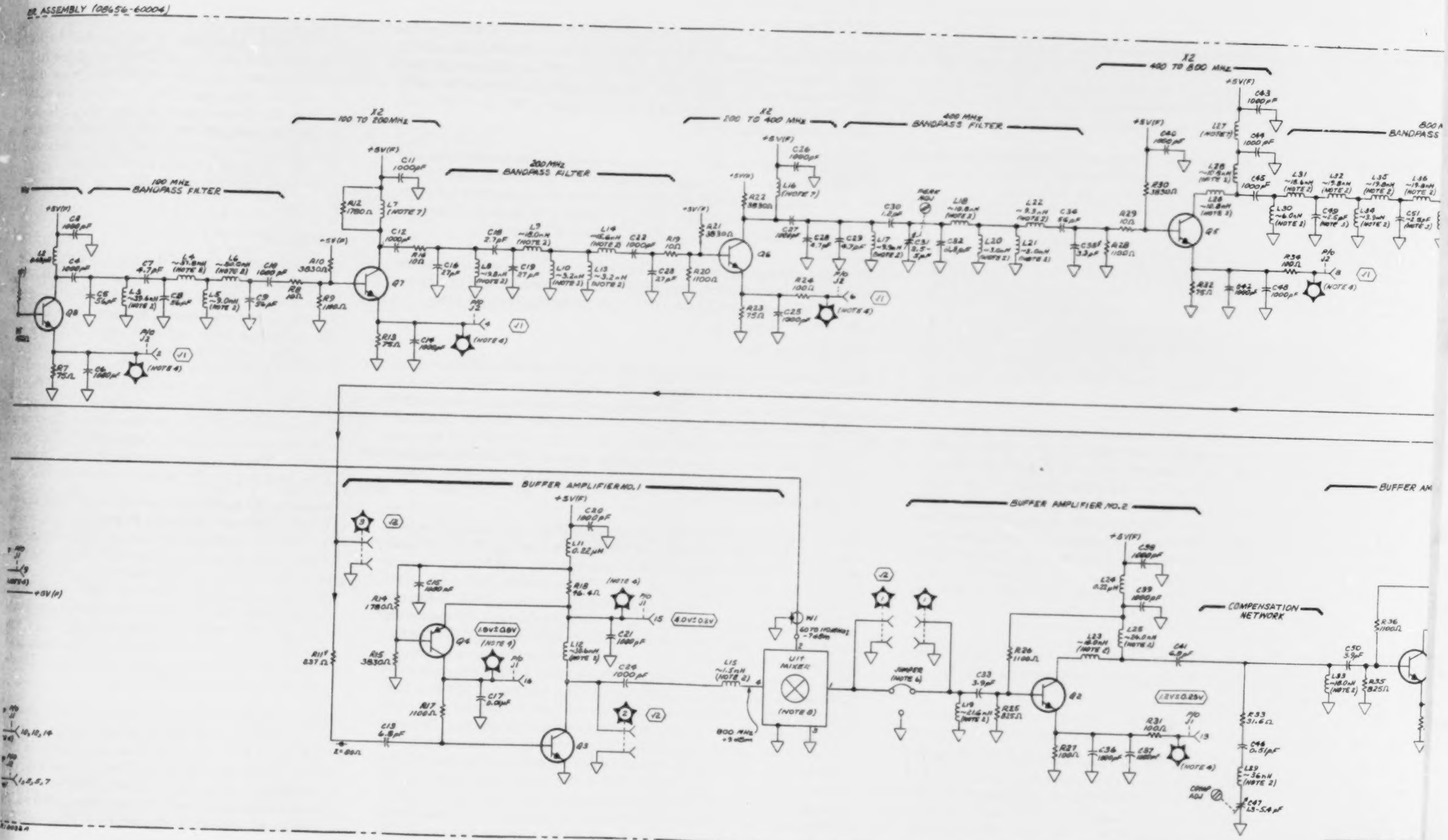
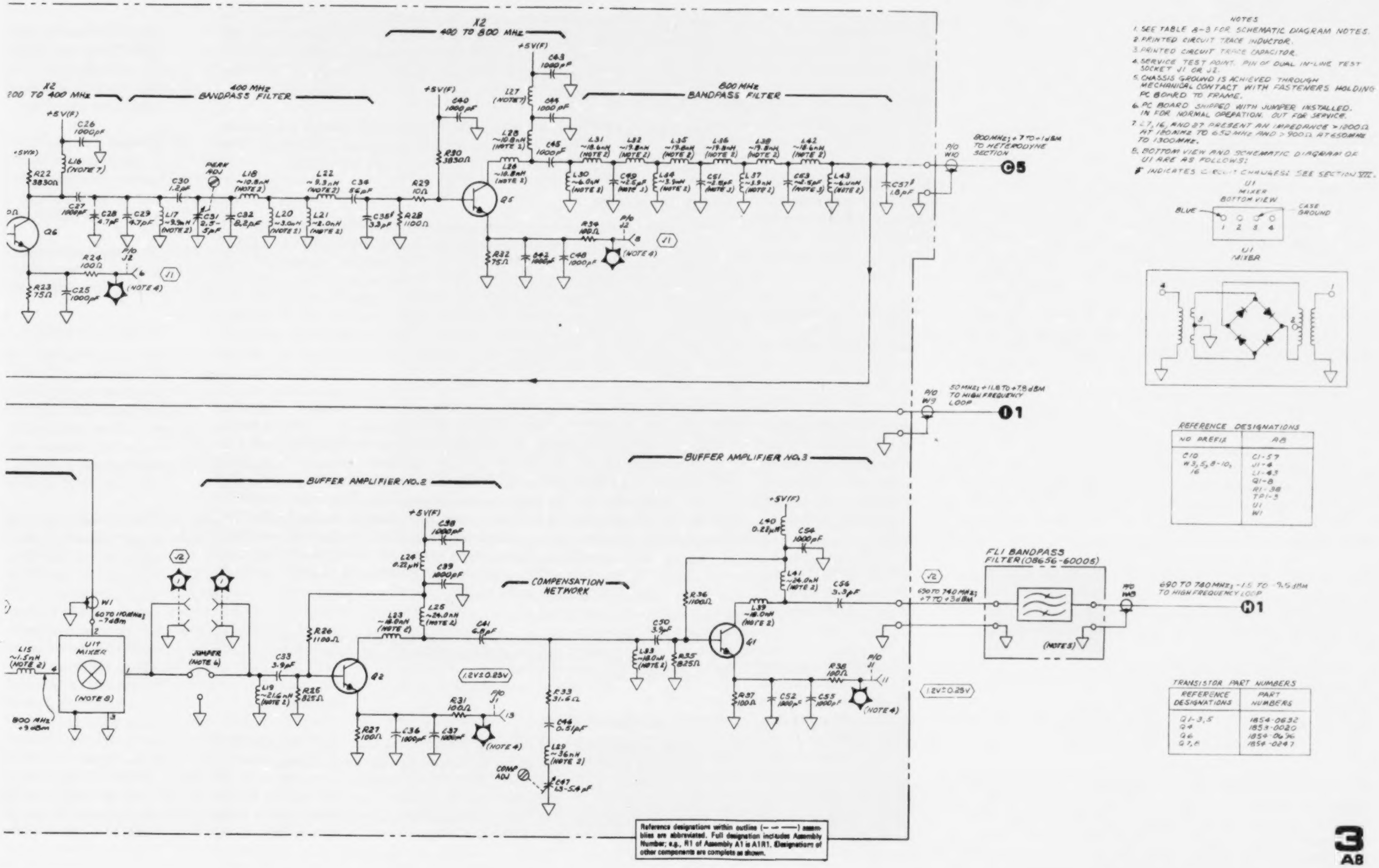

A8 FREQUENCY MULTIPLIER ASSEMBLY
TO HIGH FREQUENCY LOOP
W9
I1
50 MHz +13 dBm
POWER SPLITTER
FROM 50 MHz REFERENCE OSCILLATOR
13 A
W5
J3
50 MHz +15 dBm
50 TO 100 MHz
X2
100 MHz BANDPASS FILTER
100 TO 200 MHz
X2
200 MHz BANDPASS FILTER
200 TO 400 MHz
X2
400 MHz BANDPASS FILTER
400 TO 830 MHz
X2
800 MHz BANDPASS FILTER
TO HETERODYNE SECTION
W10
C5
800 MHz +7 dBm
BUFFER AMPLIFIER NO. 1
MIXER
BUFFER AMPLIFIER NO. 2
COMPENSATION NETWORK
GAIN
F_IN
BUFFER AMPLIFIER NO. 3
FL1 BANDPASS FILTER
TO HIGH FREQUENCY LOOP
W8
H1
690 TO 740 MHz 5 dBm
800 MHz +9 dBm
690 to 740 MHz +0.5 dBm
FROM LOW FREQUENCY LOOP
8 B
W3
J4
A8W1
60 TO 110 MHz -7 dBm
60 TO 110 MHz -7 dBm
3

Figure 8-45. Frequency Multiplier Block Diagrams


A8 FREQUENCY MULTIPLIER ASSEMBLY (08656-60004)
X2 50 TO 100 MHz
100 MHz BANDPASS FILTER
POWER SPLITTER
60MHz;+15dBm FROM 50 MHz REFERENCE OSCILLATOR
J2
P/O W5
13 A
J3
R2 121Ω
R3 178Ω
R1 17.8Ω
C2 1000pF
R6 3830Ω
R5 1100Ω
+5V(F)
+5V(F)
C8 1000pF
L2 0.68μH
C4 1000pF
Q8
C5 56pF
C7 4.7pF
L3 ~39.6nH (NOTE 2)
C8 56pF
L4 ~37.8nH (NOTE 2)
L5 ~9.0nH (NOTE 2)
L6 ~30.0nH (NOTE 2)
C9 56pF
C10 1000pF
R7 75Ω
C6 1000pF
P/O J2
2
J1
(NOTE 4)
R4 287Ω
60 TO 110 MHz;-7dBm FROM LOW FREQUENCY LOOP
8 B
P/O W3
J4
W1
FROM +5V SUPPLY
22 G
P/O W16
92
C10 1000pF
92
+5V
L1 5.6μH
C1 15μF
P/O J1
9
(NOTE 4)
+5V(F)
(NOTE 5)
P/O J1
10, 12, 14
(NOTE 4)
P/O J2
1, 3, 5, 7
(NOTE 4)
8656A FREQUENCY MULTIPLIER: 2038A


ASSEMBLY (08656-60004)
100 MHz BANDPASS FILTER
X2 100 TO 200MHz
200 MHz BANDPASS FILTER
X2 200 TO 400 MHz
400 MHz BANDPASS FILTER
X2 400 TO 800 MHz
800 M
BANDPASS
+5V(F)
Q8
Q7
Q6
Q5
Q4
Q3
Q2
C8 1000pF
C4 1000pF
C5 56pF
L3 ~39.6nH (NOTE 2)
C7 4.7pF
C8 56pF
L4 ~51.8nH (NOTE 2)
L5 ~3.0nH (NOTE 2)
L6 ~50.0nH (NOTE 2)
C9 56pF
C10 1000pF
R8 10Ω
R10 3830Ω
R9 1100Ω
R7 75Ω
C6 1000pF
P/O J2
(NOTE 4)
J1
C11 1000pF
R12 1780Ω
L7 (NOTE 7)
C12 1000pF
R14 10Ω
R13 75Ω
C14 1000pF
C16 27pF
C18 2.7pF
L8 ~19.8nH (NOTE 2)
C19 27pF
L9 ~18.0nH (NOTE 2)
L10 ~3.2nH (NOTE 2)
L13 ~3.2nH (NOTE 2)
L14 ~18.6nH (NOTE 2)
C22 1000pF
C23 27pF
R19 10Ω
R20 1100Ω
R21 3830Ω
R22 3830Ω
C26 1000pF
L16 (NOTE 7)
C27 1000pF
C28 4.7pF
C29 4.7pF
R23 75Ω
C25 1000pF
R24 100Ω
C30 1.2pF
PEAK ADJ
L17 ~9.9nH (NOTE 2)
C31 0.5-5pF
L18 ~10.8nH (NOTE 2)
C32 6.8pF
L20 ~3.0nH (NOTE 2)
L21 ~3.0nH (NOTE 2)
L22 ~9.3nH (NOTE 2)
C34 56pF
C35 3.3pF
R28 1100Ω
R29 10Ω
C40 1000pF
R30 3830Ω
C43 1000pF
L27 (NOTE 7)
C44 1000pF
L28 ~10.5nH (NOTE 2)
L26 ~10.8nH (NOTE 2)
C45 1000pF
L30 ~6.0nH (NOTE 2)
L31 ~18.6nH (NOTE 2)
L32 ~19.8nH (NOTE 2)
C49 ~2.6pF (NOTE 3)
L34 ~3.9nH (NOTE 2)
L35 ~19.8nH (NOTE 2)
L36 ~19.8nH (NOTE 2)
C51 ~2.5pF (NOTE 3)
R32 75Ω
C42 1000pF
C48 1000pF
R34 100Ω
BUFFER AMPLIFIER NO. 1
C20 1000pF
L11 0.22μH
C15 1000pF
R14 1780Ω
R15 3830Ω
R18 46.4Ω
P/O J1
4.0V±0.2V
1.0V±0.8V
(NOTE 4)
C21 1000pF
L12 ~36nH (NOTE 2)
C24 1000pF
C17 0.01μF
R11 237Ω
R17 1100Ω
C13 6.8pF
Z=80Ω
L15 ~1.5nH (NOTE 2)
W1
60 TO 110dBm
-7dBm
U17 MIXER (NOTE 8)
800 MHz +3dBm
J2
JUMPER (NOTE 4)
BUFFER AMPLIFIER NO. 2
C38 1000pF
L24 0.22μH
C39 1000pF
L25 ~24.0nH (NOTE 2)
L23 ~18.0nH (NOTE 2)
C41 6.8pF
R26 1100Ω
C33 3.9pF
L19 ~21.6nH (NOTE 2)
R25 825Ω
1.2V±0.25V
R27 100Ω
C36 1000pF
C37 1000pF
R31 100Ω
COMPENSATION NETWORK
R33 31.6Ω
C46 0.51pF
L29 ~36nH (NOTE 2)
COMP ADJ
C47 1.3-5.4pF
C50 3.9pF
L33 ~18.0nH (NOTE 2)
R35 825Ω
R36 1100Ω
BUFFER AM
+5V(P)
10, 12, 14
1, 2, 5, 7

Reference designations within
blies are abbreviated. Full desi
Number; e.g., R1 of Assembly A
other components are complete


X2
200 TO 400 MHz
400 MHz
BANDPASS FILTER
X2
400 TO 800 MHz
800 MHz
BANDPASS FILTER
+5V(F)
+5V(H)
R22 3830Ω
C26 1000pF
L16 (NOTE 7)
C27 1000pF
C28 4.7pF
C29 4.7pF
C30 1.2pF
PEAK ADJ
C31 2.5-5pF
L17 ~9.9nH (NOTE 2)
L18 ~10.8nH (NOTE 2)
C32 8.2pF
L20 ~3.0nH (NOTE 2)
L21 ~2.0nH (NOTE 2)
L22 ~9.3nH (NOTE 2)
C34 56pF
C35 3.3pF
R28 1100Ω
R29 10Ω
R30 3830Ω
C40 1000pF
Q6
R24 100Ω
P/O J2
6
J1
R23 75Ω
C25 1000pF
(NOTE 4)
L27 (NOTE 7)
C43 1000pF
C44 1000pF
L28 ~10.8nH (NOTE 2)
C45 1000pF
L26 ~10.8nH (NOTE 2)
Q5
L31 ~18.6nH (NOTE 2)
L32 ~19.8nH (NOTE 2)
L35 ~19.8nH (NOTE 2)
L36 ~19.8nH (NOTE 2)
L38 ~19.8nH (NOTE 2)
L42 ~18.6nH (NOTE 2)
L30 ~6.0nH (NOTE 2)
C49 ~2.5pF (NOTE 3)
L34 ~3.9nH (NOTE 2)
C51 ~2.5pF (NOTE 3)
L37 ~3.9nH (NOTE 2)
C53 ~2.5pF (NOTE 3)
L43 ~6.0nH (NOTE 2)
C57 1.8pF
R34 100Ω
P/O J2
8
R32 75Ω
C42 1000pF
C48 1000pF
P/O W10
800 MHz; +7 TO +1dBM TO HETERODYNE SECTION
C5
P/O W9
50 MHz; +11.8 TO +7.8 dBM TO HIGH FREQUENCY LOOP
D1
BUFFER AMPLIFIER NO.2
BUFFER AMPLIFIER NO.3
COMPENSATION NETWORK
W1
60 TO 110 MHz; -7dBm
U1T MIXER
(NOTE 8)
L15 ~1.5nH (NOTE 2)
800 MHz +9 dBm
J2
JUMPER (NOTE 6)
C33 3.9pF
L19 ~21.6nH (NOTE 2)
R25 825Ω
R26 1100Ω
Q2
C38 1000pF
L24 0.22μH
C39 1000pF
L25 ~24.0nH (NOTE 2)
L23 ~18.0nH (NOTE 2)
C41 6.8pF
1.2V±0.25V
R31 100Ω
P/O J1
13
R27 100Ω
C36 1000pF
C37 1000pF
R33 31.6Ω
C46 0.51pF
L29 ~36nH (NOTE 2)
COMP ADJ
C47 1.3-5.4pF
C50 3.9pF
L33 ~18.0nH (NOTE 2)
R35 825Ω
R36 1100Ω
Q1
L40 0.22μH
C54 1000pF
L41 ~24.0nH (NOTE 2)
L39 ~18.0nH (NOTE 2)
C56 3.3pF
R37 100Ω
C52 1000pF
C55 1000pF
R38 100Ω
P/O J1
11
690 TO 740 MHz; +7 TO +3dBM
FL1 BANDPASS FILTER (08656-60005)
(NOTE 5)
P/O W8
690 TO 740 MHz; -1.5 TO -9.5 dBM TO HIGH FREQUENCY LOOP
H1
U1 MIXER BOTTOM VIEW
BLUE
CASE GROUND
1 2 3 4
U1 MIXER

Reference designations within outlines (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. PRINTED CIRCUIT TRACE INDUCTOR.
3. PRINTED CIRCUIT TRACE CAPACITOR.
4. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKET J1 OR J2.
5. CHASSIS GROUND IS ACHIEVED THROUGH MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
6. PC BOARD SHIPPED WITH JUMPER INSTALLED. IN FOR NORMAL OPERATION. OUT FOR SERVICE.
7. L7, 16, AND 27 PRESENT AN IMPEDANCE >1200Ω AT 180MHz TO 650MHz AND >900Ω AT 650MHz TO 1300MHz.
8. BOTTOM VIEW AND SCHEMATIC DIAGRAM OF U1 ARE AS FOLLOWS:

✱ INDICATES CIRCUIT CHANGES; SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A8
C10 W3, 5, 8-10, 16	C1-57 J1-4 L1-43 Q1-8 R1-38 TP1-3 U1 W1

TRANSISTOR PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-3, 5	1854-0632
Q4	1853-0020
Q6	1854-0696
Q7, 8	1854-0247

3
A8

Figure 8-46. Frequency Multiplier Schematic Diagram

SERVICE SHEET 4
P/O A6 OUTPUT ASSEMBLY
P/O A7 RFI ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD2
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The 494 to 990 MHz signal from the High Frequency Oscillator is input to the RF Dividers. The signal is divided by one, two or four depending on the frequency selected at the front panel. The signal passes through the PIN Diode Modulator to the inputs to the Voltage-Tuned Filters. The signal is passed through one of the three filters as determined by the selected frequency. The filter output is amplified and coupled to the output attenuator and the Automatic Level Control (ALC) Loop.

In the ALC loop, the RF signal level is detected and compared to the dc component of the AM Ref Level input. The difference is amplified and coupled back to the PIN Modulator which acts as a current controlled attenuator. The loop serves to hold the output at a constant level.

RF Dividers

The 494 to 990 MHz oscillator output signal from the High Frequency Loop Amplifier (−3 to +4 dBm) is applied to the Output Assembly. The signal is ac coupled by C1 into the RF Dividers where they are divided by one, two or four depending on the Output Frequency selected at the front panel. The RF Dividers divide-by-one when an output frequency from 494 to 990 MHz, or less than 123.5 MHz is selected. The RF Divider divides-by-two when an output frequency from 247 to 494 MHz is selected. It divides-by-four when an output frequency from 123.5 to 247 MHz is selected.

When the RF Divider is configured to divide-by-one, the logic output of the Band Select Dividers for divide-by-one is set low by the third bit of RF Word 2, (refer to Service Sheet 5). With the divide-by-one control line low, diodes CR5 and CR7 are turned on and the signal is coupled by C13 to the PIN Modulator.

In the divide-by-two configuration, the second bit of RF Word 2 sets the divide-by-two control line low and diodes CR2, CR3 and CR9 are turned on. With diode CR3 turned on, C2 couples the input signal to U1 where it is divided by two. The output of U1 is dc coupled to Q1 which functions as an emitter-follower. The output of Q1 is coupled to the PIN (diode) Modulator by C12. Inductor L7 supplies bias voltage for U1.

Diodes CR4 and CR6 along with either CR1 or CR2 (depending on which is selected) provide voltage offsets from +5 Vdc and ground to the bias resistors R2 and R4. The result is a bias voltage of about +2.7 Vdc at the input to U1. This ensures proper triggering on the RF signal in the divide-by-two or divide-by-four modes. Diodes CR4 and CR6 are also used for temperature compensation. Inductors L2, L6 and L7 are RF chokes that pass the dc control voltages and block the RF voltages.

In the divide-by-four configuration, the first bit of RF Word 2 sets the divide-by-four control line low and diodes CR1, CR3, CR11 and CR12 are turned on. The input signal is applied to U1 which functions the same as in the divide-by-two mode. The output of

U1 is applied to Q1 which can no longer function as an emitter follower with CR9 turned off. The output is coupled from the collector of Q1 to the input of the second divider U2 by C11. Divider U2 is activated when CR11 is turned on so U2 pin 9 is pulled low. RF Divider U2 is always biased at the right voltage by R12 and R13 (+3.6 Vdc). U2 is temperature compensated by CR8 and CR10. The output of U2 is coupled by C21 and C22 to the PIN Modulator.

Inductors L14, L15 and L16 are RF chokes and resistor R15 biases the output of divider U2. Resistor R1 and inductor L1 supply dc bias voltage from CR3, CR5 and CR7 and block the RF signal.

PIN Modulator

The PIN Modulator consists of three series PIN diodes CR13, CR14 and CR18. There is a 20Ω transmission line between CR13 and CR14 and between CR14 and CR18. PIN diodes function as current controlled RF resistors where the RF resistance is inversely proportional to the current through the diodes. Approximately 50 mA current through the diodes will cause them to appear as shorts and the 20Ω transmission lines will cause a small mismatch resulting in an insertion loss of about 2 dB between the modulator's input and output.

With less than 50 mA, the diodes appear as resistors of several hundred ohms. The transmission line appears as a large capacitance. In this condition the frequency response would roll off at 6 dB/octave for a total of 18 dB for the three octaves. The input inductor L17 and resistor R16, the output inductor L18, resistor R19 and capacitor C23 function to compensate the frequency response by increasing the input and output impedance at the higher frequencies. At the lower frequencies the impedance is a few hundred ohms with a small reactance in series which decreases the gain at the lower frequencies. The modulator flatness over the three octaves is reduced to approximately ±3 dB.

The PIN Modulator is enclosed in a waveguide-beyond-cutoff filter that isolates the input from the output and provides 70 dB of dynamic range.

Voltage-Tuned Filters

Three voltage-tuned low pass filters pass the 123.5 to 990 MHz output of the PIN Modulator to remove the harmonics generated by the dividers and oscillator. Each filter covers one octave of the frequency range; therefore the harmonics are not passed to the Output Amplifier. The tune voltages for all the filter's are derived from the VTF TUNE line of the A4 Assembly's Loop Amplifier (refer to Service Sheet 2). This tune voltage is dependent on the frequency selected and is offset, amplified, and applied to the correct VTF by the VTF Drivers (part of the A6 Assembly; refer to Service Sheet 5). The +3 to +15 volts that tunes each Voltage Tuned Filter, tracks the tune voltage for the VCO as the oscillator is tuned from 494 to 990 MHz. Since the Voltage Tuned Filters are low pass filters, it is not a

problem if the filter selected is tuned to its highest frequency before the Voltage Controlled Oscillator reaches its highest frequency.

The VTF Drivers turn on the selected input and output diodes of the VTF. These are CR20 and CR36, CR19 and CR35 or CR21 and CR34. The current that biases on the input and output diodes is returned to the −15 volt supply by the VTF input resistors R21 and R98 and output resistor R29.

When a Voltage-Tuned Filter is not selected, the varactor diodes and parallel diodes at the input and output are forward biased by the current through R24, R25 or R26. This tends to increase the isolation of the unused filters. Note that the input and output diodes are biased off. Inductors L22, L23 and L24 are RF chokes.

The tune voltage of +3 to +15 volts will vary the capacitance of the varactors approximately 7 to 32 pF in the divide-by-2 and divide-by-4 filters and approximately 3.5 to 8 pF in the divide-by-1 filter.

Output Amplifier

The output of the Voltage Tuned Filters is ac coupled to the two stage Output Amplifier by capacitors C30 and C33. Capacitors C28 and 31 are distributed along the connecting transmission line to match the output of the Voltage Tuned Filters to the input of the Output Amplifier. The amplifier's input resistor R34 and inductor L31 give an input impedance of approximately 50 ohms at the low frequencies. At the high frequencies feedback in the Output Amplifier provides a 50 ohm input impedance.

The Output Amplifier is a two stage amplifier consisting of transistors Q2 and 7. Transistor Q3 provides active bias for Q2 and Q6 does the same for Q7. Transistor Q3 is biased on by +10.6 Vdc (+15 Vdc divided by resistors R10 and R11). The emitter voltage is then approximately +11.2 Vdc and current flow through Q2 will influence this emitter voltage. A current flow increase through Q2 decreases the emitter voltage. This reduces the current through Q3 thus reducing the bias voltage at the base of Q2. Therefore the current through Q2 is reduced. The net effect is that Q3 and Q6 provide negative feedback to Q2 and Q7 respectively. The emitter of Q2 has four resistors R39, R43, R44 and R47 in parallel and a bypass capacitor C39. All are used to reduce the inductance at the emitter. Resistor R45, inductor L32 and capacitor C34 provide an RF shunt feedback path from the collector to the base of Q2. At low frequencies, (100 to 500 MHz) the input impedance of Q7 is zero ohms and there is no RF voltage at the collector of Q2 and no shunt feedback. At the higher frequencies the input impedance of Q7 increases above zero ohms and there is an RF voltage feedback from collector to base of Q2. This feedback helps keep the input impedance of Q2 at approximately 50 ohms as the reactance of L31 masks the 50Ω resistor R34. Masking the 50 ohm input resistor increases the input to Q2 by approximately 3 dB and therefore the amplifier's output increases the same amount. The last amplifier Q7 is a grounded emitter shunt feedback amplifier. RF feedback is by resistor R51, inductor L35 and

SERVICE SHEET 4 (Cont'd)

capacitor C40. The total voltage gain of the Output Amplifier is approximately 24 dB from the input of Q2 to the collector of Q7.

The Output Amplifier is ac coupled by C42 to the attenuator (through R53) and to the Detector of the ALC Loop. Resistor R53 approximates a 50 ohm output impedance. The 34.8Ω of the resistor and 5Ω of loss in associated circuitry account for an output impedance of 40 ohms which is not enough of a mismatch to cause a standing wave problem. This will reduce the power loss of the signal applied to the attenuator or to the heterodyne mixer for output frequencies from 100 kHz to 123.5 MHz. The power level of -7 to +15 dBm from the Output Amplifier is measured on the output side of R53.

ALC Loop

The Output Detector of the ALC Loop detects the RF voltage at the output of the High Band Output Amplifier. The level of the detected voltage is forced by the gain of the ALC Loop to be identical to the loop's reference voltage. Therefore, the Output Amplifier must be an RF voltage source and have zero ohms impedance. Resistor R50 provides a small amount of isolation between the detector diode CR39 and the Output Amplifier and rolls off the detector output by about 2 dB over the frequency range 123.5 to 990 MHz. The gain of the Output Amplifier increases about 2 dB and the attenuator losses increase about 2 dB over this range. This helps to keep the output flat without correction. Capacitor C37 couples the RF to detector diode CR39 and stores the dc charge. Inductor L33 and capacitor C36 filter out the RF present on the dc voltage.

Detector Bias. Transistors Q8 and Q12 bias on diodes CR38 and CR39. The transistors are biased on by the resistor divider network of R40, R41 and R42. Q8 biases on CR38 and is the current source for CR38. Q12 biases on CR39 and sinks the current from both CR38 and CR39 to the -15 Vdc supply. The Detector Adjustment (Det Adj) R35 is adjusted for identical currents flowing through CR38 and CR39. When the Detector Adjustment is adjusted correctly there is a voltage difference of approximately 54 mV between the cathodes of the two diodes. This is the ideal offset voltage for the diode detector when the detector is operating linearly. Diode CR38 also temperature compensates the detector.

ALC Amplifier. The dc voltage at the collector of Q8 is equal to the peak voltage of the RF output of the Output Amplifier except for the roll off of R50 and C37. This dc voltage is the positive input to the ALC Amplifier, U6. The voltage to the negative input is the dc level correction voltage and the amplitude modulation voltage when AM modulation is selected from the Audio/Power Supply, A10. The negative input voltage is shaped by resistors R27, R30, R31 and diodes CR31 and CR37. For very low levels, the input voltage characteristic should approximate the square law region of the detector. (The square law region is the non-linear portion of the detector's current-versus-voltage curve. In this region the change in current is proportional to the square of the change in voltage.) If the voltages to the inputs are the same, there is very little distortion.

SERVICE SHEET 4 (Cont'd)

TROUBLESHOOTING

Procedures for checking part of the circuits of the A6 Output Assembly are given below. The area or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g. ⟨√3⟩. Fixed voltages are shown on the schematic inside a hexagon, e.g. ⟨2V±0.2V⟩. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Oscilloscope	HP 1222A
Power Meter	HP 436A
Power Sensor	HP 8482A
Frequency Counter	HP 5328A
Adapter Probe	HP 1250-1598
Adapter-Type N(male) to BNC(female)	HP 1250-0780
Cable BNC(male) to SMC(female)	HP 08662-60080

⟨√1⟩ RF Dividers

1. Set the Signal Generator to -10 dBm without modulation.

2. Check the voltages and levels as shown in Tables 1 and 2 for each front panel frequency setting.

Table 1. RF Divider Voltages

Signal Generator Freq. (MHz)	Divider Voltages (Vdc)			Voltages at Q1 (Vdc)			Signal at TP1	
	÷1 SEL	÷2 SEL	÷4 SEL	E	B	C	Level (dBm)	Freq (MHz)
500	+0.2	+4.8	+4.8	+4.4	+5.1	+8.6	+3.0 to -3.0	500
300	+8.0	+0.2	+8.0	+4.4	+5.1	+8.6	+3.0 to -3.0	600
200	+14	+14	+0.2	+4.4	+5.1	+8.5	+3.0 to -3.0	800

◀ Frequency Multiplier
A8
SERVICE SHEET 3

SERVICE SHEET 4 (Cont'd)

Table 2. RF Divider Chip Inputs

Signal Generator Frequency (MHz)	Voltages (Vdc) on	
	U1-pin 3	U2-pin 9
500	+4.0	+5.0
300	+3.3	+5.0
200	+3.3	+1.0

√2 Voltage-Tuned Filter

1. Set the Signal Generator to -10 dBm without modulation.

2. Check the voltages in Table 3 for each front panel frequency setting. If loop is not locked, the signal will be a triangular wave.

3. Set the Signal Generator to -10 dBm without modulation.

4. Connect a power meter to test point 2 and check the levels listed in Table 4.

5. Set switch S1 to open position and measure the dc voltage at TP2. It should be -2.0 ±0.5 Vdc.

√3 High Band Output Amplifier

1. Check bias voltages on transistors Q2, Q3, Q6, and Q7.

2. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

3. Check the power level at W14 using the adaptor probe. The power level should be -3.5 dBm ±3.0 dB

4. Change the RF amplitude to +13 dBm.

5. Check the power level at W14. The power leve should be +9.0 dBm ±3.0 dB.

6. Verify that the frequency at W14 is 500.00 MHz ±2 kHz.

√4 ALC Amplifier

1. Set the Signal Generator to 500 MHz withou modulation.

Table 3. Voltage Tuned Filter Control Voltages

Signal Generator Frequency (MHz)	VTF TUNE Voltage (Vdc)		
	123.5 to 247 MHz	247 to 494	494 to 990 MHz
900	-0.5	-0.5	+14.0
600	-0.5	-0.5	+8.5
350	-0.5	+12.9	-0.5
300	-0.5	+8.5	-0.5
200	+14.2	-0.5	-0.5
150	+8.5	-0.5	-0.5

Table 4. ALC Loop Level Measurements

Test Point	ALC Loop Switch S1	Circuit Opened By*	Power Level (dBm)	
			Closed	Opened
TP2	Closed	Disconnect C24	-11 to -21	-14 to -18
TP2	Open	Disconnect C24	-5 to -10	-6 to -10
TP3	Closed	Disconnect C33,R34	-21 to -31	+1 to -1
TP3	Open	Disconnect C33,R34	-11 to -21	-7 to -11

*The circuit is opened by unsoldering one end of the component(s) and lifting the unsoldered end from the printed circuit board.

SERVICE SHEET 4 (Cont'd)

2. Check the voltages at the stated locations and for the various output amplitudes listed in Table 5.

3. Set the Signal Generator to -10 dBm at 500 MHz with 50% AM depth and an Internal 1 kHz rate.

4. Check the waveforms and the Logic Level as indicated in Figure 1.

Table 5. ALC Amplifier Voltage Levels

Amplitude (dBm)	Test Point Measurement (Vdc)		
	J3-pin 3	J3-pin 15 and J3-pin 16	J3-pin 4*
+13	-1.4 to -6.4	+1.97 to +1.87	L
+10	-1.1 to -4.1	+1.45 to +1.35	L
+5	-1.5 to -4.0	+0.85 to +0.75	L
0	-1.2 to -3.7	+0.49 to +0.39	L
-4	-1.1 to -3.6	+0.33 to +0.23	L
-5	-1.5 to -4.0	+0.84 to +0.74	L

*Signal Generator must be in CW mode. Low is <+0.8 Vdc; K1 is closed.

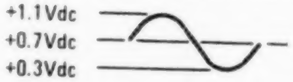
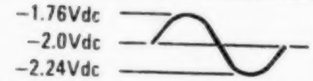
Test Point	Waveform
J3 Pin 15 and J3 Pin 16	
J3 Pin 3	
J3 Pin 4	Logic level high >2.0 Vdc, K1 should be open

Figure 1. ALC Amplifier Waveforms and Logic Level

P/O A7 ASSEMBLY

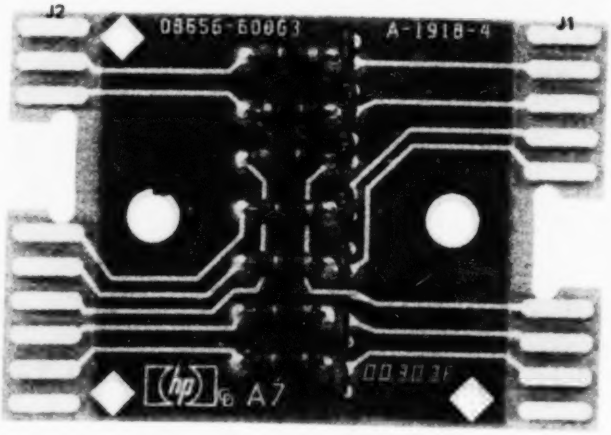


Figure 8-47. Output Section (A7 Assembly) Component Locations

P/O A6 ASSEMBLY

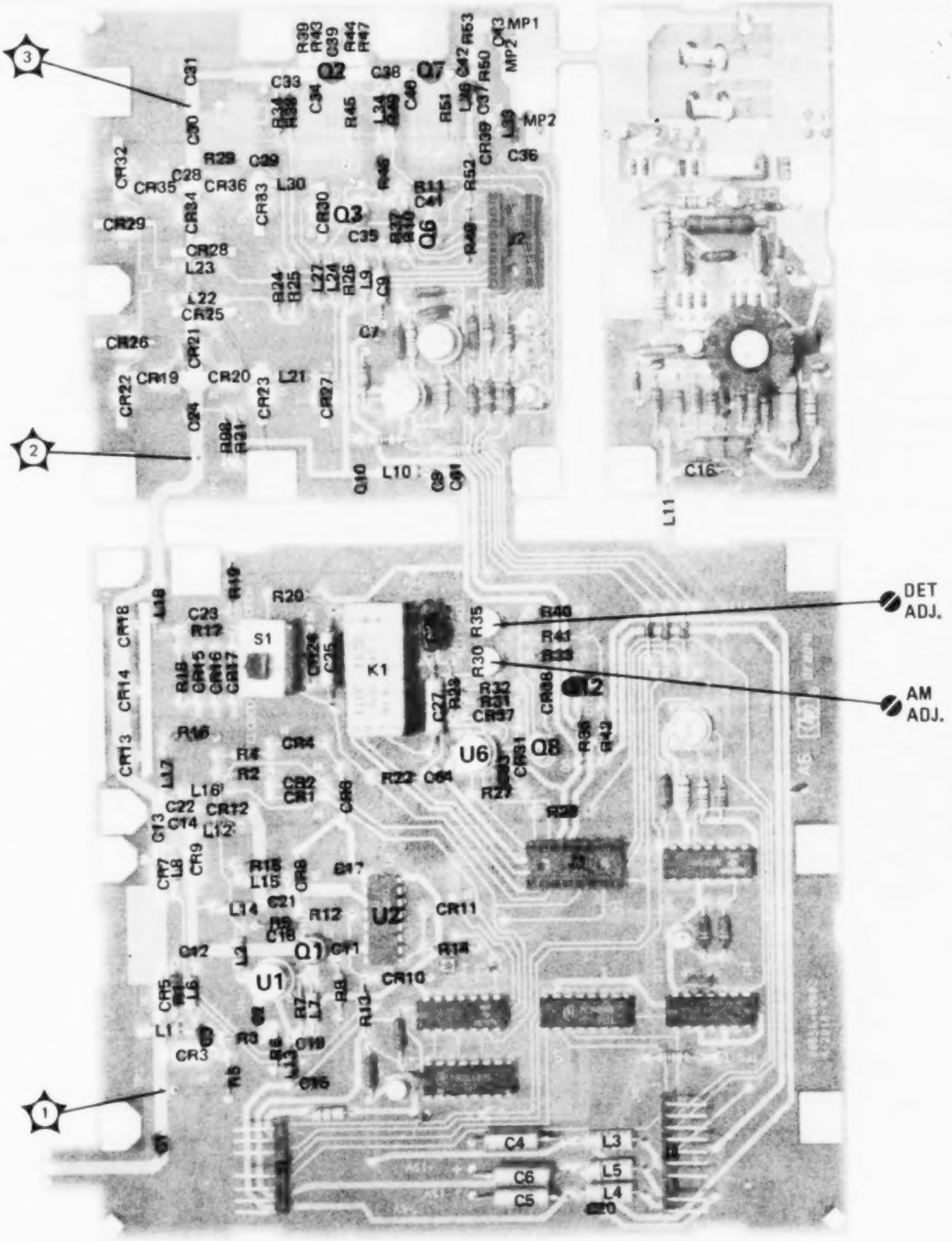

③
②
①
DET ADJ.
AM ADJ.
R39
R43
C39
R44
R47
R53
C43
MP1
MP2
C31
C33
Q2
C38
Q7
C42
R50
C34
R34
R38
R45
L34
C40
R51
L36
C37
L33
MP2
C30
CR39
C36
CR32
R29
C29
C28
CR35
CR36
CR34
CR33
L30
R46
R11
C41
R52
CR29
CR30
Q3
Q6
C35
R48
U2
CR28
L23
R24
R25
L27
L24
R26
L9
L22
CR25
C7
CR26
CR21
CR22
CR19
CR20
L21
CR23
CR27
C24
R30
R31
Q10
L10
C9
C61
C16
L11
L18
R10
R20
C23
R12
S1
CR18
CR24
C25
K1
R35
R40
R41
R33
R30
R32
R31
CR37
CR38
C27
Q12
R36
R42
CR14
R16
CR4
U6
Q8
CR31
R4
R2
CR13
L17
L16
CR2
CR1
CR6
R22
C64
R27
R28
C22
CR12
C14
C13
L12
CR7
L8
CR9
R15
L15
CR8
C17
L14
C21
R12
U2
CR11
R9
C18
C12
L3
Q1
C11
R14
CR5
L6
U1
CR10
R7
L7
R13
L1
R3
C19
CR3
R5
C15
C4
L3
C6
L5
C5
L4
C20
A6

Figure 8-48. Output Section (A6 Assembly) Component Locations

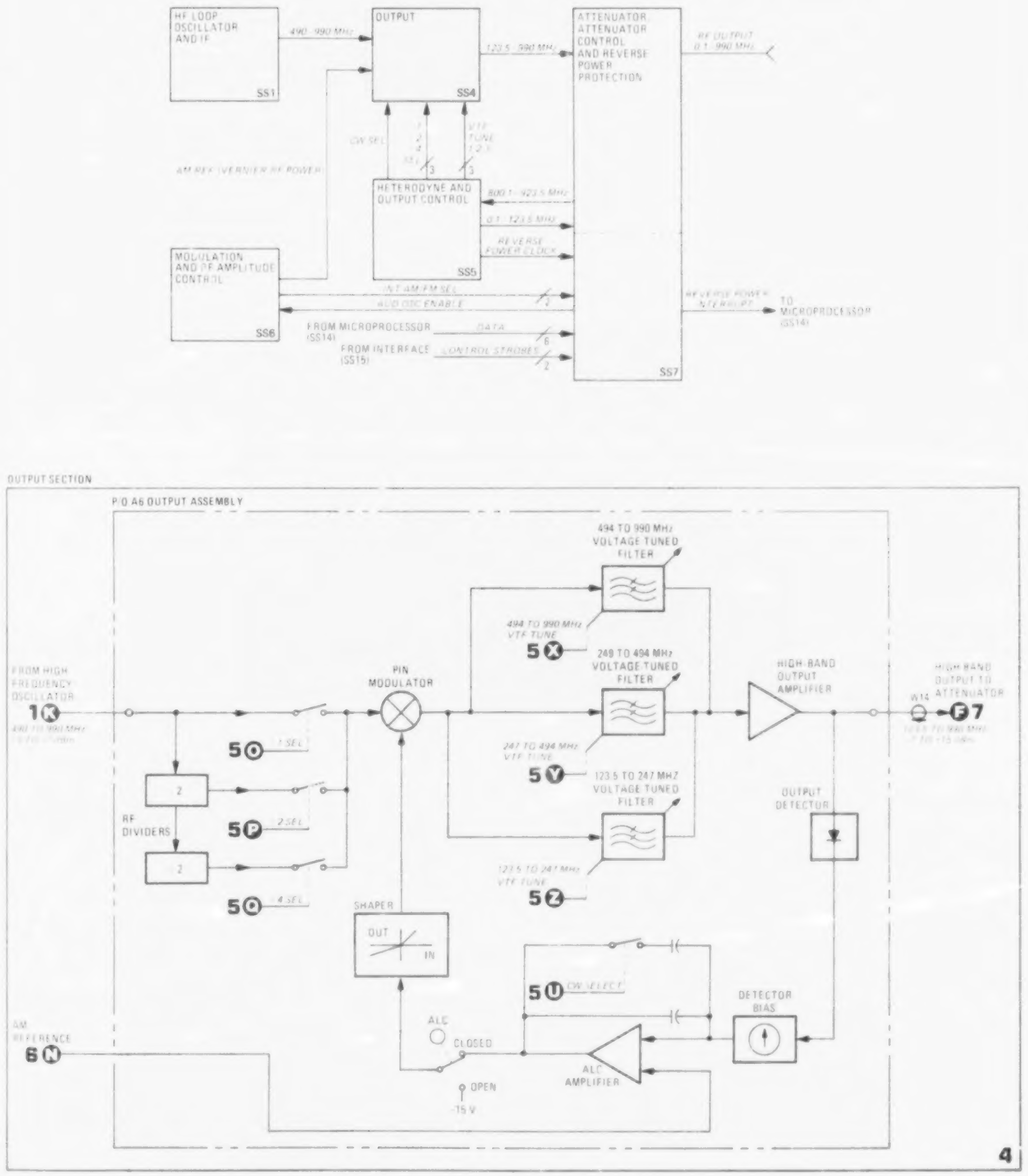
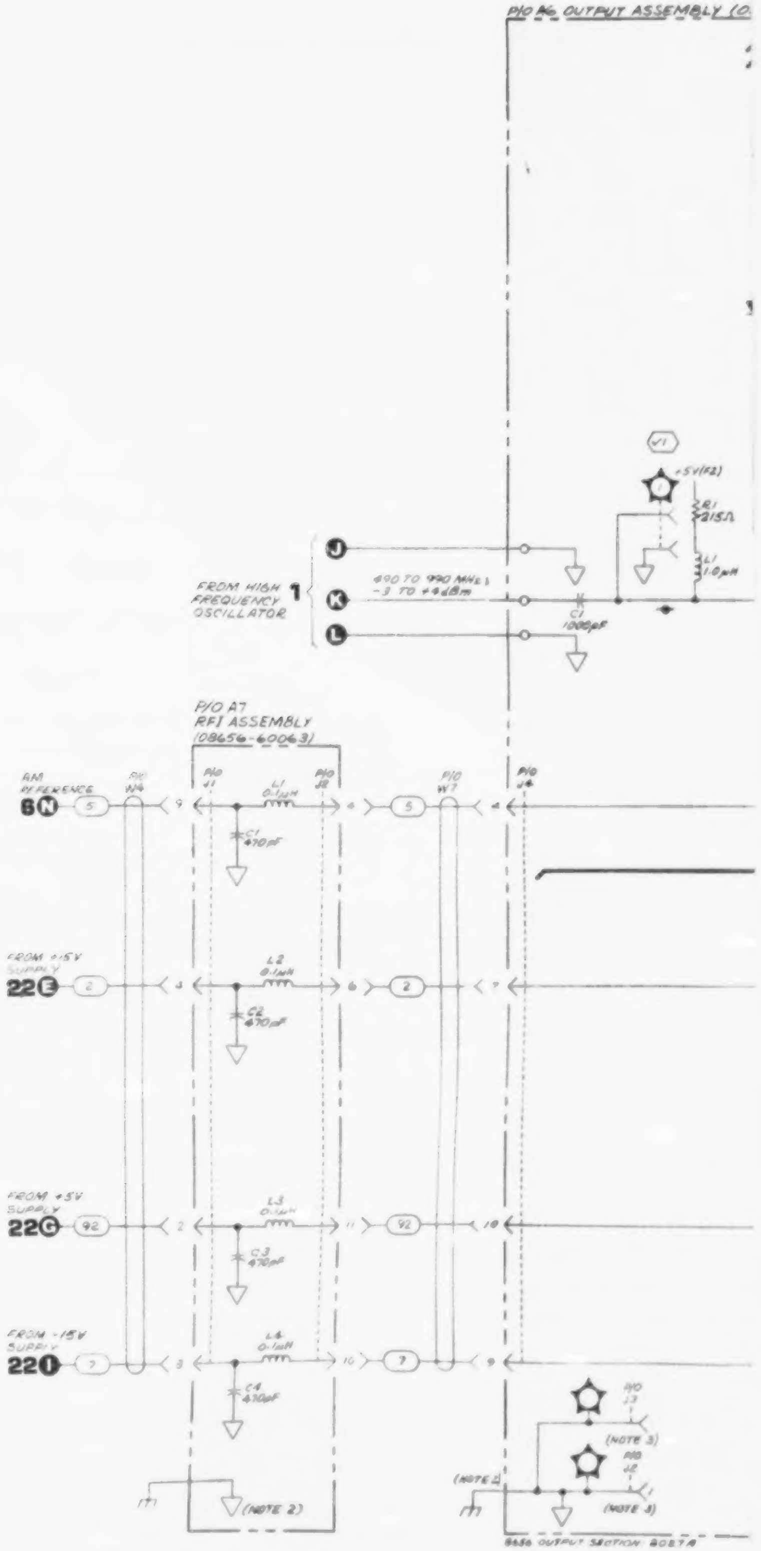
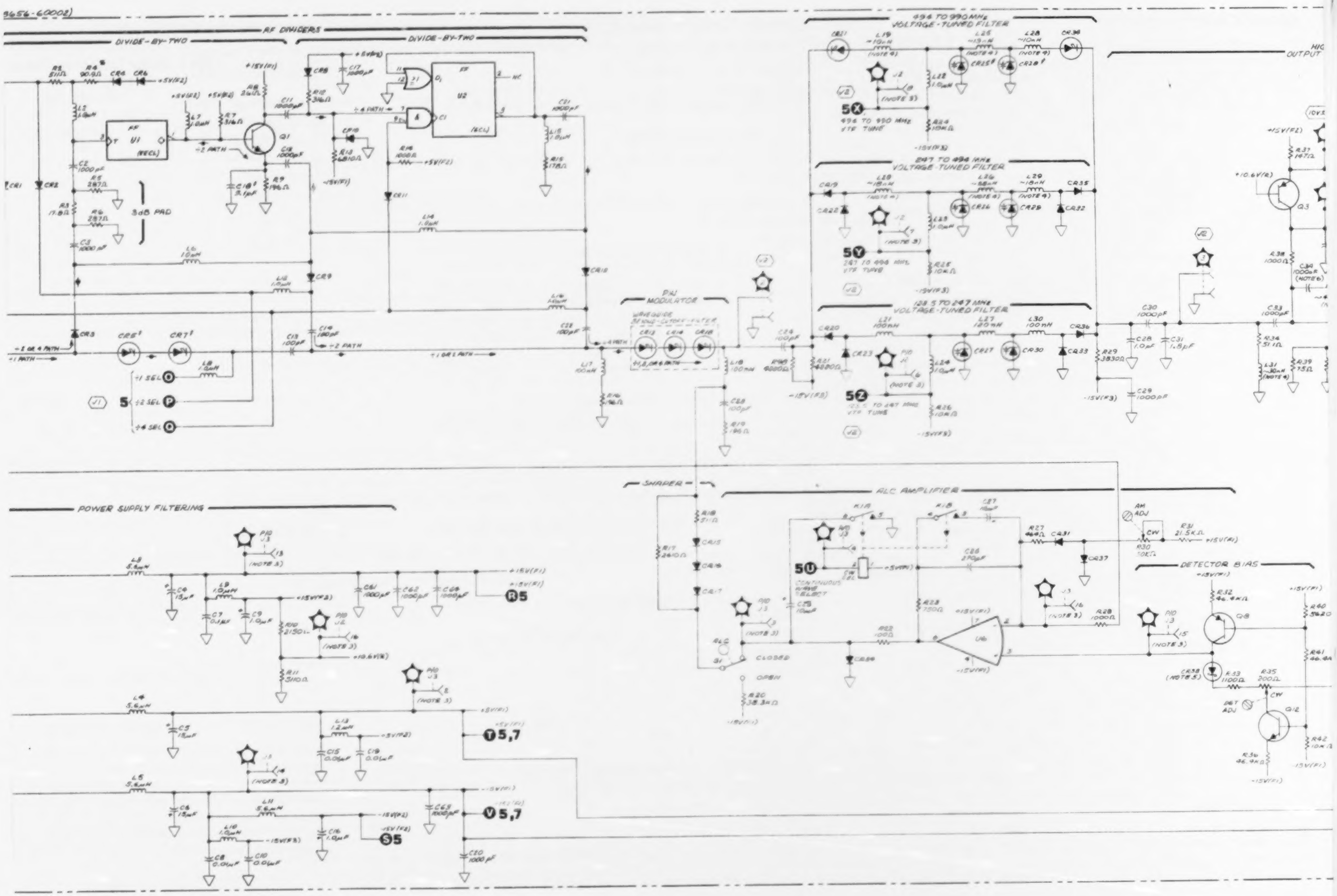
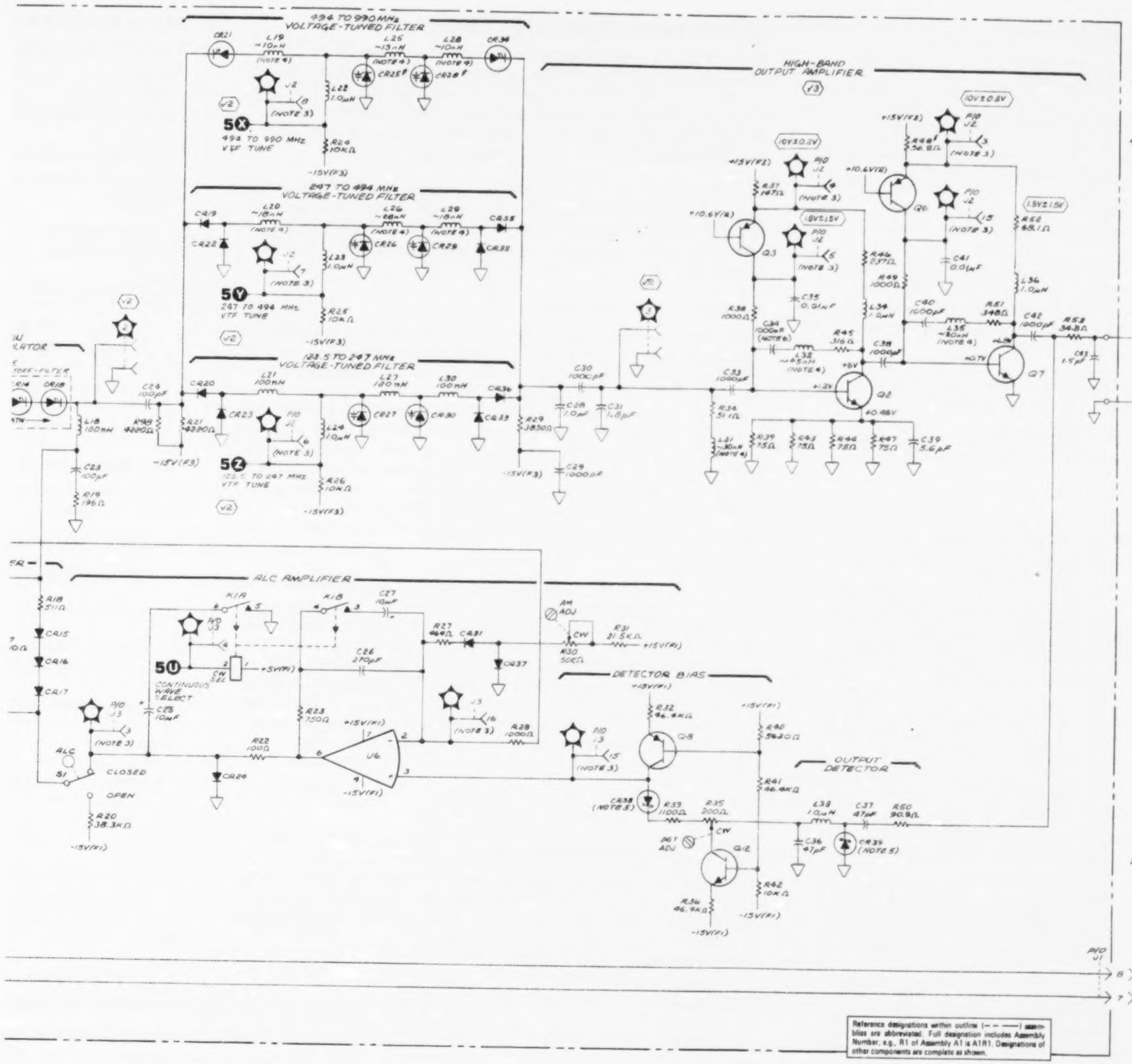

HF LOOP OSCILLATOR AND IF
SS1
490 - 990 MHz
OUTPUT
SS4
123.5 - 990 MHz
ATTENUATOR, ATTENUATOR CONTROL AND REVERSE POWER PROTECTION
RF OUTPUT 0.1 - 990 MHz
CW SEL
1 2 4 SEL
3
VTF TUNE 1 2 3
3
AM REF (VERNIER RF POWER)
HETERODYNE AND OUTPUT CONTROL
SS5
800.1 - 923.5 MHz
0.1 - 123.5 MHz
REVERSE POWER CLOCK
MODULATION AND RF AMPLITUDE CONTROL
SS6
INT AM/FM SEL
2
AUD OSC ENABLE
FROM MICROPROCESSOR (SS14)
DATA
6
FROM INTERFACE (SS15)
CONTROL STROBES
2
SS7
REVERSE POWER INTERRUPT
TO MICROPROCESSOR (SS14)
OUTPUT SECTION
P/O A6 OUTPUT ASSEMBLY
FROM HIGH FREQUENCY OSCILLATOR
1K
490 TO 990 MHz
5O
1 SEL
2
RF DIVIDERS
5P
2 SEL
2
5Q
4 SEL
PIN MODULATOR
494 TO 990 MHz VOLTAGE TUNED FILTER
494 TO 990 MHz VTF TUNE
5X
249 TO 494 MHz VOLTAGE TUNED FILTER
247 TO 494 MHz VTF TUNE
5Y
123.5 TO 247 MHZ VOLTAGE TUNED FILTER
123.5 TO 247 MHz VTF TUNE
5Z
HIGH-BAND OUTPUT AMPLIFIER
HIGH BAND OUTPUT TO ATTENUATOR
W14
F7
123.5 TO 990 MHz
OUTPUT DETECTOR
SHAPER
OUT
IN
5U
CW SELECT
DETECTOR BIAS
AM REFERENCE
6N
ALC
CLOSED
OPEN
-15 V
ALC AMPLIFIER
4

Figure 8-49. Output Section Block Diagrams


P/O A6 OUTPUT ASSEMBLY (0
V1
+5V(F2)
R1 215Ω
L1 1.0μH
J
FROM HIGH FREQUENCY OSCILLATOR 1
K
490 TO 990 MHz
-3 TO +4dBm
L
C1 1000pF
P/O A7 RFI ASSEMBLY (08656-60063)
AM REFERENCE
6N
5
P/O W4
P/O J1
L1 0.1μH
P/O J2
C1 470pF
P/O W7
P/O J4
FROM +15V SUPPLY
22E
2
L2 0.1μH
C2 470pF
FROM +5V SUPPLY
22G
92
L3 0.1μH
C3 470pF
FROM -15V SUPPLY
22I
7
L4 0.1μH
C4 470pF
(NOTE 2)
P/O J3
(NOTE 3)
P/O J2
(NOTE 3)
(NOTE 2)
8656 OUTPUT SECTION 8027A


3656-60002)
RF DIVIDERS
DIVIDE-BY-TWO
DIVIDE-BY-TWO
R2 511Ω
R4 90.9Ω
CR4
CR6
+5V(F2)
L2 1.0µH
FF U1 (ECL)
+5V(F2)
L7 1.0µH
R7 316Ω
+15V(F1)
R8 261Ω
Q1
÷2 PATH
C11 1000pF
C12 1000pF
C18 3.1pF
R9 196Ω
CR8
+5V(F2)
C17 1000pF
R12 316Ω
÷4 PATH
CR10
R13 6810Ω
-15V(F1)
R14 1000Ω
+5V(F2)
CR11
FF U2 (ECL)
NC
C21 1000pF
L15 1.0µH
R15 178Ω
CR1
CR2
C2 1000pF
R5 287Ω
R3 17.8Ω
R6 287Ω
3dB PAD
C3 1000pF
L6 1.0µH
L14 1.0µH
CR9
L12 1.0µH
CR12
L16 1.0µH
CR3
CR5
CR7
C13 100pF
C14 180pF
÷2 PATH
÷1 OR 2 PATH
C22 100pF
÷2 OR 4 PATH
÷1 PATH
L8 1.0µH
÷1 SEL
÷2 SEL
÷4 SEL
V1
5
O
P
Q
L17 100nH
R16 196Ω
PIN MODULATOR
WAVEGUIDE BELOW-CUTOFF-FILTER
CR13
CR14
CR18
÷1,2,OR 4 PATH
L18 100nH
C24 100pF
R40 5000Ω
R21 4220Ω
-15V(F3)
C23 100pF
R19 196Ω
494 TO 990 MHz VOLTAGE-TUNED FILTER
CR21
L19 ~10nH (NOTE 4)
L25 ~13nH (NOTE 4)
L28 ~10nH (NOTE 4)
CR34
CR25
CR28
L22 1.0µH
J2 8 (NOTE 3)
V2
5X
494 TO 990 MHz VTF TUNE
R24 10KΩ
-15V(F3)
247 TO 494 MHz VOLTAGE-TUNED FILTER
CR19
L20 ~18nH (NOTE 4)
L26 ~38nH (NOTE 4)
L29 ~18nH (NOTE 4)
CR35
CR22
CR26
CR29
CR32
L23 1.0µH
J2 7 (NOTE 3)
5Y
247 TO 494 MHz VTF TUNE
R25 10KΩ
-15V(F3)
128.5 TO 247 MHz VOLTAGE-TUNED FILTER
CR20
L21 100nH
L27 120nH
L30 100nH
CR36
CR23
CR27
CR30
CR33
P10 J2 6 (NOTE 3)
L24 1.0µH
5Z
128.5 TO 247 MHz VTF TUNE
R26 10KΩ
-15V(F3)
R29 3830Ω
C30 1000pF
C28 1.0pF
C31 1.8pF
C29 1000pF
-15V(F3)
HIG OUTPUT
+15V(F2)
R37 147Ω
+10.6V(R)
Q3
R38 1000Ω
C34 1000pF (NOTE 6)
C33 1000pF
R34 51.1Ω
L31 ~30nH (NOTE 4)
R39 75Ω
POWER SUPPLY FILTERING
L3 5.6µH
P10 J3 13 (NOTE 3)
C4 15µF
L9 1.0µH
+15V(F2)
C7 0.1µF
C9 1.0µF
R10 2150Ω
P10 J2 16 (NOTE 3)
+10.6V(R)
R11 5110Ω
C61 1000pF
C62 1000pF
C64 1000pF
+15V(F1)
+15V(F1)
R5
L4 5.6µH
C5 15µF
L13 1.2µH
+5V(F2)
C15 0.01µF
C19 0.01µF
P10 J3 2 (NOTE 3)
+5V(F1)
+5V(F1)
T 5,7
L5 5.6µH
J3 14 (NOTE 3)
C6 15µF
L11 5.6µH
-15V(F2)
L10 1.0µH
-15V(F3)
C8 0.01µF
C10 0.01µF
C16 1.0µF
-15V(F2)
S5
C63 1000pF
-15V(F1)
-15V(F1)
V 5,7
C20 1000pF
SHAPER
R18 511Ω
R17 2610Ω
CR15
CR16
CR17
ALC AMPLIFIER
K1A
K1B
C27 10µF
P10 J3 4
5U
CONTINUOUS WAVE SELECT
CW SEL
+5V(F1)
C26 270pF
C25 10µF
P10 J3 3 (NOTE 3)
ALC
S1
CLOSED
OPEN
R20 38.3KΩ
-15V(F1)
R22 100Ω
CR24
R23 750Ω
+15V(F1)
U6
-15V(F1)
R27 464Ω
CR31
CR37
J3 16 (NOTE 3)
R28 1000Ω
AM ADJ
CW
R30 50KΩ
R31 21.5KΩ
+15V(F1)
DETECTOR BIAS
+15V(F1)
R32 46.4KΩ
Q8
P10 J3 15 (NOTE 3)
CR38 (NOTE 5)
R33 1100Ω
R35 200Ω
CW
DET ADJ
Q12
R36 46.4KΩ
-15V(F1)
+15V(F1)
R40 5620
R41 46.4Ω
R42 10KΩ
-15V(F1)]


494 TO 990 MHz VOLTAGE-TUNED FILTER
247 TO 494 MHz VOLTAGE-TUNED FILTER
123.5 TO 247 MHz VOLTAGE-TUNED FILTER
HIGH-BAND OUTPUT AMPLIFIER
ALC AMPLIFIER
DETECTOR BIAS
OUTPUT DETECTOR
5X
494 TO 990 MHz VTF TUNE
5Y
247 TO 494 MHz VTF TUNE
5Z
123.5 TO 247 MHz VTF TUNE
5U
CONTINUOUS WAVE SELECT
AM ADJ
DET ADJ
ALC
S1
CLOSED
OPEN
U6
Q2
Q3
Q6
Q7
Q8
Q12
(NOTE 3)
(NOTE 4)
(NOTE 5)
-15V(F3)
+15V(F2)
+15V(F1)
-15V(F1)
+5V(F1)
123.5 TO 990 MHz; +8 TO +15dBm
HIGH-BAND OUTPUT TO ATTENUATOR
F7
TO HIGH FREQUENCY SECTION
B
C
1

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKET J2 OR J3.
4. PRINTED CIRCUIT TRACE INDUCTOR.
5. MATCHED FOR TEMPERATURE CHARACTERISTICS.
6. THIS COMPONENT IS MOUNTED ON EITHER 0, 1 OR 2 NON-INDUCTIVE BEADS PER LEAD (HP P/N 4330-0[illegible]) THEREBY SELECTING THE DESIRED LEAD INDUCTANCE. IF THE COMPONENT IS CHANGED, BE SURE TO INCLUDE THE SAME NUMBER OF BEADS WHEN MOUNTING THE NEW PART.

* INDICATES FACTORY SELECTED PART. TYPICAL VALUE IS SHOWN. REFER TO SECTION V FOR SELECTION PROCEDURE.

† INDICATES CIRCUIT CHANGE. SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A6 CONT
W4, 6, 7, 14	R1-53, 98 S1 TP1-3 U1, 2, 6
A6	A7
C1-31, 33-43 61-64 CR1-39 J1-4 K1 L1-36 Q1-3, 6-8, 12	C1-4 J1, 2 L1-4

LOGIC LEVELS

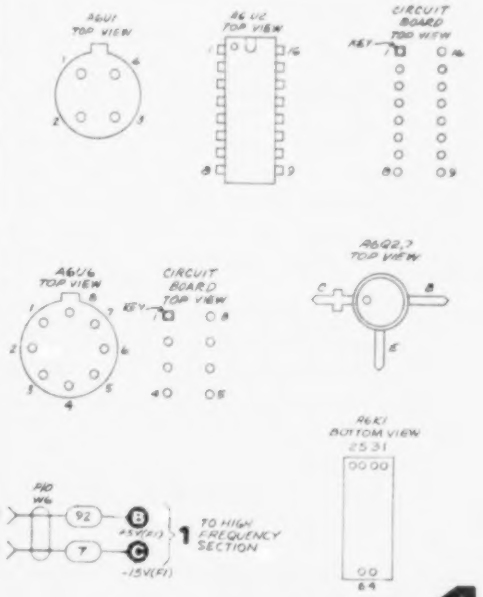
	TTL	ECL	EECL
HIGH	>2V	>+4.2V	>+5.1V
LOW	<0.8V	<+3.3V	<+4.74
< IS MORE NEG. THAN > IS MORE POS. THAN			
OPEN	HIGH	LOW	LOW
GROUND	LOW	HIGH	HIGH

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1854-0696
Q2	1854-0632
Q3, 6, 8	1853-0007
Q7	1854-0720
Q12	1854-0071
U1	1820-1811
U2	1820-2106
U6	1826-0488

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V(F2) - 4 ▽ - 2 (CASE)
U2	+5V(F2) - 1, 16 ▽ - 4-6, 8, 10, 13-15


A6U1 TOP VIEW
A6 U2 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY
A6U6 TOP VIEW
CIRCUIT BOARD TOP VIEW
A6Q2,7 TOP VIEW
A6K1 BOTTOM VIEW

4

P/O A6, P/O A7

Figure 8-50. Output Section Schematic Diagram

SERVICE SHEET 5
P/O A6 OUTPUT ASSEMBLY
P/O A7 RFI ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD2
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

When the RF OUTPUT frequency is between 0.1 and 123.5 MHz, the Divide-by-1/Heterodyne mode is selected. The High Frequency Loop's oscillator frequency, in this case between 800.1 and 923.5 MHz, is mixed with the 800 MHz reference signal. The difference frequencies from the Mixer are those that fall within the required RF output frequency band.

The VTF TUNE input is translated by the VTF Drivers to voltages that will tune each of the three VTF filters. The filter selected determines the RF divider mode.

Serial Output Data is clocked into the Band Select Shift Register and on to the register found among the circuits shown on Service Sheet 2. The output of U7 enables the appropriate VTF and the cw mode of operation.

Heterodyne Section

A Frequency input between 0.1 and 123.5 MHz selects the Divide-by-1/Heterodyne mode. The RF signal from the Output Assembly to the A9 Attenuator Assembly (between 800.1 and 923.5 MHz) is switched to the Output Assembly. Switching occurs at front panel frequencies of 123.5999 MHz when incrementing up and 123.4000 MHz when incrementing down. After mixing with the 800 MHz reference, the Diplexed Filter passes the difference frequencies while attenuating the other mixing products. The 0.1 to 123.5 MHz signal is applied to the step attenuator in the A9 Assembly before being coupled to the front panel RF OUTPUT connector.

A frequency from 800.1 MHz to 923.5 MHz at a level from +15 to −7 dBm, vernier dependent, is switched to the Output Assembly and applied to the Mixer A6U10 through an adjustable pad. The pad, consisting of resistors R55, R56, R57, R58 and C56, is adjustable from 20 to 24 dB. The pad reduces the signal into the mixer to a maximum of −7 dBm which prevents spurious signal generation. The LO input to the Mixer is a fixed frequency of 800 MHz at +6 dBm. The 800 MHz enters the Output Assembly through an 800 MHz Bandpass Filter where it is coupled to the Mixer. The difference output frequencies (0.1 to 123.5 MHz) are passed by the Diplexed Filter to the Low Band Output Amplifier. The input of the filter is diplexed by C57 and R59 to give a good match at all frequencies and to reduce spurious signals, primarily the summed mixing product. The output of the filter is ac coupled to the Low Band Output Amplifier by capacitor C52. The value of C52 provides the best signal coupling while preventing amplifier transistors Q14 and Q15 from being reverse biased when the instrument is turned on.

Resistors R64, R62, and R60 form a voltage divider used to dc bias Q14. The voltage divider also contains RF choke L50. Resistors R67, R70, and R72 in the emitter of Q14 provide series feedback. By using these three resistors, the inductance in the emitter current path is reduced. Resistor R68 completes the emitter's dc return and capacitor C55 is the ac path to ground.

SERVICE SHEET 5 (Cont'd)

The output of Q14 is dc coupled to the base of Q15. Resistors R69 and R84 provide dc voltage for the collector of Q15. Inductors L52 and L53 are RF chokes. The emitter circuit components R77, R78, R81, R82, and C47 have the same function as those components of Q14. Resistor R85 and capacitor C49 are a low Q series resonant circuit used to increase the gain of Q15 at the higher frequencies.

The output of Q15 is ac coupled to the Attenuator Assembly by capacitor C59. The 383Ω resistor, R65, lowers the Q of the Diplexed Filter. The Low Band Output Amplifier provides 30 dB of gain ±0.5 dB to restore the RF signal to the same level as input but at the lower frequency.

VTF Drivers and Band Select

The VTF TUNE voltage from the A4 Assembly's Loop Amplifier is applied through voltage divider R71 and R73 to the negative input of U3. This variable tune voltage, −7.5 to +12 volts, is dependent on the frequency selected. The resistors, which act as a voltage divider, offset the input voltage. Operational amplifier U3, transistor Q5 and their associated components, further offset the input voltage. The resulting VTF TUNE voltages vary between +3 and +15 volts. The voltage at the negative input of U3 (the collector voltage of Q5 divided by resistors R75 and R76) is compared to the positive input of U3. Transistor Q5 is a power amplifier that increases the current capability, providing enough current to turn on the input and output diodes of the VTF selected.

Resistors R90 and R91, R86 and R87, and R79 and R80 provide dc bias for transistors Q9, Q10 and Q11 respectively. Transistors Q9, Q10, and Q11 are biased on by bits 5,6, and 7 of High Frequency Word 2. This control signal is received from the Microprocessor by the Band Select Shift Register and Drivers. When the fifth, sixth or seventh bit of the frequency word selects 0 Vdc, diodes CR42, CR41, or CR40 will be forward biased. This turns on transistor Q9, Q10, or Q11, selects the VTF and supplies the tune voltage. These three bits also select one of the three Voltage Tuned Filters on Service Sheet 4, thereby determining the RF Divider mode.

TROUBLESHOOTING

Procedures for checking the circuits of the A6 Output Assembly are given below. The area or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g. ⟨√3⟩. Fixed voltages are shown on the schematic inside a hexagon, e.g. ⟨2V ±0.2V⟩. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Oscilloscope	HP 1222A
Power Meter	HP 436A
Power Sensor	HP 8482A
Frequency Counter	HP 5328A
Adapter Probe	HP 1250-1598

SERVICE SHEET 5 (Cont'd)

Test Equipment (Cont'd)

Adapter, Type N male to BNC female	HP 1250-0780
Cable, BNC (male) to SMC (female)	HP 08662-60080

⟨√1⟩ Heterodyne Section

1. Set the Signal Generator to −10 dBm at 100 MHz without modulation.

2. Measure power level and frequency as shown in Table 1 using the adapter probe.

Table 1. Heterodyne Section Power Levels

Test Point	Power Level (dBm)	Frequency (MHz)
W10	+6.5 to +3.5	800.00
W13	−2.5 to −4.5	900.00
C59	−3.0 to −4.0	100.00

⟨√2⟩ Output Section Data Storage/Driver

1. Set the Signal Generator to −10 dBm at 500 MHz without modulation (cw mode).

2. Check CW SEL at J3-pin 4. It should be +0.2 Vdc (low).

3. Set the Signal Generator to 50% AM at the internal 1 kHz rate.

4. Check CW SEL at J3-pin 4. It should be +5.0 Vdc (high).

5. Check voltages on the J3 test points at the front panel Frequency settings as indicated in Table 2

Table 2. Band Select Shift Register and Driver Voltages

Front Panel Frequency (MHz)	Voltage Measured at J3 (Vdc)		
	÷1 SEL at Pin 8	÷2 SEL at Pin 5	÷4 SEL at Pin 7
500	+0.2	+4.8	+4.8
300	+8.4	+0.2	+8.4
200	+14.0	+14.0	+0.2

6. Check J3-Pin 12. It should measure less than or equal to +0.2 Vdc with the Signal Generator set to ON and +15.0 Vdc in the STBY mode.

⟨√3⟩ VTF Drivers

1. Set the Signal Generator to −10 dBm without modulation.

2. Check the voltages shown in Table 3 for the front panel frequency indicated. If the High Frequency Loop is not locked the voltage will be a triangular wave.

SERVICE SHEET 5 (Cont'd)

Table 3. Voltage Tuned Filter TUNE Voltages

Front Panel Frequency (MHz)	VTF TUNE (Vdc)			J2-Pin 13 (Vdc)
	123.5 to 247 MHz	247 to 494 MHz	494 to 990 MHz	
900	–0.5	–0.5	+14.3	+14.4
600	–0.5	–0.5	+ 8.5	+ 8.6
494	–0.5	–0.5	+ 4.9	+ 5.0
350	–0.5	+12.9	–0.5	+13.0
300	–0.5	+ 8.5	–0.5	+ 8.6
200	+14.3	–0.5	–0.5	+14.4
150	+ 8.6	–0.5	–0.5	+ 8.6

3. Remove the tune voltage to the A5 Assembly. The loop is unlocked. The waveforms shown in Figure 1 should occur on the stated connector and pin.

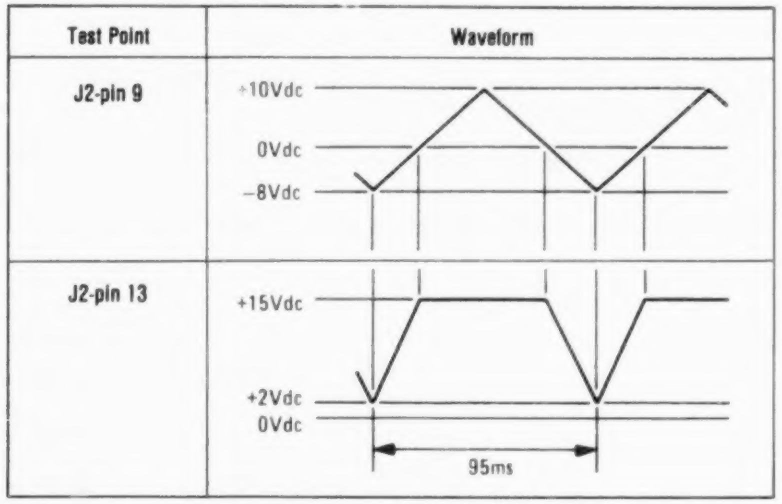


Figure 1. Waveforms with HF Loop Unlocked

TROUBLESHOOTING USING SIGNATURE ANALYSIS

This is an alternate method of troubleshooting the Service Sheet 5 (and Service Sheet 2) circuits. If the signatures for these circuits are correct, the problem may be in the controlled (analog) circuits. In this case, continue with the preceding troubleshooting information. Remember that a malfunction could be on the control (digital) circuits of Service Sheet 2. If the problem is definitely in the Output or High Frequency Loop circuits, you may wish to refer to BD2.

NOTE

The signatures are not valid for Signal Generators with serial number prefixes of 2018A and below.

SERVICE SHEET 5 (Cont'd)

Purpose. Verify correct data transfer from the Microprocessor to the Output Assembly.

Setup. Connect the signature analyzer as follows:

1) GND to GND A11TP2
2) CLK to SA4 A11TP7
3) START to SA5 A11TP9
4) STOP to SA5 A11TP9

Set the signature analyzer controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Generator as follows:

1) On the A6 Output Assembly board, short TP5 and TP6 to TP4 (ground).
2) Set the LOGIC/RAM switch P/O A11S1 to LOGIC.

Initialize. Briefly short A11TP3 NMI to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

Probe. Connect the probe to the node indicated in Table 4. Verify that the signature at each node is correct and stable.

Table 4. Band Select Shift Register Signatures

Node	Correct Signature	Comments
+5V	F84P	
*U7#3	F84P	SIPO CLK
U7#2	6UPP	DATA IN
U7#4/U4#2	P9C5	÷4 BND
U7#5/U4#4	74HA	÷2 BND
U7#6/U4#6	3A6H	÷1 BND
U7#7/U4#15	9H36	CW BIT
U7#14/U4#12	029U	RF OFF

*This signature is the same as the +5V signature but the signature analyzer's probe should blink.

Remove the jumpers between ground, TP5 and TP6. Reset the LOGIC/RAM switch to the RAM position. Set the front panel RESET-STBY-ON switch to STBY and back to ON.

P/O A7 ASSEMBLY

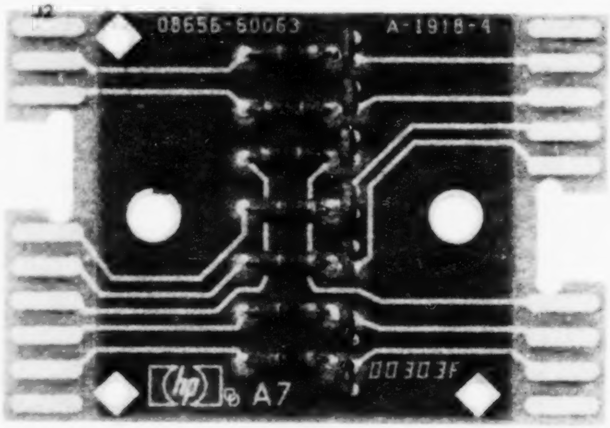

J2
08656-60063
A-1918-4
A7
00303F

Figure 8-51. Heterodyne and Output Control (A7 Assembly) Component Locations

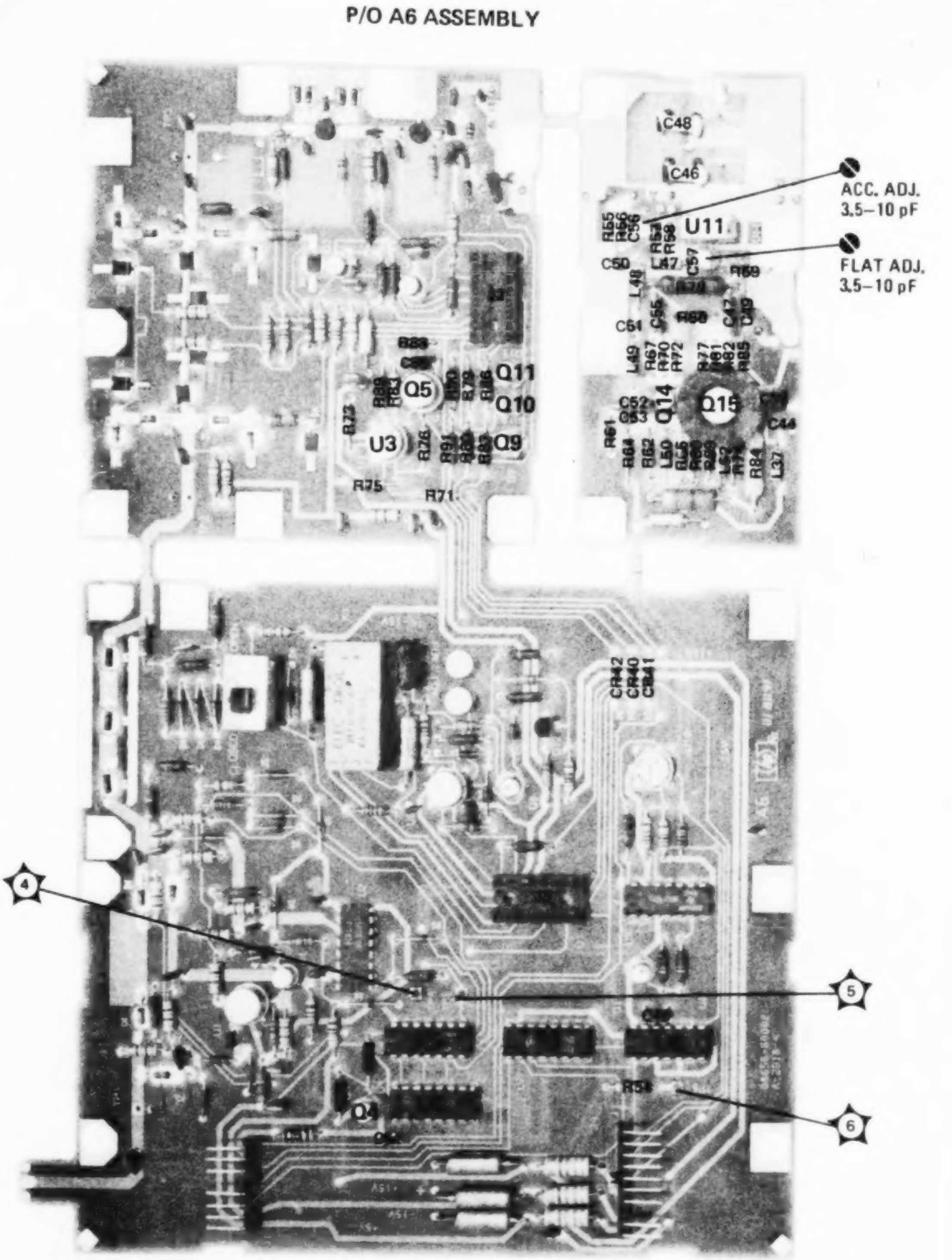

P/O A6 ASSEMBLY
C48
C46
ACC. ADJ.
3.5–10 pF
R55
R56
C56
U11
R53
R58
FLAT ADJ.
3.5–10 pF
C50
L47
C57
R69
L48
C61
C55
R68
C47
C49
L49
R67
R70
R72
R77
R81
R82
R85
R88
Q11
Q5
Q10
R79
R86
R73
U3
R76
Q9
R75
R71
C52
C53
Q14
Q15
C44
R61
R64
R62
L50
R84
L37
CR42
CR40
CR41
4
5
6
R54
Q4

Figure 8-52. Heterodyne and Output Control (A6 Assembly) Component Locations

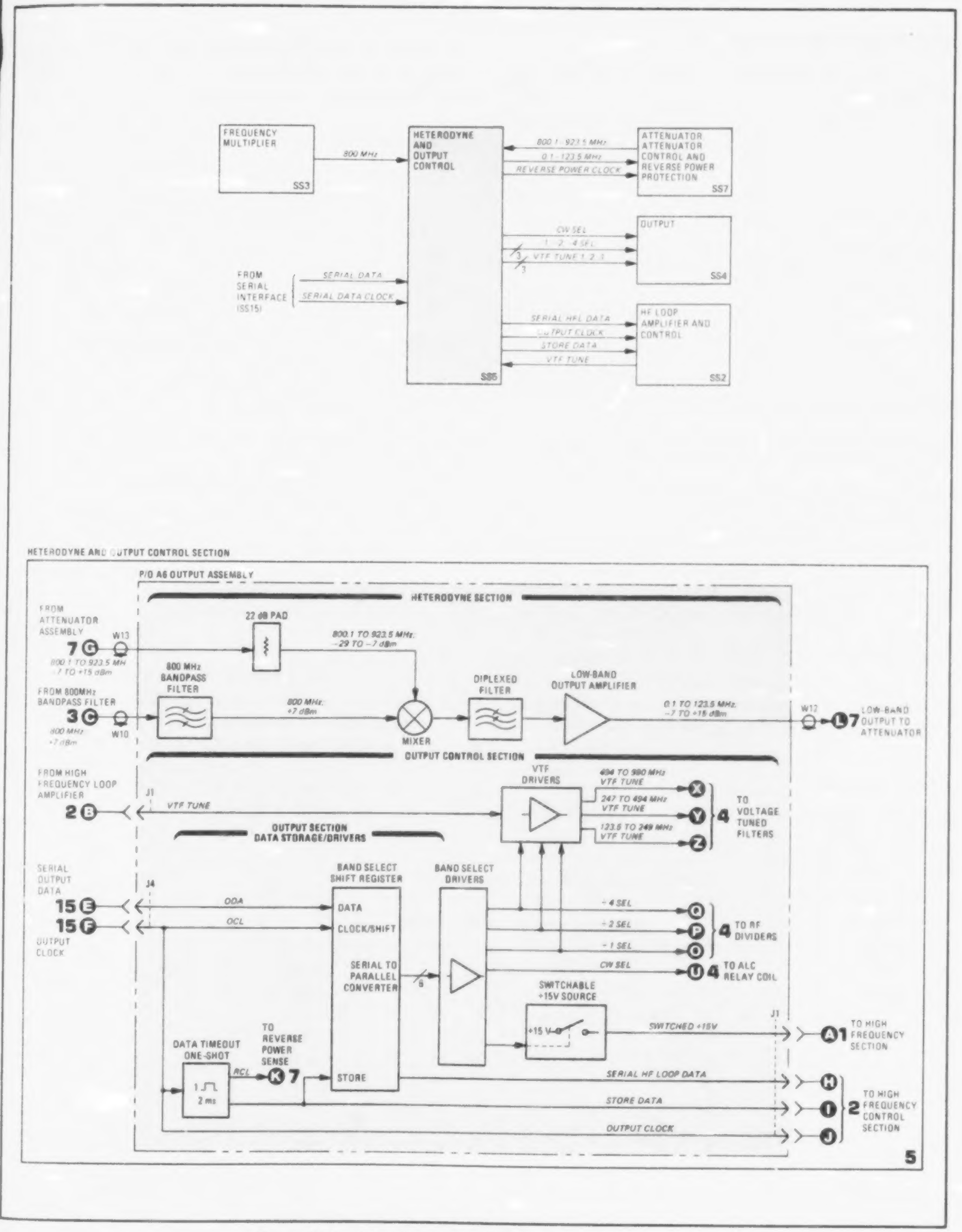
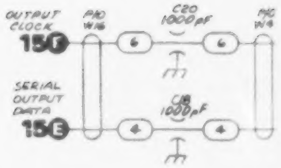
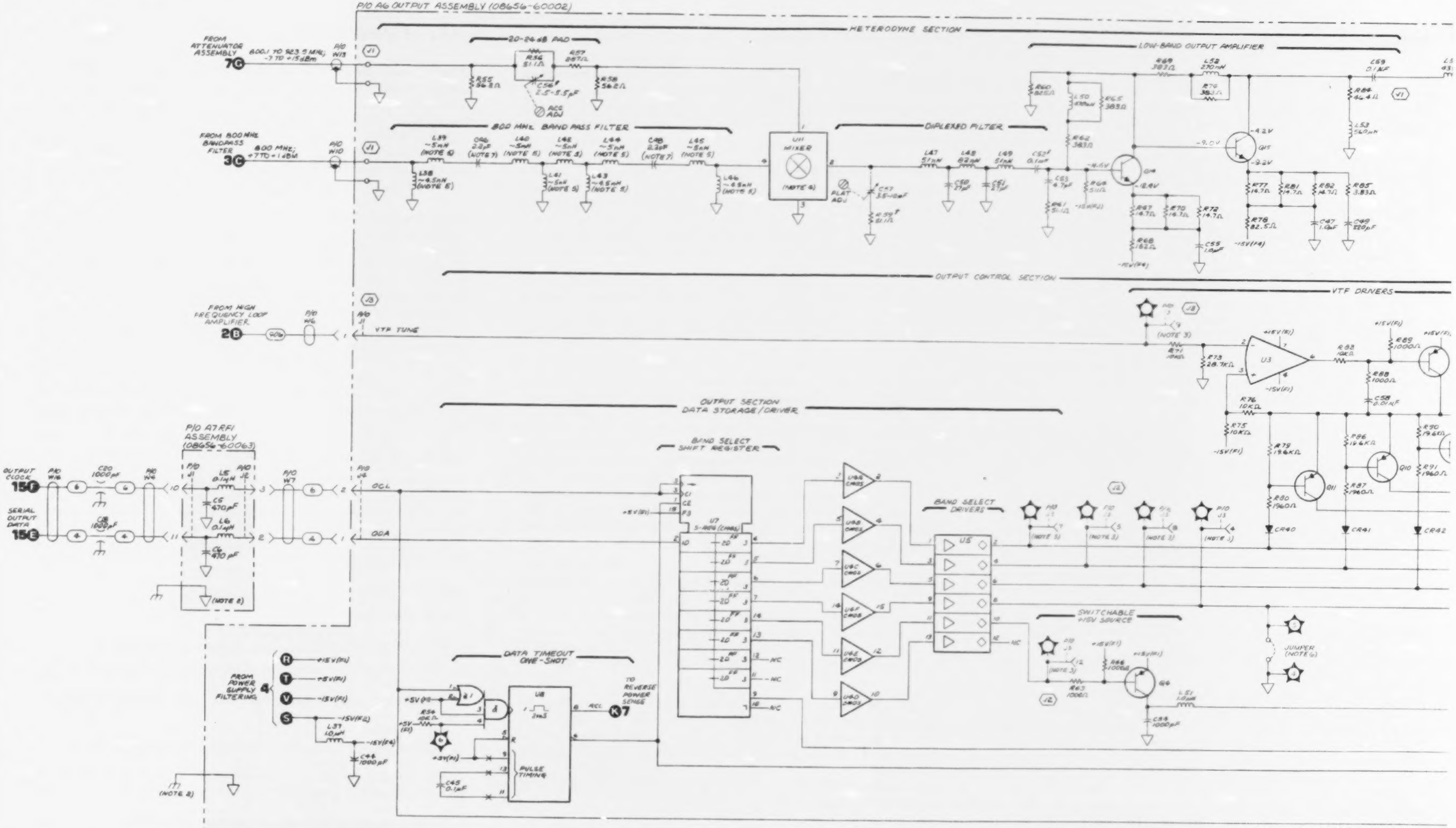
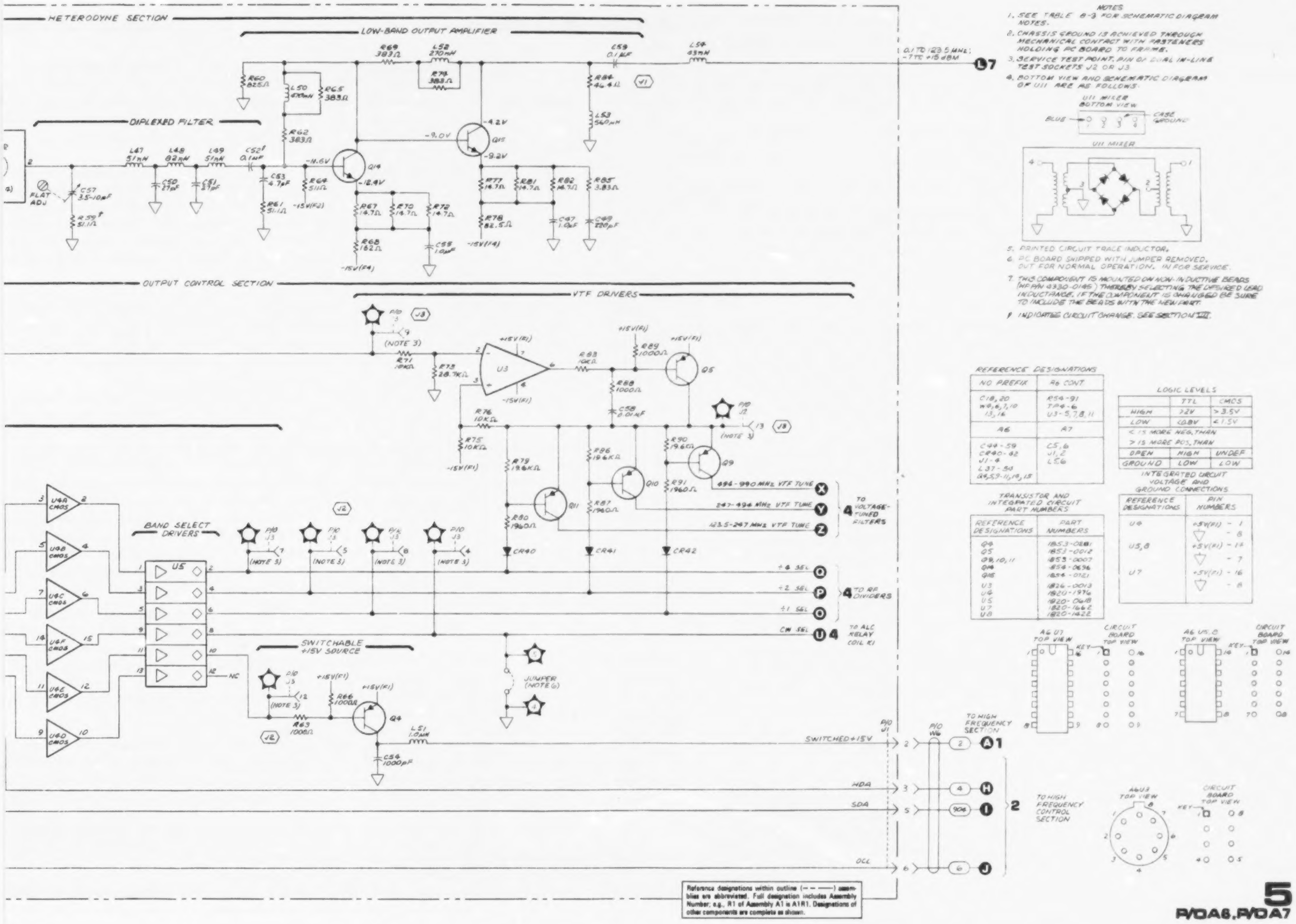

FREQUENCY MULTIPLIER
SS3
800 MHz
HETERODYNE AND OUTPUT CONTROL
SS5
800.1 - 923.5 MHz
0.1 - 123.5 MHz
REVERSE POWER CLOCK
ATTENUATOR ATTENUATOR CONTROL AND REVERSE POWER PROTECTION
SS7
CW SEL
1 - 2 - 4 SEL
3
VTF TUNE 1, 2, 3
3
OUTPUT
SS4
FROM SERIAL INTERFACE (SS15)
SERIAL DATA
SERIAL DATA CLOCK
SERIAL HFL DATA
OUTPUT CLOCK
STORE DATA
VTF TUNE
HF LOOP AMPLIFIER AND CONTROL
SS2
HETERODYNE AND OUTPUT CONTROL SECTION
P/O A6 OUTPUT ASSEMBLY
HETERODYNE SECTION
FROM ATTENUATOR ASSEMBLY
W13
7 G
800.1 TO 923.5 MH
-7 TO +15 dBm
22 dB PAD
800.1 TO 923.5 MHz:
-29 TO -7 dBm
800 MHz BANDPASS FILTER
FROM 800MHz BANDPASS FILTER
3 C
800 MHz
+7 dBm
W10
800 MHz:
+7 dBm
MIXER
DIPLEXED FILTER
LOW-BAND OUTPUT AMPLIFIER
0.1 TO 123.5 MHz:
-7 TO +15 dBm
W12
L 7
LOW-BAND OUTPUT TO ATTENUATOR
OUTPUT CONTROL SECTION
FROM HIGH FREQUENCY LOOP AMPLIFIER
2 B
J1
VTF TUNE
VTF DRIVERS
494 TO 980 MHz VTF TUNE
247 TO 494 MHz VTF TUNE
123.5 TO 249 MHz VTF TUNE
X
Y
Z
4
TO VOLTAGE TUNED FILTERS
OUTPUT SECTION DATA STORAGE/DRIVERS
SERIAL OUTPUT DATA
J4
15 E
15 F
OUTPUT CLOCK
ODA
OCL
BAND SELECT SHIFT REGISTER
DATA
CLOCK/SHIFT
SERIAL TO PARALLEL CONVERTER
STORE
6
BAND SELECT DRIVERS
÷ 4 SEL
÷ 2 SEL
÷ 1 SEL
Q
P
O
4
TO RF DIVIDERS
CW SEL
U 4
TO ALC RELAY COIL
SWITCHABLE +15V SOURCE
+15 V
SWITCHED +15V
J1
A 1
TO HIGH FREQUENCY SECTION
DATA TIMEOUT ONE-SHOT
1
2 ms
RCL
TO REVERSE POWER SENSE
K 7
SERIAL HF LOOP DATA
STORE DATA
OUTPUT CLOCK
H
I
J
2
TO HIGH FREQUENCY CONTROL SECTION
5

Figure 8-53. Heterodyne and Output Control Block Diagrams


OUTPUT CLOCK
15 F
P/O W16
C20 1000pF
6
6
P/O W4
SERIAL OUTPUT DATA
15 E
C18 1000pF
4
4


P/O A6 OUTPUT ASSEMBLY (08656-60002)
HETERODYNE SECTION
20-24 dB PAD
FROM ATTENUATOR ASSEMBLY
800.1 TO 923.5 MHz; -7 TO +15 dBm
7G
P/O W13
J1
R55 56.2Ω
R56 51.1Ω
R57 287Ω
R58 56.2Ω
C56 2.5-5.5pF
ACC ADJ
800 MHz BAND PASS FILTER
FROM 800 MHz BANDPASS FILTER
800 MHz; +7 TO +1 dBM
3C
P/O W10
L39 ~5nH (NOTE 5)
C46 2.2pF (NOTE 7)
L40 ~5nH (NOTE 5)
L42 ~5nH (NOTE 5)
L44 ~5nH (NOTE 5)
C48 2.2pF (NOTE 7)
L45 ~5nH (NOTE 5)
L38 ~4.5nH (NOTE 5)
L41 ~5nH (NOTE 5)
L43 ~4.5nH (NOTE 5)
L46 ~6.5nH (NOTE 5)
U11 MIXER (NOTE 4)
DIPLEXED FILTER
FLAT ADJ
L47 51nH
L48 82nH
L49 51nH
C47 3.5-10pF
C50 27pF
C51 27pF
C52 0.1μF
C53 4.7pF
R59 51.1Ω
R61 51.1Ω
LOW-BAND OUTPUT AMPLIFIER
R60 825Ω
L50 470nH
R65 383Ω
R62 383Ω
R69 383Ω
L52 270nH
R74 383Ω
C59 0.1μF
R84 46.4Ω
L53 560nH
Q14
Q15
R67 14.7Ω
R70 14.7Ω
R72 14.7Ω
R68 162Ω
C55 1.0μF
R77 14.7Ω
R81 14.7Ω
R82 14.7Ω
R85 3.83Ω
R78 82.5Ω
C47 1.0μF
C49 220pF
-15V(F4)
OUTPUT CONTROL SECTION
VTF DRIVERS
FROM HIGH FREQUENCY LOOP AMPLIFIER
2B
P/O W6
P/O J1
J3
VTF TUNE
(NOTE 3)
R71 10KΩ
R73 28.7KΩ
U3
+15V(F1)
-15V(F1)
R83 10KΩ
R89 1000Ω
R88 1000Ω
C58 0.01μF
R76 10KΩ
R75 10KΩ
R79 19.6KΩ
R80 1960Ω
Q11
R86 19.6KΩ
R87 1960Ω
Q10
R90 19.6KΩ
R91 1960Ω
CR40
CR41
CR42
OUTPUT SECTION DATA STORAGE/DRIVER
P/O A7 RFI ASSEMBLY (08656-60063)
OUTPUT CLOCK
15F
SERIAL OUTPUT DATA
15E
P/O W16
C80 1000pF
C8 1000pF
P/O W4
L5 0.1μH
C5 470pF
L6 0.1μH
C6 470pF
(NOTE 8)
P/O W7
OCL
ODA
BAND SELECT SHIFT REGISTER
U7 S-REG (CMOS)
+5V(F1)
N/C
U6B CMOS
U6A CMOS
U6C CMOS
U6F CMOS
U6E CMOS
U6D CMOS
BAND SELECT DRIVERS
U5
SWITCHABLE +15V SOURCE
R66 1000Ω
R63 1000Ω
Q4
L51 1.0μH
C54 1000pF
JUMPER (NOTE 6)
DATA TIMEOUT ONE-SHOT
U8
PULSE TIMING
R54 10KΩ
C45 0.1μF
TO REVERSE POWER SENSE
RCL
K7
FROM POWER SUPPLY FILTERING
4
R +15V(F1)
T +5V(F1)
V -15V(F1)
S -15V(F2)
L37 1.0μH
C44 1000pF
-15V(F4)
(NOTE 8)

8656A HETERODYNE AND OUTPUT CONTROL SECTIONS: 2035A


HETERODYNE SECTION
LOW-BAND OUTPUT AMPLIFIER
DIPLEXED FILTER
FLAT ADJ
C57 3.5-10pF
R59 51.1Ω
L47 51nH
L48 82nH
L49 51nH
C52 0.1µF
C50 27pF
C51 27pF
C53 4.7pF
R61 51.1Ω
R64 511Ω
-15V(F2)
R60 825Ω
L50 470nH
R65 383Ω
R62 383Ω
-11.6V
Q14
-12.4V
R67 14.7Ω
R70 14.7Ω
R72 14.7Ω
R68 162Ω
-15V(F4)
C55 1.0µF
R69 383Ω
L52 270nH
R79 383Ω
-9.0V
Q15
-4.2V
-9.2V
R77 14.7Ω
R81 14.7Ω
R82 14.7Ω
R85 3.83Ω
R78 82.5Ω
C47 1.0µF
C49 220pF
C59 0.1µF
R84 46.4Ω
V1
L53 560nH
L54 43nH
0.1 TO 123.5 MHz; -7 TO +15 dBM
L7
OUTPUT CONTROL SECTION
VTF DRIVERS
P/O J3
J8
(NOTE 3)
R71 10KΩ
R73 28.7KΩ
+15V(F1)
U3
-15V(F1)
R83 10KΩ
R89 1000Ω
Q5
R88 1000Ω
C58 0.01µF
P/O J2
13
R76 10KΩ
R75 10KΩ
R79 19.6KΩ
R86 19.6KΩ
R90 19.6KΩ
Q11
Q10
Q9
R80 1960Ω
R87 1960Ω
R91 1960Ω
494-990 MHz VTF TUNE
247-494 MHz VTF TUNE
123.5-247 MHz VTF TUNE
X
Y
Z
4 TO VOLTAGE-TUNED FILTERS
CR40
CR41
CR42
÷4 SEL
÷2 SEL
÷1 SEL
Q
P
O
4 TO RF DIVIDERS
CW SEL
U 4
TO ALC RELAY COIL K1
U4A CMOS
U4B CMOS
U4C CMOS
U4F CMOS
U4E CMOS
U4D CMOS
BAND SELECT DRIVERS
U5
NC
J2
SWITCHABLE +15V SOURCE
R66 1000Ω
R63 1000Ω
Q4
L51 1.0mH
C54 1000pF
JUMPER (NOTE 6)
SWITCHED+15V
HDA
SDA
OCL
P/O J1
P/O W6
TO HIGH FREQUENCY SECTION
A1
H
I
J
2
TO HIGH FREQUENCY CONTROL SECTION
U11 MIXER BOTTOM VIEW
BLUE
CASE GROUND
U11 MIXER
A6 U7 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY
A6 U5,8 TOP VIEW
A6 U3 TOP VIEW

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKETS J2 OR J3
4. BOTTOM VIEW AND SCHEMATIC DIAGRAM OF U11 ARE AS FOLLOWS.
5. PRINTED CIRCUIT TRACE INDUCTOR.
6. PC BOARD SHIPPED WITH JUMPER REMOVED. OUT FOR NORMAL OPERATION. IN FOR SERVICE.
7. THIS COMPONENT IS MOUNTED ON NON-INDUCTIVE BEADS (HP P/N 4330-0145) THEREBY SELECTING THE DESIRED LEAD INDUCTANCE. IF THE COMPONENT IS CHANGED BE SURE TO INCLUDE THE BEADS WITH THE NEW PART.

† INDICATES CIRCUIT CHANGE. SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A6 CONT
C18, 20 W4, 6, 7, 10 13, 16	R54-91 TP4-6 U3-5, 7, 8, 11
A6	A7
C44-59 CR40-42 J1-4 L37-54 Q4, 5, 9-11, 14, 15	C5, 6 J1, 2 L56

LOGIC LEVELS

	TTL	CMOS
HIGH	>2V	>3.5V
LOW	<0.8V	<1.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	UNDEF
GROUND	LOW	LOW

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q4	1853-0281
Q5	1853-0012
Q9, 10, 11	1853-0007
Q14	1854-0696
Q15	1854-0121
U3	1826-0013
U4	1820-1976
U5	1820-0618
U7	1820-1662
U8	1820-1422

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U4	+5V(F1) - 1 ▽ - 8
U5, 8	+5V(F1) - 14 ▽ - 7
U7	+5V(F1) - 16 ▽ - 8

5
P/O A6, P/O A7

Figure 8-54. Heterodyne and Output Control Schematic Diagram

SERVICE SHEET 6 (Cont'd)

⟨√3⟩ P/O Modulation Control Latches, FM Deviation DAC

1. Set the Signal Generator to −10 dBm at 500 MHz with a 1 kHz source in FM mode.

2. Set FM kHz as indicated in Table 5 and make the indicated voltage checks.

⟨√4⟩ P/O Modulation Control Latches, Comparators, and FET switches

1. Set the Signal Generator to −10 dBm at 500 MHz without modulation.

2. Set the function as indicated in Table 6 and make the indicated voltage checks.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

This is an alternate method of troubleshooting the circuits of Service Sheet 6. If these signatures are incorrect, recall that the data strobes are decoded on the circuitry of Service Sheet 15 and the data is output from the Microprocessor which is on Service Sheet 14. If these signatures are correct, and the problem does not seem to be related to modulation, return to Service Sheet BD4 for further digital troubleshooting. If the problem seems to be related to a modulation problem, continue troubleshooting on this service sheet or refer to Service Sheet BD2.

Test Equipment

Signature Analyzer . . . . HP 5004A

Purpose. To verify correct transfer of encoded data and strobe information from the Microprocessor to the modulation control latches.

Setup. Connect the signature analyzer as follows:

1) GND as close to the circuitry being probed as possible. (Bad grounding can cause unstable signatures.)
2) CLK to 'E' A11TP11
3) START to 'SA1' A11TP6
4) STOP to 'SA2' A11TP6

Set the signature analyzer controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN

Set up the Signal Generator as follows:

1) Disconnect the attenuator cable W17 from the power supply board to the attenuator.
2) Set the LOGIC/RAM switch P/O A11S1 to LOGIC.

NOTE

If the Signal Generator's address switch has been set to other than 07, the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON.

Table 5. FM Deviation Control Voltage Levels

Front Panel FM (kHz)	Measure the voltage* as indicated at										
	U13				U16						Test Point J6-pin 8 (Vrms)
	12	15	16	19	2	5	6	9	12	15	
1	L	L	L	L	H	H	H	H	L	H	0.2407
5	L	H	L	L	H	H	L	L	H	L	1.205
10	H	L	L	H	H	L	L	H	L	H	2.423
20	L	L	L	H	H	H	H	L	H	H	0.485
50	L	H	L	L	H	H	L	L	H	L	1.209
80	L	H	H	H	H	L	H	L	H	L	1.935
99	H	L	L	H	L	H	H	H	H	H	2.400

*Low ≤0.8Vdc; High ≥2.0Vdc.

SERVICE SHEET 6 (Cont'd)

Initialize. Briefly short A11TP3 NMI to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

Probe. Connect the probe to each node indicated in Tables 7 through 11. Verify that the signature is correct and stable.

NOTES

Disconnect any external modulation from the BNC jack.

In case of unstable or incorrect signatures, ground the data probe as close as possible to the node being tested.

Table 6. Function Control Voltage Levels

Function Selected	Control Latch	Pin No.	Logic* State	Comparator	Comparator Output (Vdc)	FET Switch	Open/ Closed
Int 1 kHz AM	U19	5	H	U21B	0.0	Q9	Closed
Int 400 Hz	U19	9	H	U22A	+1.0	Q11	Closed
Int Mod	U19	2	H	U22B	+5.0	Q10	Closed
Int FM	U19	6	H	U21D (SS12)	0.0	Q7 (SS12)	Closed
Ext AM	U19	16	H	U21A	0.0	Q8	Closed
Ext FM	U19	19	H	U21C (SS12)	0.0	Q6	Closed
Amplitude +10 dBm	U16	19	H	U18D	−13	Q4	Open
Ext AM No Input	—	—	—	U22D	−14	J6 Pin 4 J6 Pin 15	L H
Ext AM 1V-pk Input	—	—	—	U22D	−14	J6 Pin 14 J6 Pin 15	H L

* Low <+0.8 Vdc; High >+2.0 Vdc

SERVICE SHEET 6 (Cont'd)

Table 7. AM/Level Control Signatures

Node	Correct Signature	Comments
+5V	H6H5	
U5 #2	5713	Lev DAC
U5 #5	3UA1	
U5 #6	PF25	
U5 #9	8953	
U5 #12	U314	
U5 #15	28HU	
U5 #16	1PCP	
U5 #19	P5H2	
U9 #2	C33C	
U9 #5	UCUU	

Table 8. AM% Control Signatures

Node	Correct Signature	Comments
U9 #6	48U0	AM DAC
U9 #9	H934	
U9 #12	5449	
U9 #15	H3CA	
U9 #16	6U7U	
U9 #19	37P1	
U13 #2	5869	
U13 #5	05A7	
U13 #6	PU57	
U13 #9	P580	
U16 #19	7H7C	AM Range Select

Table 9. FM Deviation Control Signatures

Node	Correct Signature	Comments
+5V	H6H5	
U13 #12	50P3	FM DAC
U13 #15	3P3A	
U13 #16	681U	
U13 #19	6U79	
U16 #2	15A4	
U16 #5	0AU5	
U16 #6	5599	
U16 #9	F65U	
U16 #12	9467	
U16 #15	U761	

Table 10. Audio Oscillator Control Signatures

Node	Correct Signature	Comments
+5V	H6H5	
U19 #2	1821	OSC OUT
U19 #5	52HC	INT AM
U19 #6	7P3H	INT FM
U19 #9	3CU7	OSC FRQ
U19 #16	7FCP	EXT AM
U19 #19	4HFF	EXT FM

Incorrect signatures could be due to:

1) data to latch problem (data bus)
2) strobe to latch problem
3) latch problem
4) test point 'TO2' A2TP13 shorted to "GND" on the display board.

Table 11. Modulation Strobe Signatures

Node	Correct Signature	Comments
+5V	H6H5	
U5 #11	58AP	U5 Strobe
U9 #11	57F4	U9 Strobe
U13 #11	97CC	U13 Strobe
U16 #11	A5FP	U16 Strobe
U19 #11	P1H1	U19 Strobe

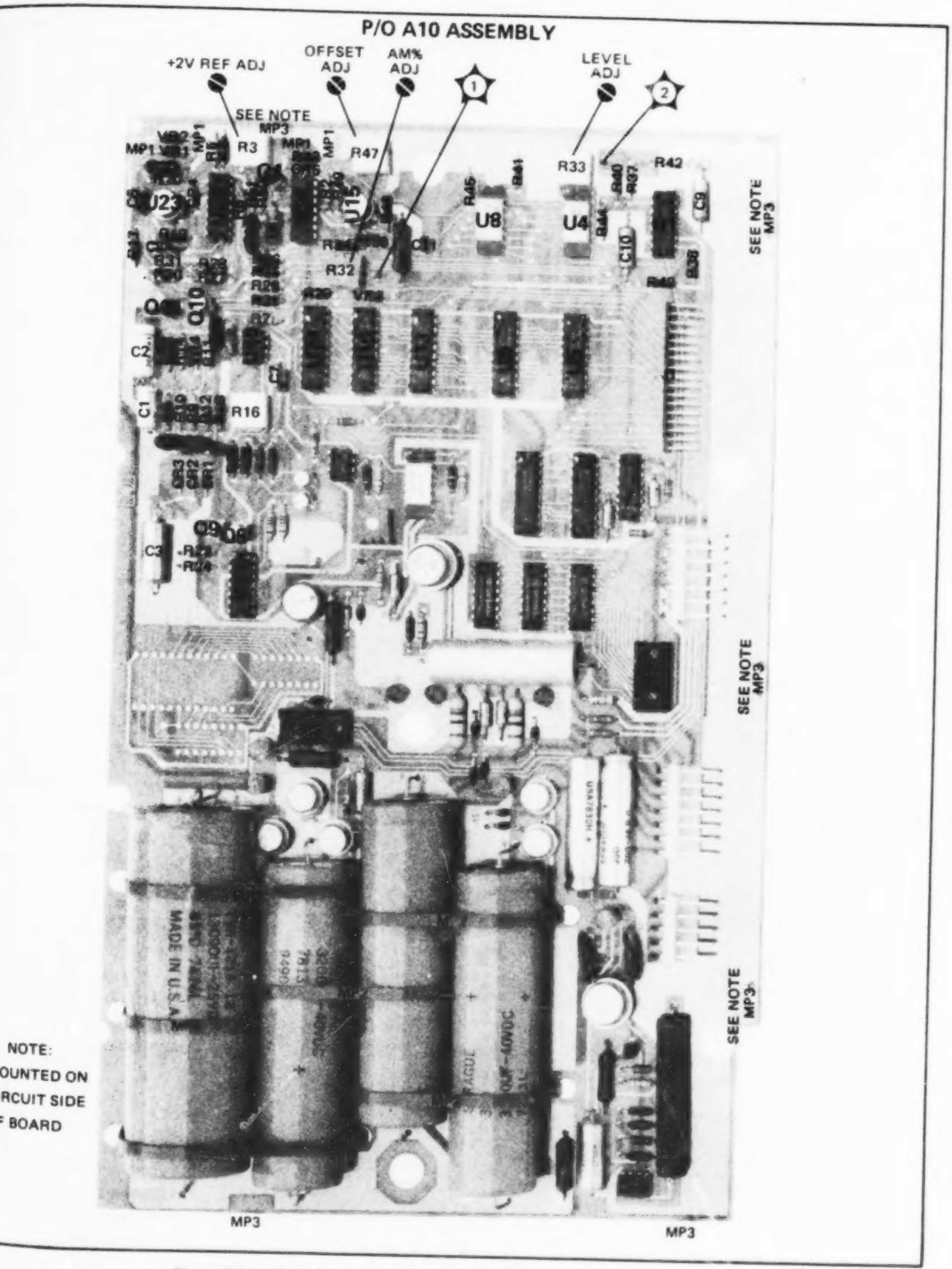
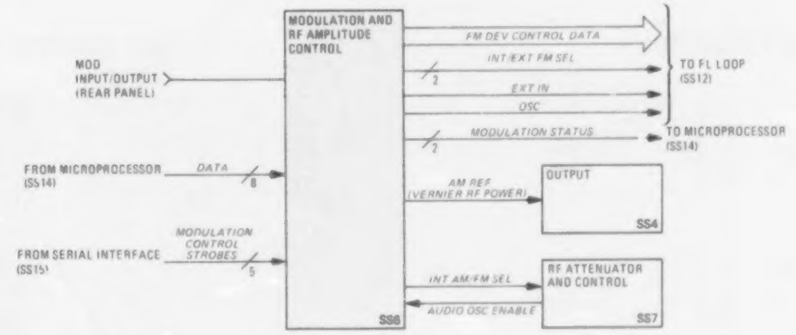

P/O A10 ASSEMBLY
+2V REF ADJ
OFFSET ADJ
AM% ADJ
①
LEVEL ADJ
②
SEE NOTE
MP3
R3
R47
MP1
R33
R42
R45
R41
R40
R37
U8
U4
U15
U23
R32
C9
C10
C11
SEE NOTE
MP3
SEE NOTE
MP3
SEE NOTE
MP3
Q10
C2
C1
R16
C3
Q9
MP3
MP3
NOTE:
OUNTED ON
RCUIT SIDE
F BOARD

Figure 8-55. Modulation and RF Amplitude Control Component Locations


MODULATION AND RF AMPLITUDE CONTROL
SS6
MOD INPUT/OUTPUT (REAR PANEL)
FROM MICROPROCESSOR (SS14)
DATA
8
FROM SERIAL INTERFACE (SS15)
MODULATION CONTROL STROBES
5
FM DEV CONTROL DATA
INT/EXT FM SEL
2
EXT IN
OSC
TO FL LOOP (SS12)
MODULATION STATUS
2
TO MICROPROCESSOR (SS14)
AM REF (VERNIER RF POWER)
OUTPUT
SS4
INT AM/FM SEL
AUDIO OSC ENABLE
RF ATTENUATOR AND CONTROL
SS7

AM SYSTEM

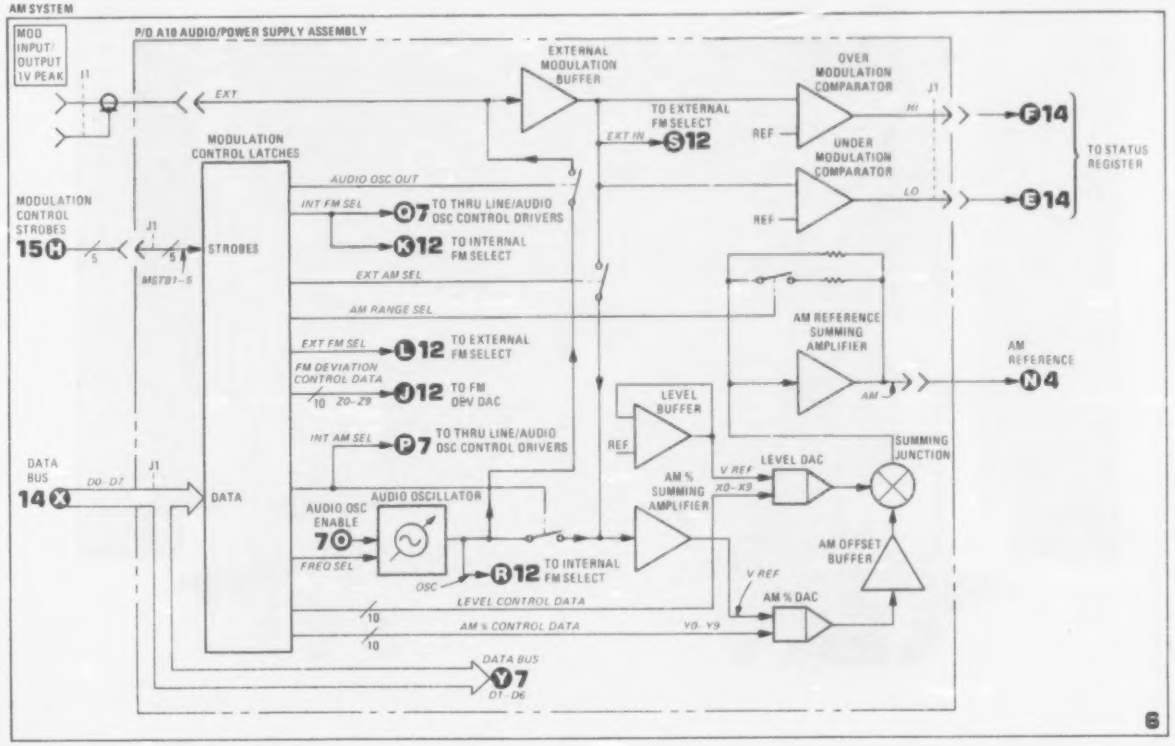
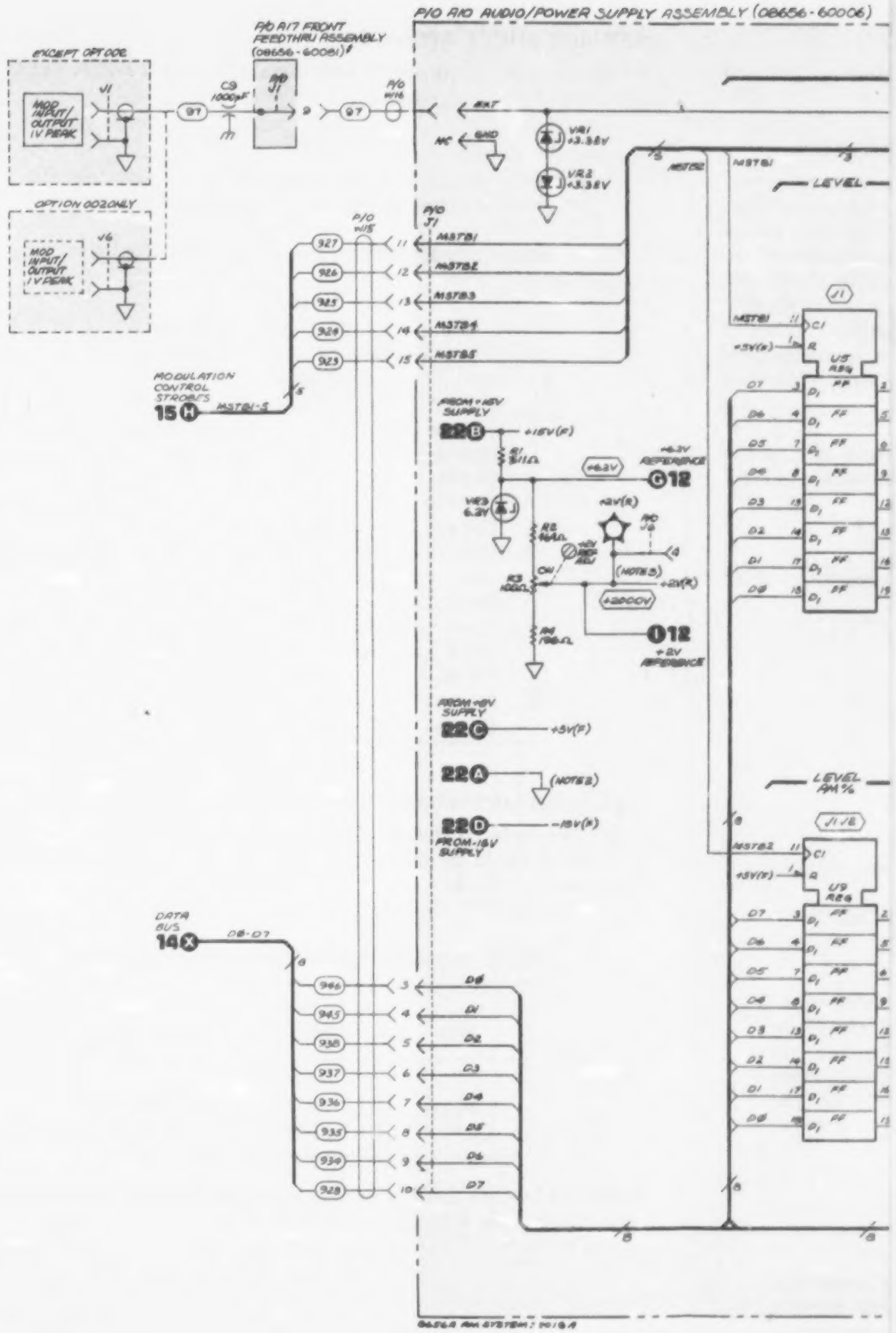
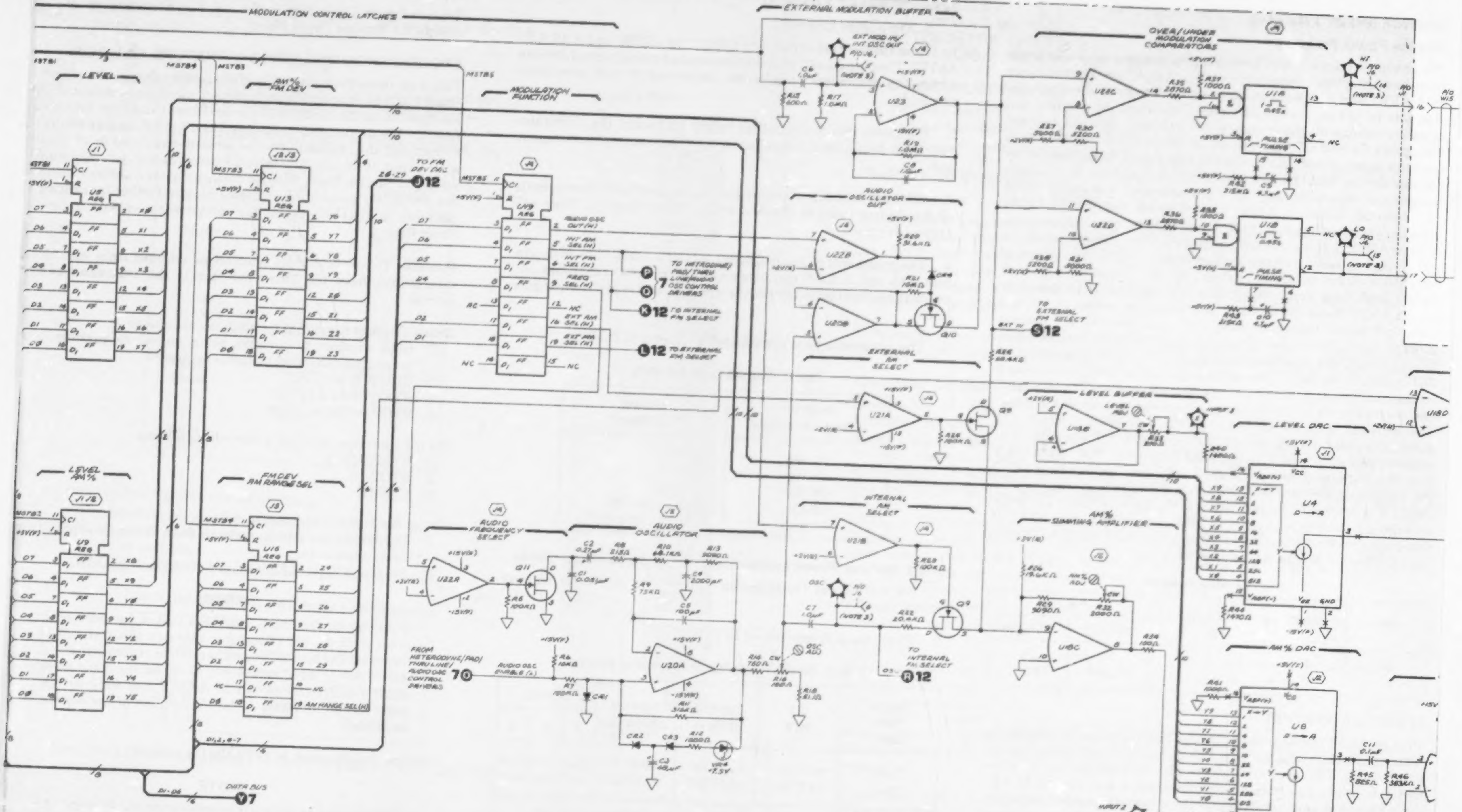

MOD INPUT/ OUTPUT 1V PEAK
J1
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY
EXT
EXTERNAL MODULATION BUFFER
OVER MODULATION COMPARATOR
REF
J1
HI
F14
UNDER MODULATION COMPARATOR
REF
LO
E14
TO STATUS REGISTER
TO EXTERNAL FM SELECT
EXT IN
S12
MODULATION CONTROL LATCHES
MODULATION CONTROL STROBES
15H
5
J1
5
MSTB1-5
STROBES
AUDIO OSC OUT
INT FM SEL
Q7 TO THRU LINE/AUDIO OSC CONTROL DRIVERS
K12 TO INTERNAL FM SELECT
EXT AM SEL
AM RANGE SEL
EXT FM SEL
L12 TO EXTERNAL FM SELECT
FM DEVIATION CONTROL DATA
10
20-29
J12 TO FM DEV DAC
INT AM SEL
P7 TO THRU LINE/AUDIO OSC CONTROL DRIVERS
AM REFERENCE SUMMING AMPLIFIER
AM
AM REFERENCE
N4
LEVEL BUFFER
REF
DATA BUS
14X
D0-D7
J1
DATA
AUDIO OSCILLATOR
AUDIO OSC ENABLE
7O
FREQ SEL
OSC
R12 TO INTERNAL FM SELECT
AM % SUMMING AMPLIFIER
V REF
X0-X9
LEVEL DAC
SUMMING JUNCTION
AM OFFSET BUFFER
V REF
AM % DAC
LEVEL CONTROL DATA
10
AM % CONTROL DATA
10
Y0-Y9
DATA BUS
Y7
D1-D6
6

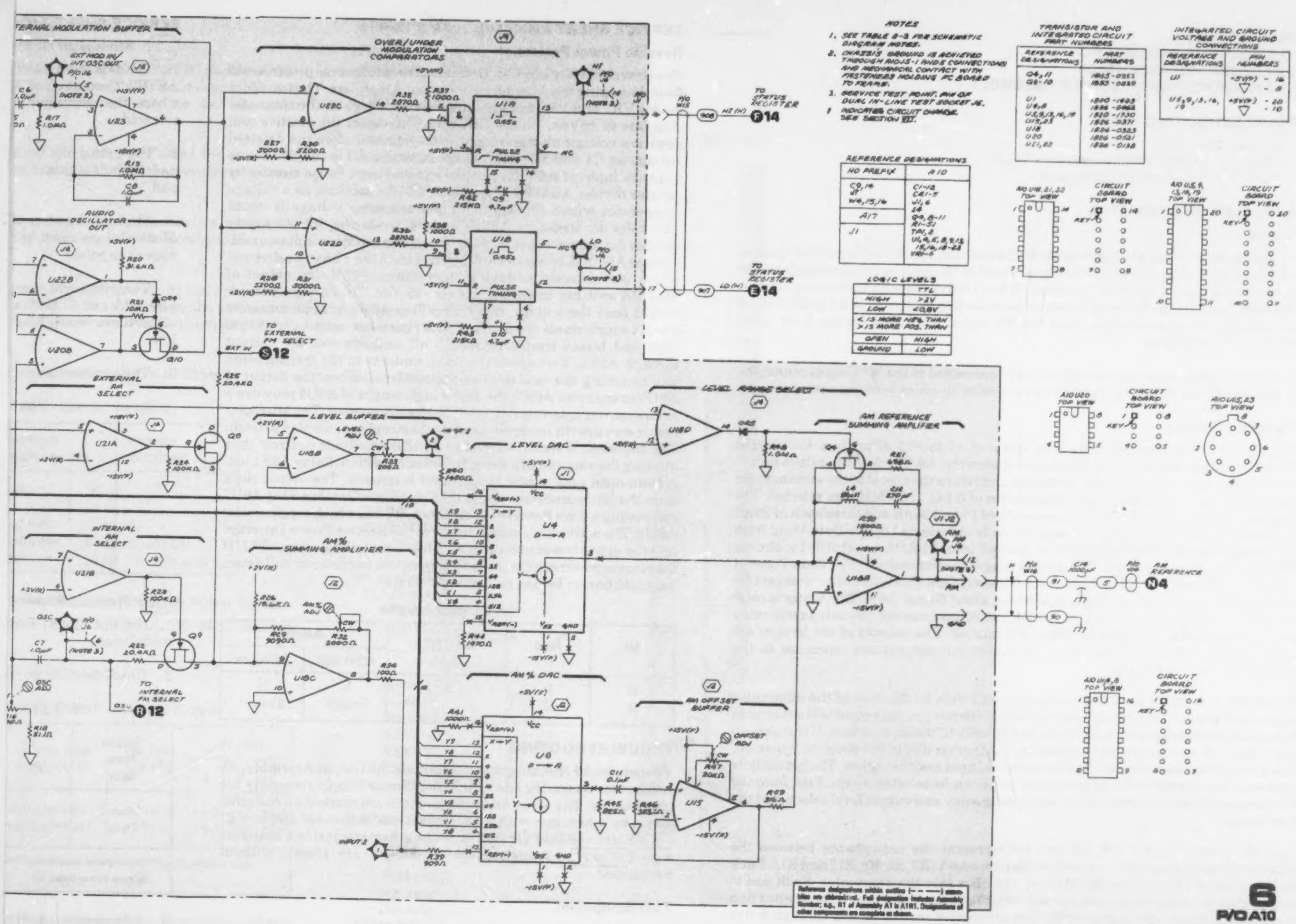
Figure 8-56. Modulation and RF Amplitude Control Block Diagrams


P/O A10 AUDIO/POWER SUPPLY ASSEMBLY (08656-60006)
EXCEPT OPT 002
MOD INPUT/ OUTPUT 1V PEAK
J1
OPTION 002 ONLY
MOD INPUT/ OUTPUT 1V PEAK
J6
97
C9 1000pF
P/O A17 FRONT FEEDTHRU ASSEMBLY (08656-60081)
P/O J1
9
97
P/O W16
EXT
NC
GND
VR1 +3.32V
VR2 +3.32V
P/O W15
P/O J1
927
926
925
924
923
11
12
13
14
15
MSTB1
MSTB2
MSTB3
MSTB4
MSTB5
MODULATION CONTROL STROBES
15H
MSTB1-5
5
5
MSTB2
MSTB1
3
LEVEL
FROM +15V SUPPLY
22B
+15V(F)
R1 511Ω
+6.2V
+6.2V REFERENCE
G12
VR3 6.2V
+2V(R)
P/O J6
R2
R3
R4
4
(NOTE 3)
+2V(R)
+2.000V
I12
+2V REFERENCE
FROM +5V SUPPLY
22C
+5V(F)
22A
(NOTE 2)
22D
-15V(F)
FROM -15V SUPPLY
J1
MSTB1
+5V(F)
C1
R
U5 REG
D7
D6
D5
D4
D3
D2
D1
D0
FF
D1
J1/E
MSTB2
+5V(F)
U9 REG
LEVEL AM %
8
DATA BUS
14X
D0-D7
8
946
945
938
937
936
935
934
928
3
4
5
6
7
8
9
10
D0
D1
D2
D3
D4
D5
D6
D7
8
8
8656A AM SYSTEM: 7019A

Y (08656-60006)



MODULATION CONTROL LATCHES
LEVEL
AM%/FM DEV
MODULATION FUNCTION
LEVEL AM%
FM DEV AM RANGE SEL
MSTB1
MSTB2
MSTB3
MSTB4
MSTB5
U5 RS6
U13 RS6
U19 RS6
U9 RS6
U15 RS6
TO FM DEV DAC
J12
AUDIO OSC OUT (H)
INT AM SEL (H)
INT FM SEL (H)
FREQ SEL (H)
EXT AM SEL (H)
EXT FM SEL (H)
TO HETRODYNE/PAD/THRU LINE/AUDIO OSC CONTROL DRIVERS
TO INTERNAL FM SELECT
TO EXTERNAL FM SELECT
AM RANGE SEL (H)
DATA BUS
D1-D6
Y7
EXTERNAL MODULATION BUFFER
EXT MOD IN/INT OSC OUT
U23
AUDIO OSCILLATOR OUT
U22B
U20B
Q10
EXTERNAL AM SELECT
U21A
Q8
INTERNAL AM SELECT
U21B
Q9
TO INTERNAL FM SELECT
R12
TO EXTERNAL FM SELECT
S12
OVER/UNDER MODULATION COMPARATORS
U28C
U28D
U1A
U1B
PULSE TIMING
HI
LO
(NOTE 3)
LEVEL BUFFER
U18B
LEVEL DAC
U4
D→A
AM% SUMMING AMPLIFIER
U18C
AM% ADJ
AM% DAC
U8
INPUT 2
AUDIO FREQUENCY SELECT
U22A
Q11
AUDIO OSCILLATOR
U20A
OSC ADJ
FROM HETERODYNE/PAD/THRU LINE/AUDIO OSC CONTROL DRIVERS
AUDIO OSC ENABLE (L)
7O
VR4 +7.5V
U18D


TERNAL MODULATION BUFFER
EXT MOD IN/ INT OSC OUT
P/O J6
(NOTE 3)
C6 1.0µF
R17 1.0MΩ
U23
+15V(F)
-15V(F)
R19 1.0MΩ
C8 1.0µF
AUDIO OSCILLATOR OUT
U22B
R20 31.6KΩ
CR4
R21 10MΩ
U20B
Q10
TO EXTERNAL FM SELECT
EXT IN
S12
R26 20.4KΩ
EXTERNAL AM SELECT
U21A
Q8
R24 100KΩ
+2V(R)
INTERNAL AM SELECT
U21B
R23 100KΩ
OSC
P/O J6
C7 1.0µF
R22 20.4KΩ
Q9
OSC ADJ
R16
R18 51.1Ω
TO INTERNAL FM SELECT
OSC
R12
OVER/UNDER MODULATION COMPARATORS
U22C
U22D
R35 2870Ω
R37 1000Ω
R27 5000Ω
R30 5200Ω
R36 2870Ω
R38 1000Ω
R28 5200Ω
R31 5000Ω
U1A
U1B
0.45s
PULSE TIMING
R42 215KΩ
C9 4.7µF
R43 215KΩ
C10 4.7µF
HI
LO
NC
P/O J1
P/O W15
TO STATUS REGISTER
HI (H)
F14
LO (H)
E14
LEVEL BUFFER
U18B
LEVEL ADJ
R33 200Ω
CW
R40 1400Ω
LEVEL DAC
U4
D → A
X → Y
VREF(+)
VREF(-)
VCC
VEE
GND
X9
X8
X7
X6
X5
X4
X3
X2
X1
X0
R44 1470Ω
AM% SUMMING AMPLIFIER
R26 19.6KΩ
AM% ADJ
R29 9090Ω
R32 2000Ω
U18C
R34 100Ω
AM% DAC
U8
R41 1000Ω
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
INPUT 2
R39 909Ω
C11 0.1µF
R45 825Ω
R46 383Ω
AM OFFSET BUFFER
OFFSET ADJ
R47 20KΩ
U15
R49 316Ω
LEVEL RANGE SELECT
U18D
CR5
R48 1.0MΩ
AM REFERENCE SUMMING AMPLIFIER
Q4
R51 698Ω
L4
C12 270pF
R50 1000Ω
U18A
AM
P/O J6
GND
P/O W16
C16 1000pF
P/O W4
AM REFERENCE
N4
A10 U18,21,22 TOP VIEW
CIRCUIT BOARD TOP VIEW
A10 U5,9,13,16,19 TOP VIEW
KEY
A10 U20 TOP VIEW
A10 U15,23 TOP VIEW
A10 U4,8 TOP VIEW

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A10J5-1 AND 5 CONNECTIONS AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKET J6.

1 INDICATES CIRCUIT CHANGE. SEE SECTION VII.

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q4,11	1855-0353
Q8-10	1855-0039
U1	1820-1423
U4,8	1826-0462
U5,9,13,16,19	1820-1730
U15,23	1826-0371
U18	1826-0323
U20	1826-0521
U21,22	1826-0138

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V(F) - 16 ▽ - 8
U5,9,13,14,19	+5V(F) - 20 ▽ - 10

REFERENCE DESIGNATIONS

NO PREFIX	A10
C9,14 J7 W4,15,16	C1-12 CR1-5 J1,6 L4 Q4,8-11 R1-51 TP1,2 U1,4,5,8,9,13,15,16,18-23 VR1-4
A17	
J1	

LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

6
P/O A10

Figure 8-57. Modulation and RF Amplitude Control Schematic Diagram

SERVICE SHEET 7
P/O A6 OUTPUT ASSEMBLY
A9 ATTENUATOR ASSEMBLY
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD2
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

Encoded data from the Microprocessor is clocked into the Heterodyne/Pad Control and Thru Line Control Latches. The data is held in the latches for approximately 60 ms after the last clock pulse. At this time, U3A or U3B resets which clears the latches. The control signals enable the heterodyne mode (at frequencies from 0.1 to 123.5 MHz) and add or remove attenuation from the RF signal depending on the front panel setting of RF amplitude.

If excessive power from an external source is connected to the RF Output connector, the Reverse Power protection circuits cause a relay in series with the output to open.

Attenuator Control

Frequencies of 123.5 to 990 MHz and levels of −7 to +15 dBm from the Output Assembly, A6 are applied to the Attenuator Assembly, A9. The first two relays switch the input signal out to the Output Assembly and return the signal to the attenuator in the Heterodyne mode when output frequencies of 0.1 to 123.5 MHz are selected. The attenuator has five attenuator pads, one each of 10 and 20 dB and three each of 30 dB for a total of 120 dB. The correct attenuator pads are selected by the Data Word from the Microprocessor. The Data word is latched into A10U10 or A10U6 by strobes ASTB1 or ASTB2 respectively. The strobes trigger the Heterodyne/Pad Data Timeout One-shot U3B and the Thru Line Data Timeout One-shot U3A. The monostable multivibrator outputs are set high. At timeout, about 60 ms, the multivibrator is reset low which resets the control latch. During the 60 ms interval, the attenuator relay pads or heterodyne relays are selected and latched. The outputs of the latches are applied to the control drivers where the active low outputs are connected to the attenuator's relay solenoids.

The center of each solenoid is connected to +24 Vdc. In the case of the attenuator relays, each low output of the drivers will switch the relay so the output will either pass through an attenuator pad or be connected directly to the next section. If the connection is through a pad, a ground is connected to that section of the stripline bypassed. This greatly increases the isolation between the input and the output. The heterodyne mode and any combination of attenuator pads can be selected by the data from the Microprocessor which is dependent on the frequency and output level selected at the front panel.

Capacitors A9A1C1, C2, C3, C6 and C8 represent the capacitance between the adjustment wire loop and the associated resistors A9A1R2, R5, R8, R12 and R15. Each one is adjusted by coupling 990 MHz at +10 dBm into the attenuator. Each pad is individually adjusted to the preset power meter reference level minus the attenuation of the selected pad. The output of the last attenuator section passes through a five section printed circuit board filter that matches the attenuator to the Reverse Power Limiter and Detector.

SERVICE SHEET 7 (Cont'd)

Reverse Power Protection

The Reverse Power Limiter/Detector prevents reverse power levels from damaging the Attenuator or Output Amplifiers. The two zener diodes VR1 and VR2 limit the maximum voltage on the transmission line to ±5Vpk. Diodes CR1 and CR2 detect the positive and negative voltage on the transmission line and store the detected voltage on C4 and C5. The voltage stored on C4 is coupled to the negative input of A6U10A in the Reverse Power Sense circuits by resistor divider A9A1R9 and A6R92. U10A functions as a voltage comparator where the positive input reference voltage is about +2.5 volts dc. Resistors A6R93 and 94 divide the +5V(F) supply voltage for the reference voltage. When the negative input to comparator A6U10A becomes more positive than the +2.5 volt reference, which is a detected voltage greater than +2.75V, the output of A6U10A switches to approximately −15 Vdc. The current through A6R95 fixes the voltage at J-K Flip-Flop A6U9 at approximately 0 volts which resets the flip-flop. The active low output of A6U9 is high and biases transistor A6Q13 off and removes the current through A9K1. This opens the relay contacts in the transmission line removing the external overvoltage level. When the output of A6U9 opens relay A9K1, the active high output of A6U9 provides a reverse power interrupt, RP1, to the Microprocessor. The Microprocessor services the interrupt causing the Amplitude display to flash. The keyboard is locked up except for the Amplitude controls thus alerting the operator of a Reverse Power condition. Relay A9K1 will remain open until a new output level is entered. The output clock from the Microprocessor clocks the Data Time Out One-Shot A6U7 generating a 2 ms Reverse Power Clock, RPCL, which toggles (sets) A6U9. The active high output removes the Reverse Power Interrupt and the active low output turns on A6Q13 energizing relay A9K1. If the reverse power condition was not removed, the detector will detect the condition as before, re-opening the relay.

Table 1. A6U9 Operation

Set	Reset	CLK (RPCL) To J-K	Outputs	
			Active High	Active Low
H H	L H	X ↑	L Toggle	H Toggle

TROUBLESHOOTING

Procedures for checking the circuits of the A6 Output Assembly, A9 Attenuator Assembly and A10 Audio/Power Supply Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g., √1. Fixed voltages are shown on the schematic inside a hexagon, e.g. 2V±0.2V. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Oscilloscope	HP 1222A

SERVICE SHEET 7 (C

√1 Attenuator Cont

1. The data word is latc ASTB2. The outputs of th where the active-low c solenoids.

2. High data bits to cc pad; high data bits to cc pad.

3. The high data bits a of the drivers must be appear as pulses.

4. The pulses will be ap bles U3A and B. Each n resets the control latch a low.

5. The attenuator pads

Table 2

Amplitude Entered at Front
−5 dBm −15 dBm −25 dBm −55 dBm −85 dBm

√2 Reverse Power L

1. Set the Signal Gen modulation.

2. Check the voltages s

Table 3. Revers

Reverse Power Relay	U10 Pin 6
Closed Open	+4.5Vdc +4.5Vdc*

*The output of comparator U10 Reverse Power Relay K1.

3. After reverse power h front panel and check for

ERVICE SHEET 7 (Cont'd)

1〉 Attenuator Control

The data word is latched into A10U10 by ASTB1 and A10U6 by STB2. The outputs of the latches are applied to the Control Drivers here the active-low outputs are connected to the attenuator lenoids.

High data bits to control latch U10 will select the attenuator ad; high data bits to control latch U6 will remove the attenuator ad.

The high data bits at the control latches and active low outputs f the drivers must be checked using an oscilloscope. They will ppear as pulses.

The pulses will be approximately 60 ms controlled by monostables U3A and B. Each monostable is triggered by the strobes and sets the control latch after 60 ms when the active high output goes w.

The attenuator pads are selected as shown in Table 2.

Table 2. Step Attenuator Switching

Amplitude Entered at Front Panel	Attenuator Pads Selected
-5 dBm	10 dB
-15 dBm	20 dB
-25 dBm	30 dB (A)
-55 dBm	30 dB (A) and (B)
-85 dBm	30 dB (A), (B) and (C)

√2〉 Reverse Power Limiter/Detector, Reverse Power Sense

1. Set the Signal Generator to -10 dBm at 500 MHz without modulation.

2. Check the voltages shown in Table 3.

Table 3. Reverse Power Protection Operating Voltages

Reverse Power Relay	U10 Pin 6	Test Point J3 Pin 11	Test Point J3 Pin 10	Q1 (Vdc)		
				E	B	C
Closed	+4.5Vdc	+4.5Vdc	+0.2Vdc	+5.0	+4.3	+5.0
Open	+4.5Vdc*	+4.5Vdc*	+5.0Vdc	+5.0	+5.0	+0.0

*The output of comparator U10A-pin 6 will be low only for the time required to open Reverse Power Relay K1.

3. After reverse power has been removed, enter an amplitude at the front panel and check for the Reverse Power Clock at U9 pin 12. The Reverse Power Clock toggles the J-K Flip-Flop biasing Q13 and closing the Reverse Power Relay.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

This is an alternate method of troubleshooting the circuits of Service Sheet 7. If these signatures are incorrect, recall that the data strobes are decoded on the circuitry of Service Sheet 15 and the data comes from the Microprocessor on Service Sheet 14. If these signatures are correct and the problem does not seem to be related to 10 dB step attenuation or a 0.1 to 123.5 MHz RF output signal, you may want to return to Service Sheet BD4 for further digital troubleshooting. If the previously mentioned problems require further investigation, continue to troubleshoot on this service sheet or refer to Service Sheet BD2.

Purpose. To verify correct transfer of encoded data and strobe information from the Microprocessor to the attenuator control latches.

Setup. Connect the signature analyzer as follows:
1) GND as close to circuitry being probed as possible. (Bad grounding can cause unstable signatures.)
2) CLK to E A11TP11
3) START SA1 A11TP5
4) STOP to SA2 A11TP6

Set the signature analyzer's controls as follows:
1) START-OUT
2) STOP-IN
3) CLK-IN

Set up the Signal Generator as follows:
1) Disconnect the attenuator cable from the power supply board to the attenuator.
2) Set the LOGIC/RAM switch P/O A11S1 to LOGIC.

NOTE

If the Signal Generator's address switch has been set to other than 07, the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON. Refer to Service Sheet 17 for the location of the address switches.

Initialize. Briefly short A11TP3 NMI to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

SERVICE SHEET 7 (Cont'd)

Probe. Connect the probe to each node in Tables 4 and 5. Verify a correct and stable signature at each node.

NOTE

In case of unstable or incorrect signatures, ground the data probe as close as possible to the node being tested.

Table 4. Heterodyne/Pad and Thru Line Control Signatures

Node	Correct Signature	Comments
+5V	H6H5	HET/PAD Control Latch
U10 #2	FP66	
U10 #5	U274	
U10 #6	PCH2	
U10 #9	7A42	
U10 #12	8301	
U10 #15	8FFP	
+5V	H6H5	THRU LINE Control Latch
U6 #2	0P73	
U6 #5	3793	
U6 #6	U75P	
U6 #9	63H2	
U6 #12	7418	
U6 #15	4F66	

An incorrect signature could be due to:
1) data to latch problem (data bus)
2) strobe to latch problem
3) latch problem
4) TO2 A2TP13 shorted to GND on the display board.

Table 5. Heterodyne/Pad and Thruline Strobe Signatures

Node	Correct Signature	Comments
+5V	H6H5	
U10 #11	8685	U10 STROB
U6 #11	CF57	U6 STROB

Reset the LOGIC/RAM switch to the RAM position. Reconnect the attenuator cable W17.

P/O A9A1 ASSEMBLY

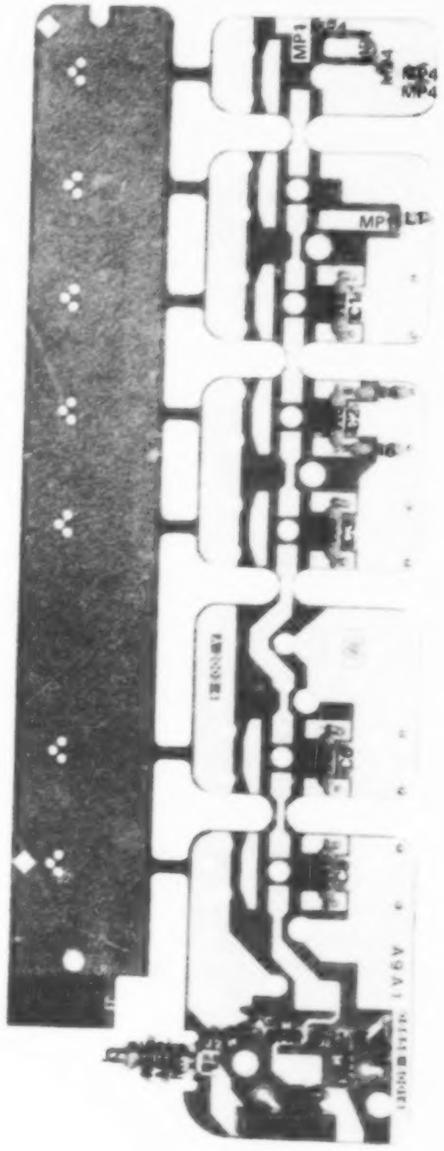


Figure 8-58. Attenuator Component Locations (Top View)

P/O A9A1 ASSEMBLY

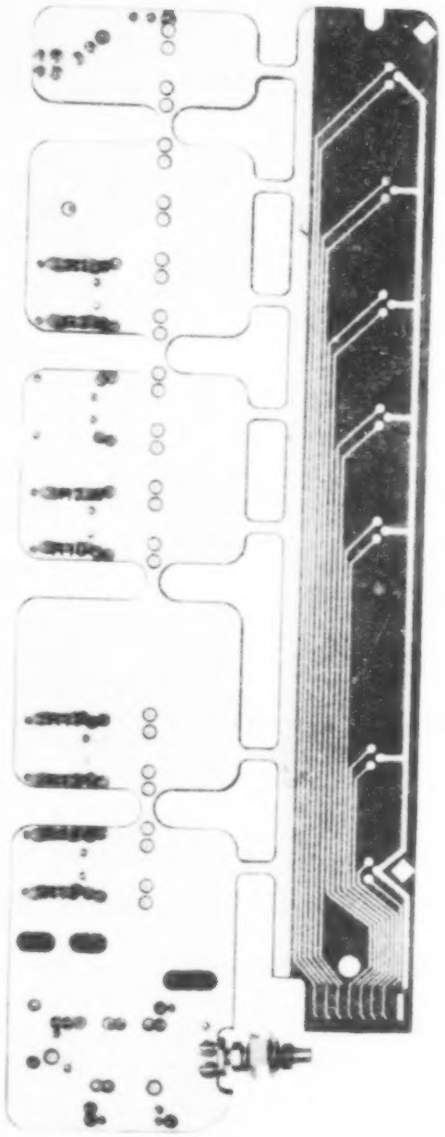


Figure 8-59. Attenuator Component Locations (Bottom View)

P/O A10 ASSEMBLY

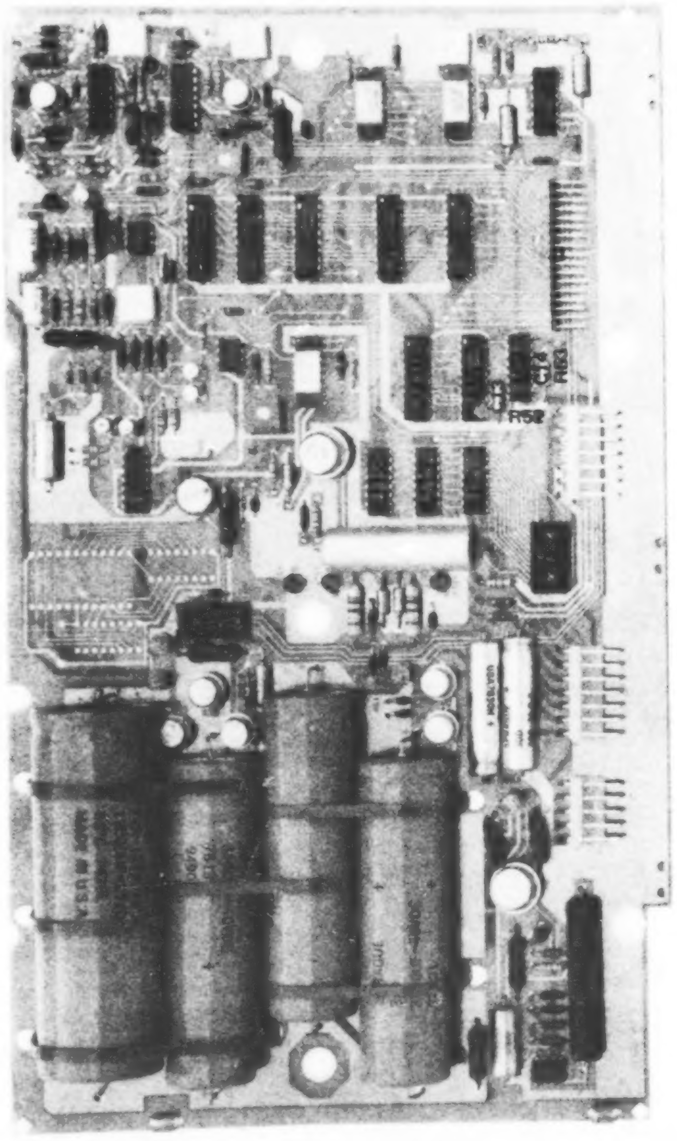


Figure 8-60. Attenuator Control Component Locations

P/O A6 ASSEMBLY

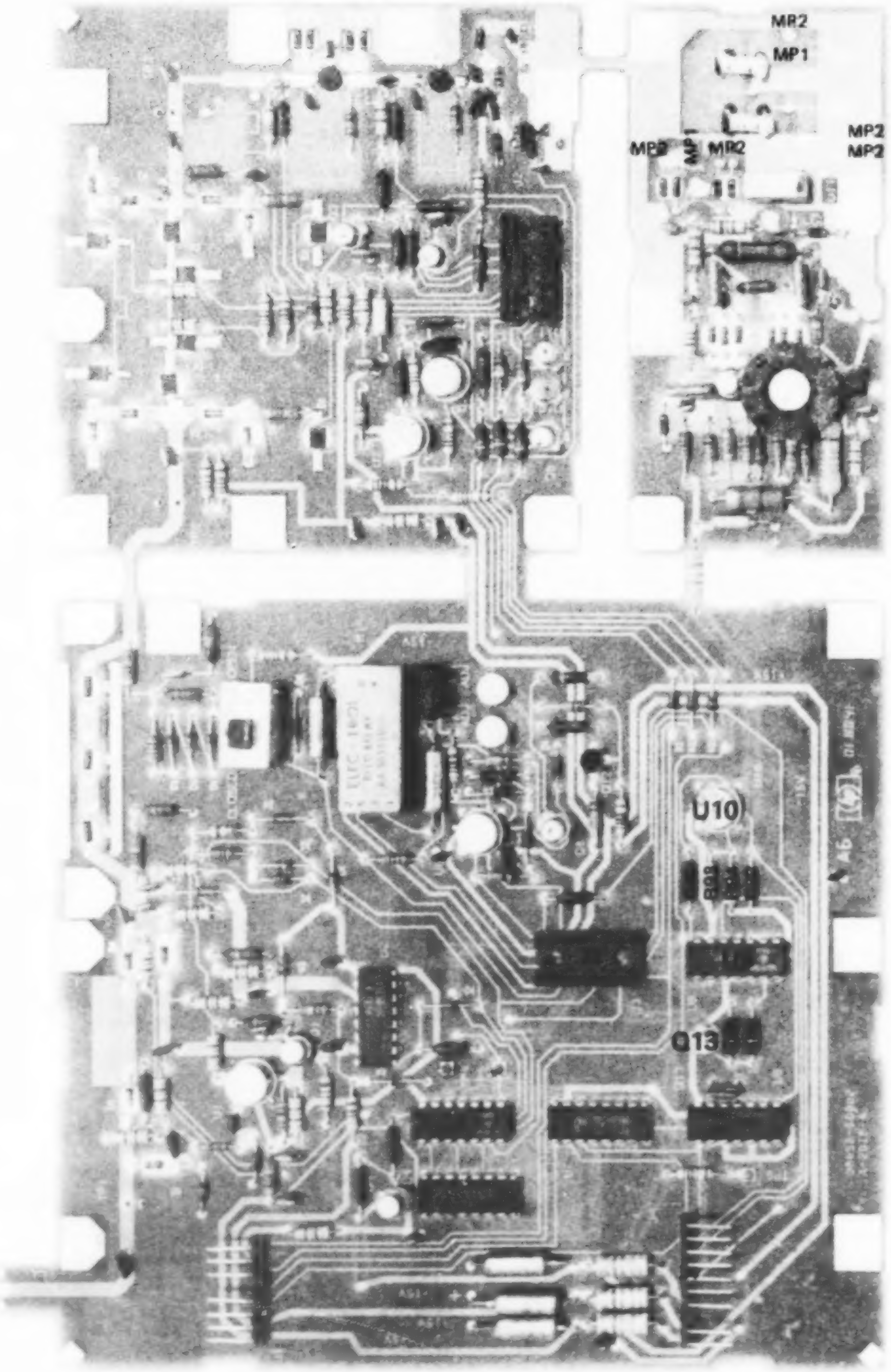
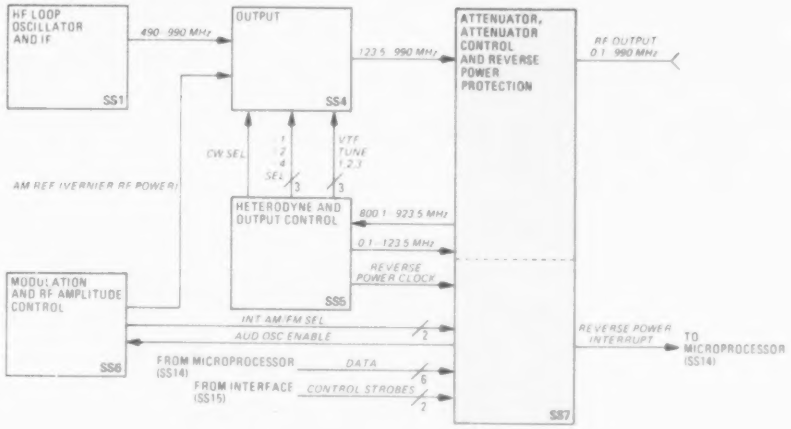

MR2
MP1
MP2
MP2
MP2
MP1
MR2
U10
R98
Q13

Figure 8-61. Reverse Power Protection Component Locations


HF LOOP OSCILLATOR AND IF
SS1
490 - 990 MHz
OUTPUT
SS4
123.5 - 990 MHz
ATTENUATOR, ATTENUATOR CONTROL AND REVERSE POWER PROTECTION
SS7
RF OUTPUT 0.1 - 990 MHz
CW SEL
SEL
VTF TUNE 1,2,3
AM REF (VERNIER RF POWER)
HETERODYNE AND OUTPUT CONTROL
SS5
800.1 - 923.5 MHz
0.1 - 123.5 MHz
REVERSE POWER CLOCK
MODULATION AND RF AMPLITUDE CONTROL
SS6
INT AM/FM SEL
AUD OSC ENABLE
FROM MICROPROCESSOR (SS14)
DATA
FROM INTERFACE (SS15)
CONTROL STROBES
REVERSE POWER INTERRUPT
TO MICROPROCESSOR (SS14)

ATTENUATOR, ATTENUATOR CONTROL AND REVERSE POWER PROTECTION

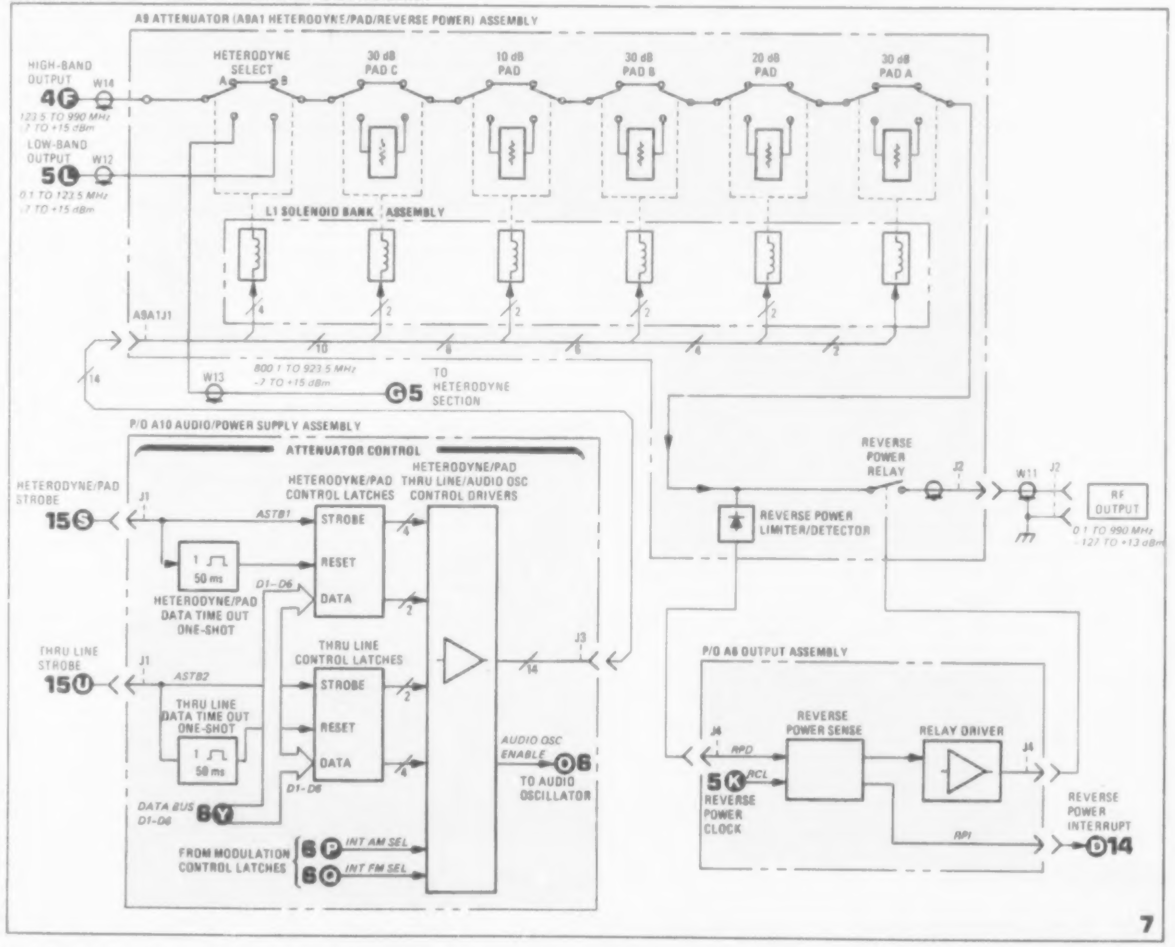
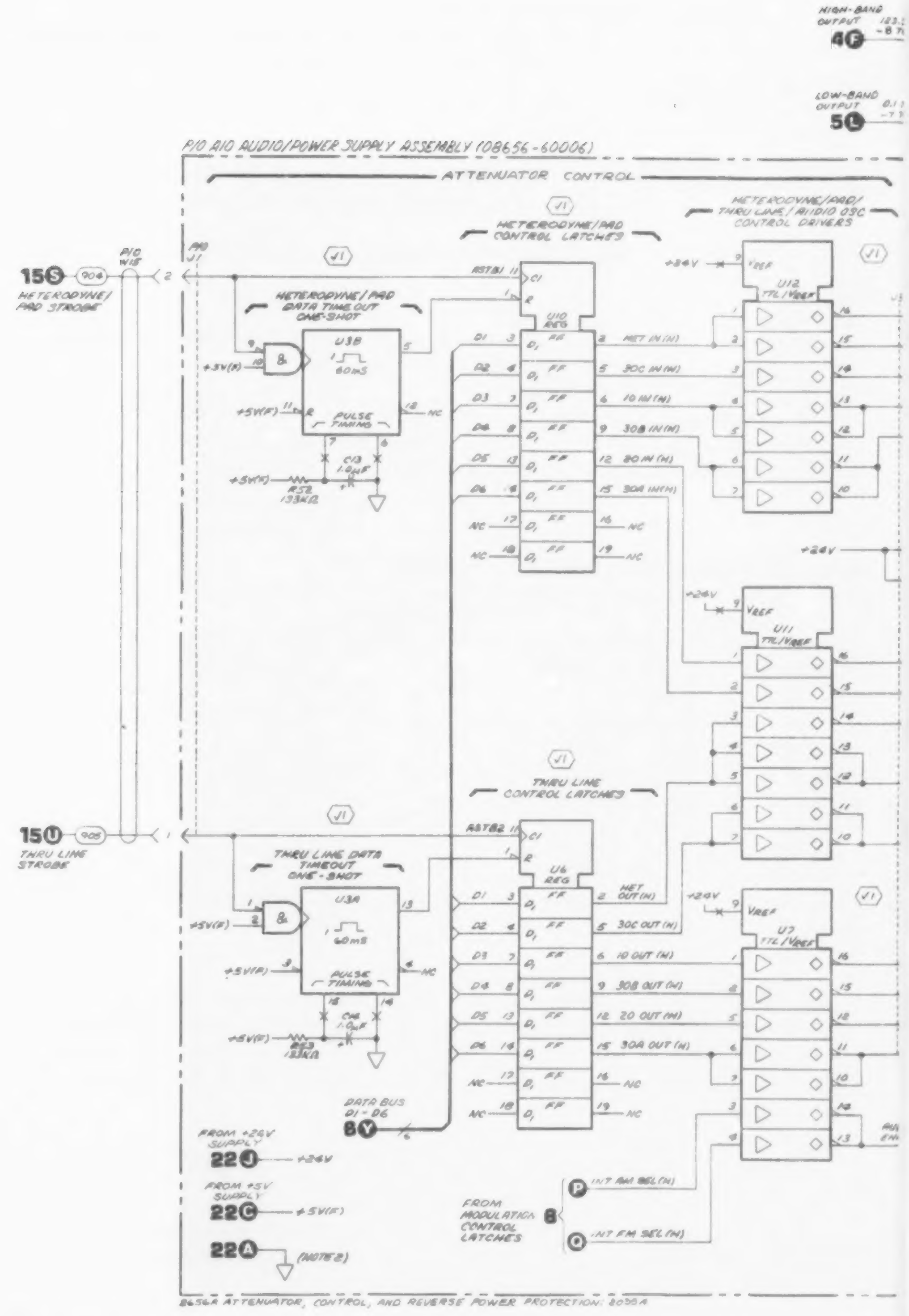
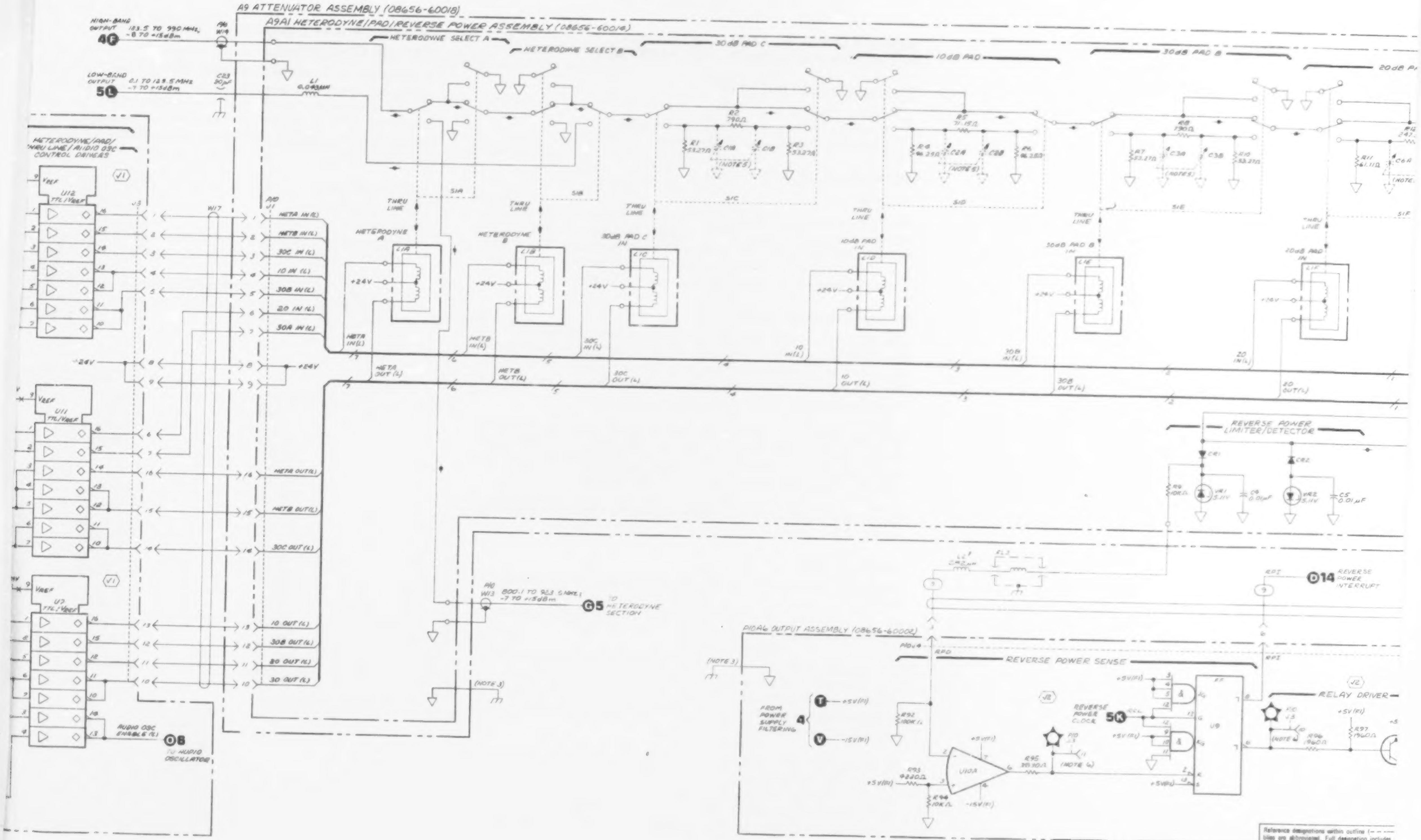
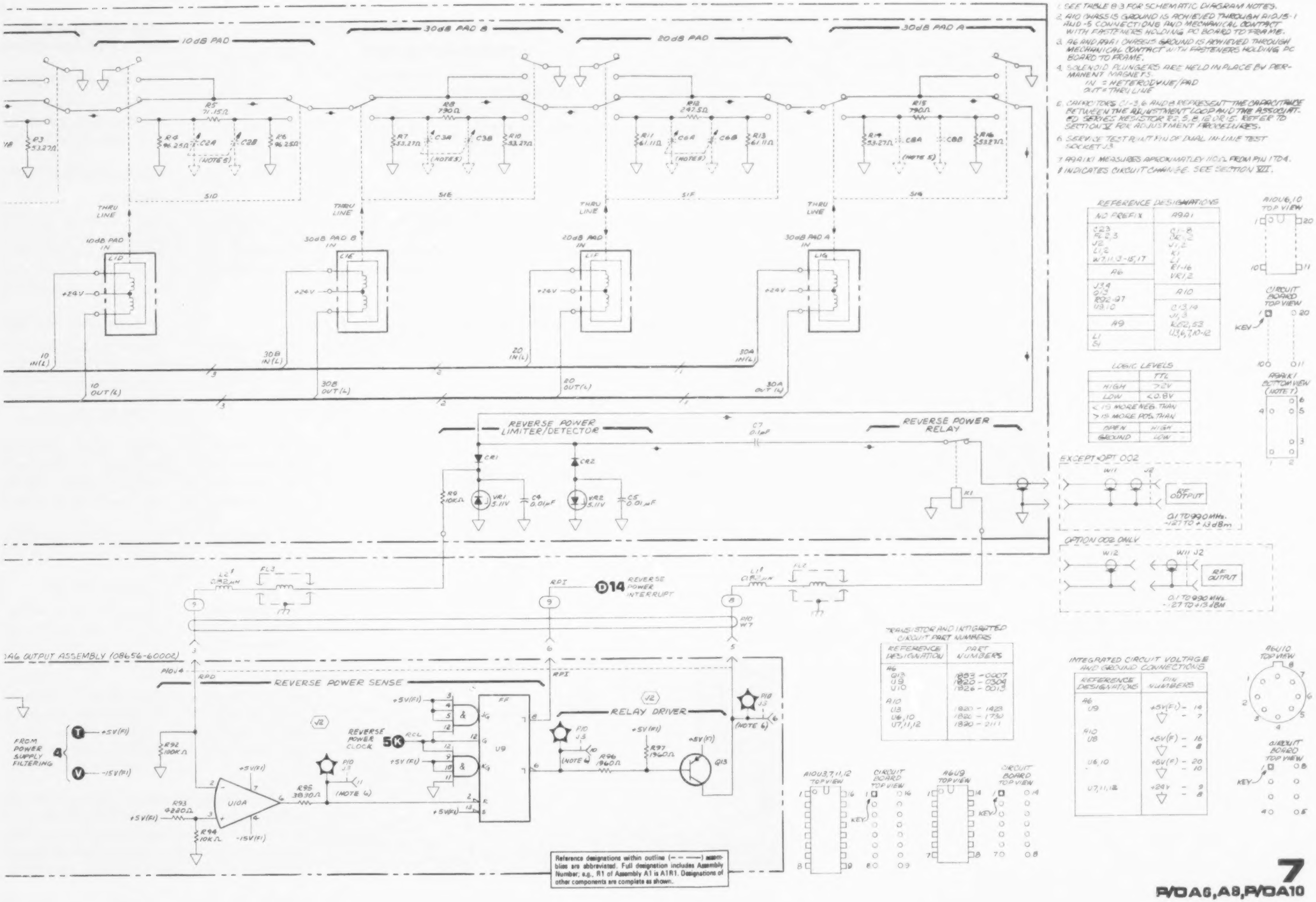

A8 ATTENUATOR (A8A1 HETERODYNE/PAD/REVERSE POWER) ASSEMBLY
HIGH-BAND OUTPUT
W14
4F
123.5 TO 990 MHz -7 TO +15 dBm
LOW-BAND OUTPUT
W12
5L
0.1 TO 123.5 MHz -7 TO +15 dBm
HETERODYNE SELECT
A
B
30 dB PAD C
10 dB PAD
30 dB PAD B
20 dB PAD
30 dB PAD A
L1 SOLENOID BANK ASSEMBLY
A8A1J1
W13
800.1 TO 923.5 MHz -7 TO +15 dBm
G5
TO HETERODYNE SECTION
REVERSE POWER RELAY
J2
W11
J7
RF OUTPUT
0.1 TO 990 MHz -127 TO +13 dBm
REVERSE POWER LIMITER/DETECTOR
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY
ATTENUATOR CONTROL
HETERODYNE/PAD CONTROL LATCHES
HETERODYNE/PAD THRU LINE/AUDIO OSC CONTROL DRIVERS
HETERODYNE/PAD STROBE
15S
J1
ASTB1
STROBE
RESET
DATA
50 ms
D1-D6
HETERODYNE/PAD DATA TIME OUT ONE-SHOT
THRU LINE STROBE
15U
ASTB2
THRU LINE CONTROL LATCHES
THRU LINE DATA TIME OUT ONE-SHOT
DATA BUS D1-D6
8Y
J3
AUDIO OSC ENABLE
O6
TO AUDIO OSCILLATOR
FROM MODULATION CONTROL LATCHES
6P
INT AM SEL
6Q
INT FM SEL
P/O A6 OUTPUT ASSEMBLY
J4
RPD
5K
RCL
REVERSE POWER CLOCK
REVERSE POWER SENSE
RELAY DRIVER
RPI
REVERSE POWER INTERRUPT
D14
7

Figure 8-62. Attenuator, Attenuator Control and Reverse Power Protection Block Diagrams


HIGH-BAND OUTPUT
4F
LOW-BAND OUTPUT
5L
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY (08656-60006)
ATTENUATOR CONTROL
15S
904
HETERODYNE/PAD STROBE
P/O W15
HETERODYNE/PAD DATA TIME OUT ONE-SHOT
U3B
60mS
PULSE TIMING
C13 1.0µF
R58 133KΩ
HETERODYNE/PAD CONTROL LATCHES
ASTB1
U10 REG
HET IN (H)
30C IN (H)
10 IN (H)
30B IN (H)
20 IN (H)
30A IN (H)
NC
HETERODYNE/PAD/THRU LINE/AUDIO OSC CONTROL DRIVERS
U12 TTL/VREF
U11 TTL/VREF
U7 TTL/VREF
+24V
15U
905
THRU LINE STROBE
THRU LINE DATA TIMEOUT ONE-SHOT
U3A
60mS
PULSE TIMING
C14 1.0µF
R63 133KΩ
THRU LINE CONTROL LATCHES
ASTB2
U6 REG
HET OUT (H)
30C OUT (H)
10 OUT (H)
30B OUT (H)
20 OUT (H)
30A OUT (H)
DATA BUS D1-D6
8Y
FROM +24V SUPPLY
22J
FROM +5V SUPPLY
22C
+5V(F)
22A
(NOTE 2)
FROM MODULATION CONTROL LATCHES
8
P
INT AM SEL (H)
Q
INT FM SEL (H)
8656A ATTENUATOR, CONTROL, AND REVERSE POWER PROTECTION: 2030A


A9 ATTENUATOR ASSEMBLY (08656-60018)
A9A1 HETERODYNE/PAD/REVERSE POWER ASSEMBLY (08656-60014)
HIGH-BAND OUTPUT 123.5 TO 990 MHz, -8 TO +15dBm
4F
A6 W14
LOW-BAND OUTPUT 0.1 TO 123.5 MHz -7 TO +15dBm
5L
C23 30pF
L1 0.093μH
HETERODYNE SELECT A
HETERODYNE SELECT B
30dB PAD C
10dB PAD
30dB PAD B
20dB P
R1 53.27Ω
R2 790Ω
R3 53.27Ω
C1A
C1B
(NOTE 5)
S1A
S1B
S1C
R4 96.25Ω
R5 71.15Ω
R6 96.25Ω
C2A
C2B
S1D
R7 53.27Ω
R8 790Ω
R10 53.27Ω
C3A
C3B
S1E
R11 61.11Ω
R12 247.
C6A
S1F
THRU LINE
HETERODYNE A
HETERODYNE B
30dB PAD C IN
10dB PAD IN
30dB PAD B IN
20dB PAD IN
L1A
L1B
L1C
L1D
L1E
L1F
+24V
HETERODYNE/PAD/ THRU LINE/AUDIO OSC CONTROL DRIVERS
U12 TTL/VREF
U11 TTL/VREF
U7 TTL/VREF
VREF
J3
W17
A10 J1
HETA IN (L)
HETB IN (L)
30C IN (L)
10 IN (L)
30B IN (L)
20 IN (L)
30A IN (L)
HETA OUT (L)
HETB OUT (L)
30C OUT (L)
10 OUT (L)
30B OUT (L)
20 OUT (L)
30 OUT (L)
AUDIO OSC ENABLE (L)
O8
TO AUDIO OSCILLATOR
A10 W13 800.1 TO 923.5 MHz, -7 TO +15dBm
G5
TO HETERODYNE SECTION
(NOTE 3)
REVERSE POWER LIMITER/DETECTOR
CR1
CR2
R9 10KΩ
VR1 5.11V
VR2 5.11V
C4 0.01μF
C5 0.01μF
L2 0.22μH
FL1
RPI
D14
REVERSE POWER INTERRUPT
A10A6 OUTPUT ASSEMBLY (08656-60002)
A10J4
RPD
REVERSE POWER SENSE
FROM POWER SUPPLY FILTERING
4
T
+5V(F1)
V
-15V(F1)
R92 100KΩ
R93 4220Ω
R94 10KΩ
U10A
R95 3830Ω
A10 J3
(NOTE 4)
REVERSE POWER CLOCK
5K
RCL
U9
FF
RELAY DRIVER
R96 1960Ω
R97 1960Ω

Reference designations within outline (— — —
blies are abbreviated. Full designation includes
Number; e.g., R1 of Assembly A1 is A1R1. Desig
other components are complete as shown.


10dB PAD
30dB PAD B
20dB PAD
30dB PAD A
THRU LINE
10dB PAD IN
30dB PAD B IN
20dB PAD IN
30dB PAD A IN
+24V
S1D
S1E
S1F
S1G
R5 71.15Ω
R8 790Ω
R12 247.5Ω
R15 790Ω
REVERSE POWER LIMITER/DETECTOR
REVERSE POWER RELAY
REVERSE POWER SENSE
RELAY DRIVER
REVERSE POWER INTERRUPT
REVERSE POWER CLOCK
FROM POWER SUPPLY FILTERING
A6 OUTPUT ASSEMBLY (08656-60002)
EXCEPT OPT 002
OPTION 002 ONLY
RF OUTPUT
0.1 TO 990 MHz -127 TO +13 dBm
A10U6,10 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY
A9A1K1 BOTTOM VIEW (NOTE 7)
A6U10 TOP VIEW
A10U3,7,11,12 TOP VIEW
A6U9 TOP VIEW

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. A10 CHASSIS GROUND IS ACHIEVED THROUGH A10J5-1 AND -5 CONNECTIONS AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. A6 AND A9A1 CHASSIS GROUND IS ACHIEVED THROUGH MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
4. SOLENOID PLUNGERS ARE HELD IN PLACE BY PERMANENT MAGNETS.
   IN = HETERODYNE/PAD
   OUT = THRU LINE
5. CAPACITORS C1-3, 6 AND 8 REPRESENT THE CAPACITANCE BETWEEN THE ADJUSTMENT LOOP AND THE ASSOCIATED SERIES RESISTOR R2, 5, 8, 12 OR 15. REFER TO SECTION V FOR ADJUSTMENT PROCEDURES.
6. SERVICE TEST POINT PIN OF DUAL IN-LINE TEST SOCKET J3.
7. A9A1K1 MEASURES APROXIMATLEY 110Ω FROM PIN 1 TO 4.
8. INDICATES CIRCUIT CHANGE. SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A9A1
C23 FL2,3 J2 L1,2 W7,11,13-15,17	C1-8 CR1,2 V1,2 K1 L1 E1-16 VR1,2
A6	A10
J3,4 Q13 R92-97 U9,10	C13,14 J1,3 R52,53 U3,6,7,10-12
A9	
L1 S1	

LOGIC LEVELS

	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATION	PART NUMBERS
A6	
Q13	1853-0007
U9	1820-0309
U10	1826-0013
A10	
U3	1820-1423
U6,10	1820-1730
U7,11,12	1820-2111

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
A6	
U9	+5V(F1) - 14 ▽ - 7
A10	
U8	+5V(F) - 16 ▽ - 8
U6,10	+5V(F) - 20 ▽ - 10
U7,11,12	+24V - 9 ▽ - 8

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

7

P/OA6,A8,P/OA10

Figure 8-63. Attenuator, Attenuator Control and Reverse Power Protection Schematic Diagram

SERVICE SHEET 8
P/O A3 LOW FREQUENCY LOOP ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The Low Frequency Voltage Controlled Oscillator (VCO) and Limiter Amplifier generate, amplify and limit the 60 to 110 MHz signal that is mixed with 800 MHz on the Multiplier Assembly. The TUNE voltage to the VCO is controlled by data from the Microprocessor. The VCO is phase locked to the reference oscillator.

Voltage Controlled Oscillator

The VCO, Q5, is a Hartley Oscillator. The amount of positive feedback from the collector to the emitter is predetermined by the taps on the inductors. The inductors are spiral printed circuit board traces. The +13 Vdc is a clean stable voltage to bias the VCO and Limiter Amplifier circuits.

The base of Q5 is biased by resistor R6 and R8, and the emitter by resistor R9. Inductor L8 suppresses any high frequency oscillations and capacitors C16 and C20 ac couple the signal to the base and emitter of Q5. Capacitors C16 and C23 are by-pass capacitors.

The 60 to 110 MHz output is dependent on the TUNE voltage. The output is ac coupled by C25 to Linear Amplifier Q6.

Linear Amplifier

The base of Q6 is biased by resistors R10 and R11, and the emitter by R13 and R14. R13 supplies some negative feedback but R14 does not since it is by-passed by C28. The inductive bead E1 reduces gain at high frequencies.

The output of Q6 is dc coupled to buffer amplifier limiter Q7. The bias voltages of Q7 are set by Q6. Feedback from the collector to base of Q7 is by diodes CR2 and 3 and capacitor C29. The diodes limit the feedback and restrict the collector voltage swing to ±0.6V to provide a constant output level.

The output of the Limiter Amplifier is ac coupled by capacitor C32 to the VCO Buffer Q8 shown on Service Sheet 9 and by capacitor C34 to the 110 MHz Low-Pass Filter. Resistors R4, R5 and R7 form a 2 dB pad whichs isolates the amplifier from the 110 MHz Low-Pass Filter. This makes the filter impedance nearer 50Ω at all VCO frequencies.

110 MHz Low-Pass Filter

Capacitor C31 and inductor L17 form a series resonant circuit. At resonance, R15 and R16 reduce the series impedance for increased output. This is tuned to vary the output level at 110 MHz (flatness). The filter passes 60 to 110 MHz and rejects 120 MHz and above.

SERVICE SHEET 8 (Cont'd)

TROUBLESHOOTING

Procedures for checking circuits of the A3 Low Frequency Loop Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g. ⟨√1⟩. Fixed voltages are shown on the schematic inside a hexagon e.g. ⟨2V±0.2V⟩. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Power Meter	HP 436A
Power Sensor	HP 8482A
Frequency Counter	HP 5328A
Adapter Probe	HP 1250-1598
Adapter, Coaxial Type-N female to BNC male	HP 1250-0077
Adapter, Coaxial BNC female to BNC female	HP 1250-0080
Cable, BNC male to SMC female	HP 08662-60080

SERVICE SHEET 8 (Cont'd)

⟨√1⟩ Voltaged Controlled Oscillator, Limiter Amplifier and 110 MHz Low-Pass Filter

1. Set the Signal Generator to −10 dBm at 80 MHz with no modulation.

2. Change the frequency to 90 MHz. This ensures the frequency of the Low Frequency Loop VCO will be 60 MHz.

3. Check the following levels at the frequencies indicated in Table 1.

NOTES

When probing the oscillator with the covers removed, a frequency shift may be introduced.

Covers for the oscillator must be installed so that the lip on the bottom cover makes a good contact with the ground plane on the printed circuit board.

Table 1. VCO Frequency, Power Output and TUNE Voltage

Frequency (MHz)		VCO Tune Voltage (Vdc)	Power Level (dBm)	
Front Panel Setting	VCO Output (at TP6)		at TP6	at J4
90	60	+11.0 to +9.0	+6.8 to +4.8	−7.7 to −9.7
85	65	+10.0 to +8.0	+7.0 to +5.0	−7.5 to −9.5
80	70	+9.0 to +7.0	+7.0 to +5.0	−7.3 to −9.3
75	75	+9.0 to +5.0	+7.2 to +5.2	−7.3 to −9.3
70	80	+8.0 to +4.0	+6.5 to +4.5	−7.1 to −9.1
65	85	+7.0 to +3.0	+6.2 to +4.2	−7.0 to −9.0
60	90	+6.0 to +2.0	+5.9 to +3.9	−7.0 to −9.0
55	95	+6.0 to 0.0	+5.7 to +3.7	−7.2 to −9.2
50	100	+5.0 to −1.0	+6.0 to +4.0	−7.8 to −9.8
45	105	+4.0 to −2.0	+6.2 to +4.2	−8.0 to −10.0
40	110	+2.5 to −3.5	+5.8 to +3.8	−8.4 to −10.4

◀ Attenuator, Attenuator Control
and Reverse Power Protection
P/O A6, A9A1, P/O A10
SERVICE SHEET 7

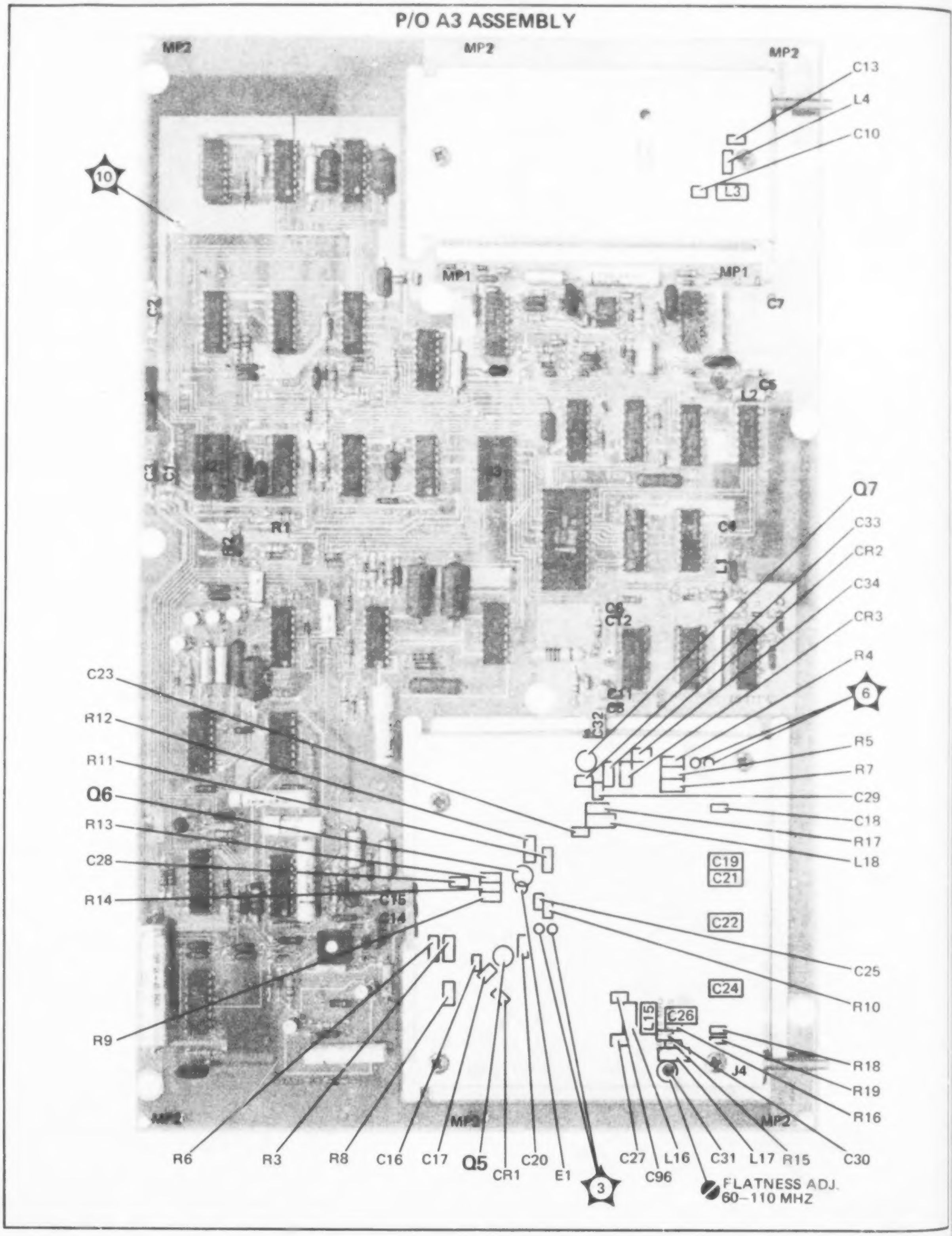

P/O A3 ASSEMBLY
MP2
MP2
MP2
C13
L4
C10
L3
10
MP1
MP1
C7
C2
C5
L2
C3
C1
R1
R2
C4
L1
C8
C12
C11
C32
Q7
C33
CR2
C34
CR3
R4
6
R5
R7
C29
C18
R17
L18
C19
C21
C22
C25
C24
R10
L15
C26
J4
R18
R19
R16
C23
R12
R11
Q6
R13
C28
R14
C15
C14
R9
MP2
MP3
MP2
R6
R3
R8
C16
C17
Q5
CR1
C20
E1
3
C27
C96
L16
C31
L17
R15
C30
FLATNESS ADJ.
60–110 MHZ

Figure 8-64. LF Loop VCO Component Locations

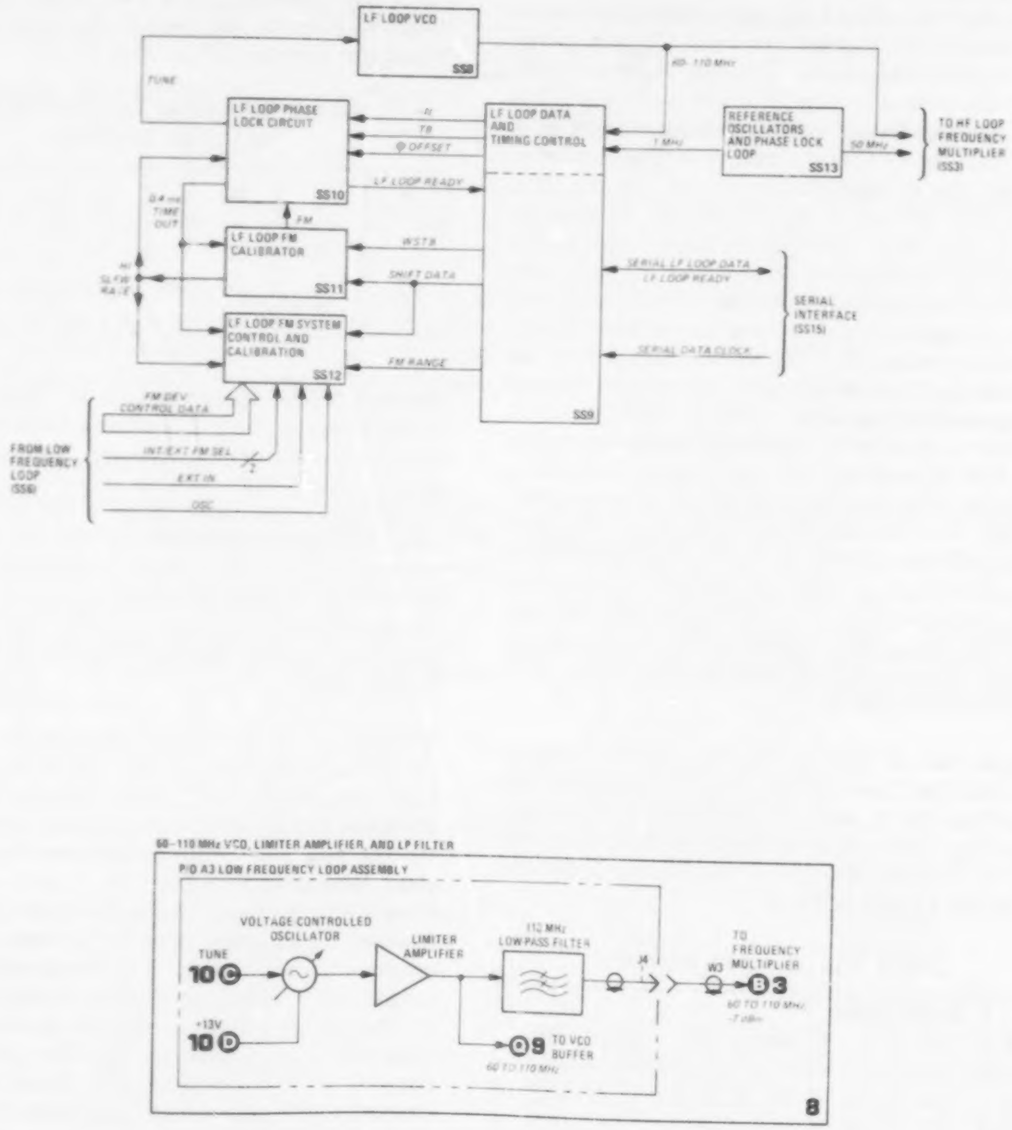
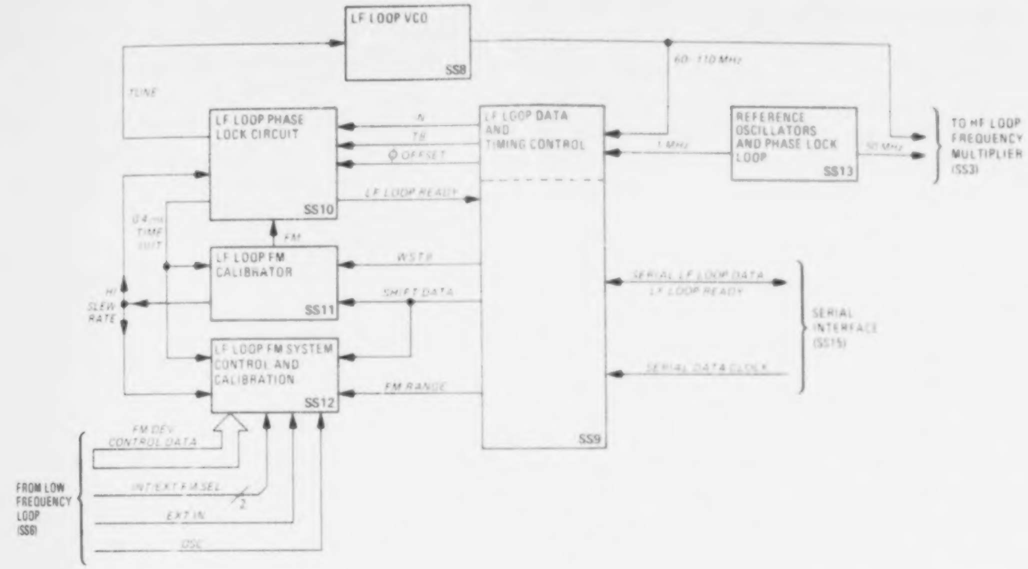

LF LOOP VCO
SS8
TUNE
60–110 MHz
LF LOOP PHASE LOCK CIRCUIT
SS10
N
TB
Φ OFFSET
LF LOOP READY
LF LOOP DATA AND TIMING CONTROL
SS9
REFERENCE OSCILLATORS AND PHASE LOCK LOOP
SS13
1 MHz
50 MHz
TO HF LOOP FREQUENCY MULTIPLIER (SS3)
0.4 ms TIME OUT
FM
LF LOOP FM CALIBRATOR
SS11
WSTB
SHIFT DATA
HI SLEW RATE
LF LOOP FM SYSTEM CONTROL AND CALIBRATION
SS12
FM RANGE
SERIAL LF LOOP DATA
LF LOOP READY
SERIAL INTERFACE (SS15)
SERIAL DATA CLOCK
FM DEV CONTROL DATA
INT/EXT FM SEL
2
EXT IN
OSC
FROM LOW FREQUENCY LOOP (SS6)
60–110 MHz VCO, LIMITER AMPLIFIER, AND LP FILTER
P/O A3 LOW FREQUENCY LOOP ASSEMBLY
VOLTAGE CONTROLLED OSCILLATOR
TUNE
10 C
+13V
10 D
LIMITER AMPLIFIER
112 MHz LOW PASS FILTER
J4
W3
TO FREQUENCY MULTIPLIER
B 3
60 TO 110 MHz
-7 dBm
Q 9
TO VCO BUFFER
60 TO 110 MHz
8

Figure 8-65. LF Loop VCO Block Diagrams


LF LOOP VCO
SS8
60–110 MHz
TUNE
LF LOOP PHASE LOCK CIRCUIT
SS10
N
TB
Φ OFFSET
LF LOOP DATA AND TIMING CONTROL
1 MHz
REFERENCE OSCILLATORS AND PHASE LOCK LOOP
SS13
50 MHz
TO HF LOOP FREQUENCY MULTIPLIER (SS3)
LF LOOP READY
0.4 ms TIME OUT
FM
LF LOOP FM CALIBRATOR
SS11
WSTB
SHIFT DATA
HI SLEW RATE
LF LOOP FM SYSTEM CONTROL AND CALIBRATION
SS12
FM RANGE
SERIAL LF LOOP DATA
LF LOOP READY
SERIAL INTERFACE (SS15)
SERIAL DATA CLOCK
SS9
FM DEV CONTROL DATA
INT/EXT FM SEL
2
EXT IN
OSC
FROM LOW FREQUENCY LOOP (SS6)

60–110 MHz VCO, LIMITER AMPLIFIER, AND LP FILTER

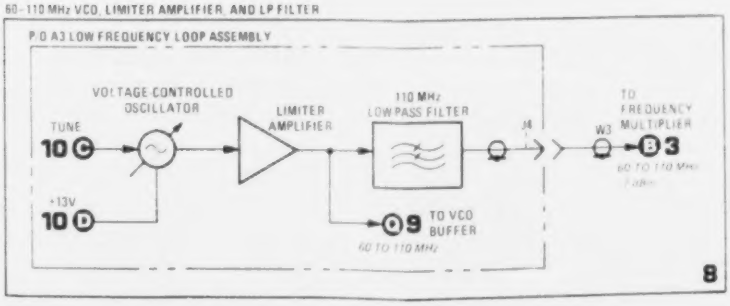
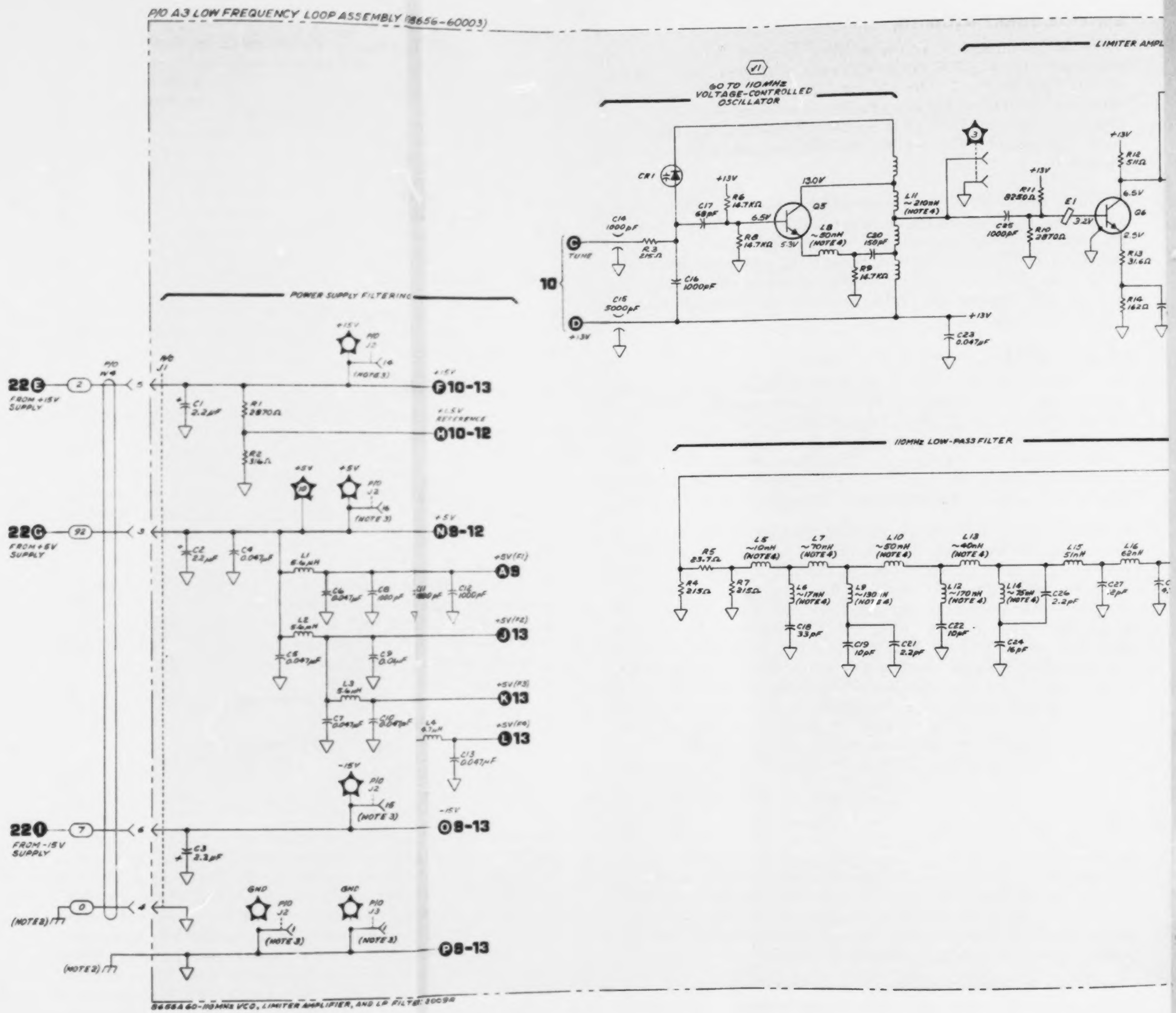
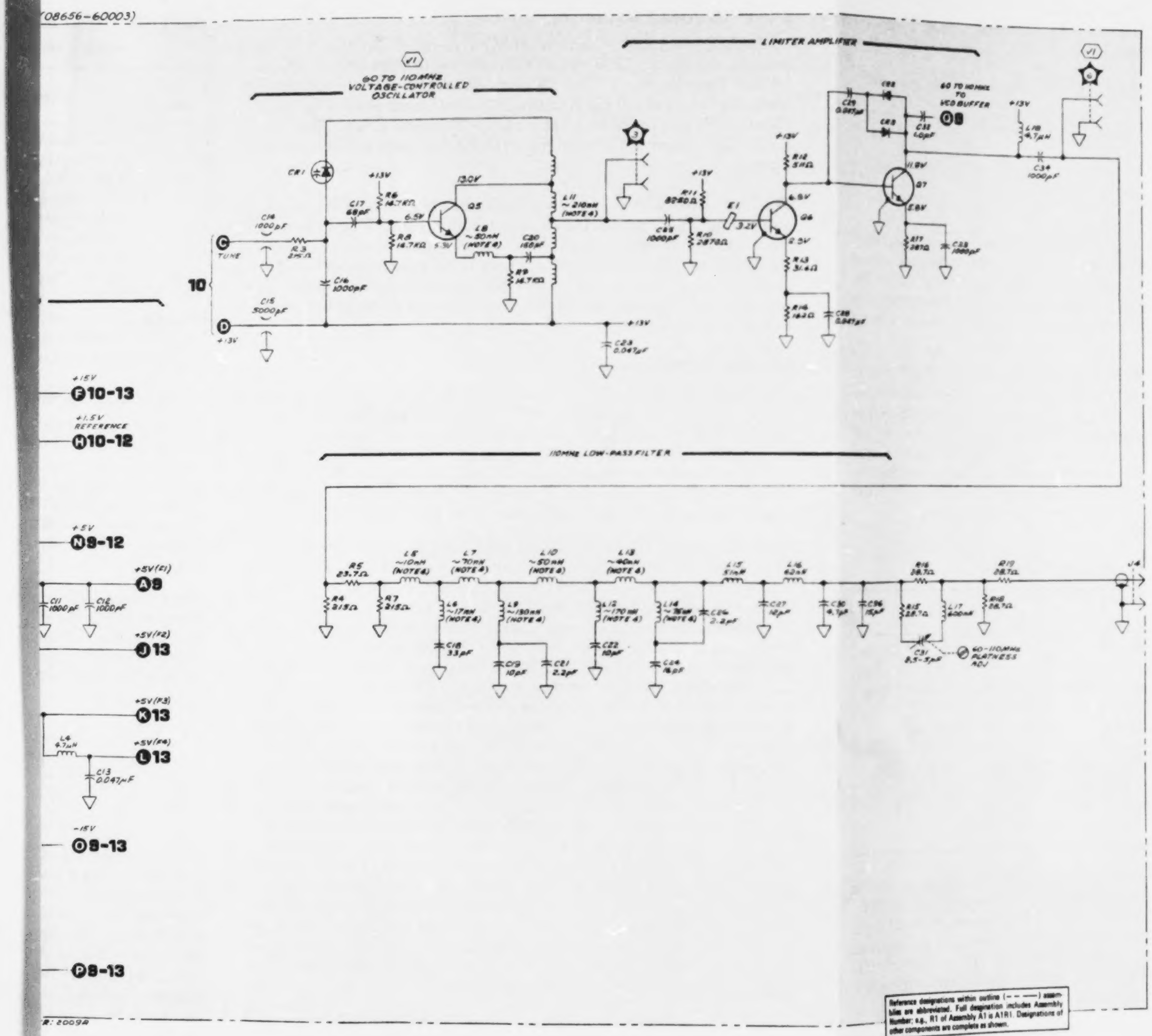

P/O A3 LOW FREQUENCY LOOP ASSEMBLY
VOLTAGE-CONTROLLED OSCILLATOR
TUNE
10 Ⓒ
+13V
10 Ⓓ
LIMITER AMPLIFIER
110 MHz LOW PASS FILTER
J4
W3
TO FREQUENCY MULTIPLIER
Ⓑ 3
60 TO 110 MHz
7 dBm
9
TO VCO BUFFER
60 TO 110 MHz
8

Figure 8-65. LF Loop VCO Block Diagrams


P/O A3 LOW FREQUENCY LOOP ASSEMBLY (8656-60003)
V1
60 TO 110MHz VOLTAGE-CONTROLLED OSCILLATOR
LIMITER AMPL
CR1
+13V
R6 14.7KΩ
C17 68pF
13.0V
Q5
6.5V
5.3V
R8 14.7KΩ
L8 ~50nH (NOTE 4)
C20 150pF
R9 14.7KΩ
L11 ~210nH (NOTE 4)
C14 1000pF
R3 215Ω
C16 1000pF
C15 5000pF
C TUNE
D +13V
10
C23 0.047µF
+13V
3
R11 8250Ω
R10 2870Ω
C25 1000pF
E1
3.2V
Q6
R12 511Ω
6.5V
2.5V
R13 31.6Ω
R14 162Ω
110MHz LOW-PASS FILTER
R5 23.7Ω
R4 215Ω
R7 215Ω
L5 ~10nH (NOTE 4)
L6 ~17nH (NOTE 4)
C18 33pF
L7 ~70nH (NOTE 4)
L9 ~130nH (NOTE 4)
C19 10pF
C21 2.2pF
L10 ~50nH (NOTE 4)
L12 ~170nH (NOTE 4)
C22 10pF
L13 ~40nH (NOTE 4)
L14 ~75nH (NOTE 4)
C24 16pF
C26 2.2pF
L15 51nH
C27 .2pF
L16 62nH
POWER SUPPLY FILTERING
22 E FROM +15V SUPPLY
2
P/O W4
P/O J1
5
C1 2.2µF
R1 2870Ω
R2 316Ω
+15V
P/O J2
16
(NOTE 3)
+15V
F 10-13
+1.5V REFERENCE
H 10-12
22 C FROM +5V SUPPLY
92
3
C2 2.2µF
C4 0.047µF
+5V
10
+5V
P/O J2
16
(NOTE 3)
+5V
N 8-12
L1 5.6µH
C6 0.047µF
C8 1000pF
C11 1000pF
C12 1000pF
+5V(F1)
A 8
L2 5.6µH
C5 0.047µF
C9 0.01µF
+5V(F2)
J 13
L3 5.6µH
C7 0.047µF
C10 0.047µF
+5V(F3)
K 13
L4 4.7µH
C13 0.047µF
+5V(F4)
L 13
-15V
P/O J2
16
(NOTE 3)
-15V
O 8-13
22 I FROM -15V SUPPLY
7
6
C3 2.2µF
0
4
(NOTE 2)
GND
P/O J2
1
(NOTE 3)
GND
P/O J3
(NOTE 3)
P 8-13
(NOTE 2)
8656A 60-110MHz VCO, LIMITER AMPLIFIER, AND LP FILTER 30094


(08656-60003)
V1
60 TO 110MHZ VOLTAGE-CONTROLLED OSCILLATOR
LIMITER AMPLIFIER
110MHz LOW-PASS FILTER
10
C
TUNE
D
+13V
C14 1000pF
R3 215Ω
C15 5000pF
CR1
C16 1000pF
C17 68pF
+13V
R6 14.7KΩ
6.5V
R8 14.7KΩ
13.0V
Q5
5.3V
L8 ~50nH (NOTE 4)
C20 160pF
R9 14.7KΩ
L11 ~210nH (NOTE 4)
+13V
C23 0.047μF
3
+13V
R11 8250Ω
C85 1000pF
R10 2870Ω
E1
3.2V
+13V
R12 51Ω
6.9V
Q6
2.5V
R13 31.6Ω
R14 162Ω
C88 0.047μF
C29 0.047μF
CR2
CR3
C32 1.0pF
60 TO 110MHz TO VCO BUFFER
8
11.8V
Q7
5.8V
R17 287Ω
C33 1000pF
+13V
L18 4.7μH
C34 1000pF
V1
6
R5 23.7Ω
R4 215Ω
R7 215Ω
L5 ~10nH (NOTE 4)
L6 ~17nH (NOTE 4)
C18 33pF
L7 ~70nH (NOTE 4)
L9 ~130nH (NOTE 4)
C19 10pF
C21 2.2pF
L10 ~50nH (NOTE 4)
L12 ~170nH (NOTE 4)
C22 10pF
L13 ~40nH (NOTE 4)
L14 ~35nH (NOTE 4)
C24 16pF
C26 2.2pF
L15 51nH
C27 12pF
L16 62nH
C30 4.7pF
C96 15pF
R16 28.7Ω
R15 28.7Ω
L17 600nH
C31 0.5-3pF
60-110MHz FLATNESS ADJ
R19 28.7Ω
R18 28.7Ω
J4
V1
P/O W3
60 TO 110 MHz, -7dBm TO FREQUENCY MULTIPLIER
B3
+15V
F10-13
+1.5V REFERENCE
H10-12
+5V
N9-12
+5V(F1)
A9
C11 1000pF
C12 1000pF
+5V(F2)
J13
+5V(F3)
K13
L4 4.7μH
+5V(F4)
L13
C13 0.047μF
-15V
O9-13
P8-13
R: 2009A

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A3J1-4 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKET J2 OR J3.
4. PRINTED CIRCUIT TRACE INDUCTOR.

REFERENCE DESIGNATIONS

NO PREFIX	A3 CONT.
W3, 4	L1-18 Q5-7 R1-19 TP3, 6, 10
A3	
C1-34, 96 CR1-3 E1 J1-4	

TRANSISTOR PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q5 Q6 Q7	1854-0610 1854-0345 1854-0696

8
P/O A3

Figure 8-66. LF Loop VCO Schematic Diagram

SERVICE SHEET 9
P/O A3 LOW FREQUENCY LOOP ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

Inputs to the divider circuits shown on Service Sheet 9 are from the Low Frequency Loop Voltage Controlled Oscillator (VCO) output and the 1 MHz reference signal (divided from 50 MHz). The 60 to 110 MHz VCO signal is divided-by-N to 100 or 250 Hz. The 1 MHz signal is divided to 100 or 250 Hz in Counter 1 of the Triple Programmable Counter. These signals, ÷N and TB, are phase compared in circuits shown on Service Sheet 10.

Counter No. 1 divides the 60 to 110 MHz VCO signal by 16. For each 100 Hz change in the LF Loop output frequency, the data bits to U23 change by 1. Counter No. 2 divides the output of Counter No. 1 by 16. For each 1600 Hz change in the LF Loop output frequency, the data bits to U27 change by 1. Changes in steps of 25.6 kHz (16 x 16 x 100 Hz) do not affect Counters No. 1 and 2. For a 25.6 kHz frequency step, data is written to Counter 0 (P/O U20) only. Because of the RF divider circuits in the Output Section (refer to Service Sheet 4), the RF output frequencies do not seem to correlate with the output of the Low Frequency Loop. Refer to Table 1 for more information.

Table 1. RF Output Versus LF Loop Output Frequencies

Output Divider Mode	RF Frequencies					LF Loop Frequencies					
	Output (MHz)	LF Loop Band (MHz)	High Slew Rate Band kHz)	Counter Resolution		Output (MHz)	LF Loop Band (MHz)	High Slew Rate Band (kHz)	Counter Resolution		Counter Data Change
				#1 (kHz)	#2 (kHz)				#1 (kHz)	#2 (kHz)	
÷1/Heterodyne	0.1-123.5	50	25.6	0.1	1.6	60-110	50	25.6	0.1	1.6	1
÷4	123.5-247	12.5	6.65	0.1	1.6	60-110	50	25.6	0.4	6.4	4
÷2	247-494	25	13.3	0.1	1.6	60-110	50	25.6	0.2	3.2	2
÷1	494-990	50	25.6	0.1	1.6	60-110	50	25.6	0.1	1.6	1

At the end of the ÷N count cycle, a pulse is output from Counter 0. This pulse clocks the Terminal Count Flip-Flop. The resulting output enables the terminal count gate U14A with a high at pin 2 and resets U31A with a low at pin 1. This allows the next clock transition from Counter No. 2 to be gated to the ÷N output instead of the input to Counter 0. Therefore, a 0.5 ms window is opened every 10 ms (100 Hz) or 4 ms (250 Hz) which allows Counter No. 2's terminal count to become the terminal count of the entire ÷N Counter.

The ÷N pulse is used to load Counter No. 2 U27 directly. It also passes through level translator U30B and C to set the Reload Transient Blocking Flip-Flop No. 1 U26A which halts the clock pulse to Counter No. 2. The effect of setting U26A tries to place a low at U26B-Pin 10. The terminal count output of Counter No. 1 U23-Pin 4 overrides this and holds the input high. When the terminal count of Counter No. 1 is reached, the low at U26B-Pin 10 is transferred to U26B-Pin 15 which reloads Counter No. 1. The ÷N terminal count pulse is cut short when the low at the D input to the Terminal Count Reset Flip-Flop U28-Pin 2 is clocked through to reset the Terminal Count Flip-Flop U31B. The output of Counter No. 2 is switched back to the input of Counter 0.

The high used to set U26A is removed when the ÷N terminal count pulse ends. This enables the clock to Counter No. 2. When Counter No. 1 was reloaded, the output at pin 4 goes high replacing a high at U26B-Pin 10. The active-high output of U26B goes high on the first clock pulse which allows Counter No. 1 to begin counting on the second pulse. The counters again count up to the ÷N terminal count and the cycle repeats.

LF Loop Shift Registers

The serial LF Loop Data bus is pulsed low for approximately 0.5 ms every 10 ms or 4 ms (depending on the frequency resolution, 100 Hz or 250 Hz). This tells the Microprocessor that the Low Frequency Loop is ready to receive data. If the Microprocessor has data to write to the LF Loop Assembly, 9.5 ms is the time allowed in the 100 Hz frequency resolution mode and 3.5 ms in the 250 Hz frequency resolution mode starting at the termination of the LF Loop Ready pulse.

Serial LF Loop Data written to the LF Loop consists of control and data words for the Triple Programmable Counter U20 and data words for Counters No. 1 and No. 2, U23 and U27. Refer to Table 2. There are eight sixteen bit control and data words that are written to the Low Frequency Loop Assembly. They are clocked into U24A, B and U25A by the LF Loop Clock. Only the last twelve bits of each sixteen bit words are used. Each word consists of 4 blank, 4 control and 8 data bits. All eight words are written to the LF Loop when the instrument is RESET or when line power voltage is connected to the Signal Generator and it goes through the power up routine. In all other cases, control words 1, 3, and 5 are not written to the LF Loop Assembly. Data words 2 and 4 are written whenever the frequency resolution is changed from 100 Hz to 250 Hz or 250 Hz to 100 Hz. Data words 6 and 7 are written when the LF VCO frequency goes beyond the 25.6 kHz band edge. LF Loop data word 8 is left latched into shift registers U24A, B and U25A. The four most significant data bits (from U24B) are loaded into U27 Counter No. 2 and the four least significant bits (from U24A) are loaded into U23 Counter No. 1. Counters No. 1 and No. 2 and Counter 0 of the Triple Programmable Counter are all part of the ÷N Counter. These circuits are used to divide the LF Loop VCO to provide an output with 100 and 250 Hz resolution. This output is phase compared with the time base TB signal to phase lock the Low Frequency Loop.

Control bits 9 through 12 are clocked into U25A. These select special functions and the counter within the Triple Programmable Counter that is to receive data. Bit 12 of LFWRD 8 selects the FM range of 0 to 10 kHz or 11 to 99 kHz. Bit 11 resets D Flip Flop U28B whose active-low output, when low, lets data be written into the Triple Programmable

Table 2. Lo

LF Word	F
1	Time Base (
2	Time Base I
3	Phase Offse
4	Phase Offse
5	Divide-by-N
6	Divide-by-N
7	Divide-by-N
8	Divide-by-N

Counter and trigger
on Service Sheet 11.
U20 receives the dat

Write Strobe Gene

The Write Strobe G
Triple Programmat
the counters and t
frequency change.
quency change is g
crosses into anothe
is reset or first conn
Figure 1.

The LF Loop Clock
triggers the Write
active-high output
About 75 μs after th
its inactive state, a

Pin
H
H

The inactive state o
low high which pla
be clocked high as
removed. Whenever
Counter U20 (the Si
changes or the LF
data bit 11 from reg
removed. When U2
data word ends, the
clocks U28B with t
low output going l
data stored in the re
Counter. Which co

Table 2. Low Frequency Loop Data and Control Words

LF Word	Function	Written to Counter(s)
1	Time Base Control	U20 Counter 1
2	Time Base Data	U20 Counter 1
3	Phase Offset Control	U20 Counter 2
4	Phase Offset Data	U20 Counter 2
5	Divide-by-N Control	U20 Counter 0
6	Divide-by-N Data	U20 Counter 0
7	Divide-by-N Data	U20 Counter 0
8	Divide-by-N Data	Counters No. 1 and 2

Counter and triggers the High Slew Rate Monostable U21B shown on Service Sheet 11. Bits 9 and 10, A0 and A1, select which counter of U20 receives the data.

Write Strobe Generator

The Write Strobe Generator U21A and U28B is used to enable the Triple Programmable Counter when data is to be written to one of the counters and to enable the LF Loop circuits for the coming frequency change. The Generator is triggered if a LF Loop frequency change is greater that 25.6 kHz, if the LF Loop frequency crosses into another 25.6 kHz band and when the Signal Generator is reset or first connected to line power. Refer to Tables 3 and 4 and Figure 1.

The LF Loop Clock clocks in each of the 16 bit serial data words and triggers the Write Strobe Generator monostable U21A with the active-high output going high and the active-low output going low. About 75 μs after the last clock pulse of each word, U21A returns to its inactive state, active-high low and active-low high.

Table 3. U21A Operation

Pin 3	Pin 1	Pin 2	Pin 13	Pin 4
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔

The inactive state of the U28B is active-high output low and active-low high which places a high on the D-input. Thus U28B is ready to be clocked high as soon as the low on the Reset input pin-13 is removed. Whenever data is to be written to the Triple Programmable Counter U20 (the Signal Generator is RESET, frequency resolution changes or the LF Loop frequency crosses a 25.6 kHz bandedge), data bit 11 from register U25A is high and the reset input to U28B is removed. When U21A returns to its inactive state, 75 μs after the data word ends, the U21A active-low output's low to high transition clocks U28B with the active-high output going high and the active-low output going low. The active-low output enables the LF Word data stored in the registers to be written to the Triple Programmable Counter. Which counter receives the data is determined by data bits

9 and 10, A0 and A1. The high at U28B's active-high output is coupled back to U21A-Pin 1. The pulse passes through the differentiator C37 and R25. This shortens the pulse to about 1 μs. At this time (between LF Data Words) U21A-Pin 2 is high. This means that U21A is set immediately. 75 μs later U21A returns to the reset condition which again clocks and resets U28B. This action ends the Triple Programmable Counter load enable and WSTR(L) signal. This process is repeated for each data word that is written to the Triple Programmable Counter.

Table 4. U28B Operation

R	S	C	D	Pin 9	Pin 8	Remarks
H	H	↑	H	H	L	Frequency change passes 25.6 kHz band edge.
H	H	↑	L	L	H	
L	H	X	X	L	H	Frequency change does not pass 25.6 kHz band edge

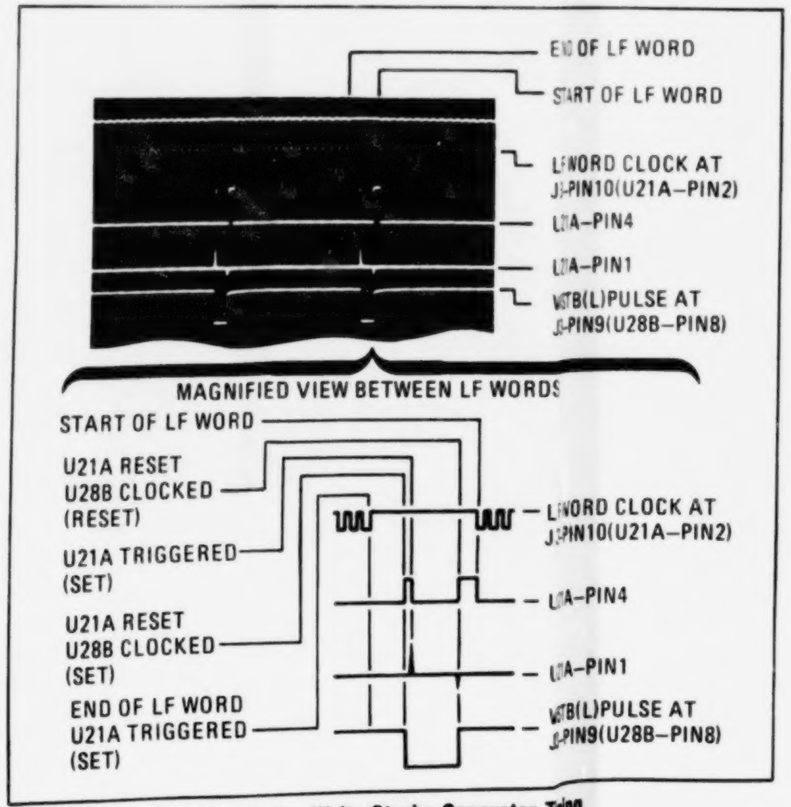

END OF LF WORD
START OF LF WORD
LF WORD CLOCK AT J-PIN10(U21A–PIN2)
U21A–PIN4
U21A–PIN1
WSTB(L)PULSE AT J-PIN9(U28B–PIN8)
MAGNIFIED VIEW BETWEEN LF WORDS
START OF LF WORD
U21A RESET U28B CLOCKED (RESET)
U21A TRIGGERED (SET)
U21A RESET U28B CLOCKED (SET)
END OF LF WORD U21A TRIGGERED (SET)
LF WORD CLOCK AT J-PIN10(U21A–PIN2)
U21A–PIN4
U21A–PIN1
WSTB(L)PULSE AT J-PIN9(U28B–PIN8)

Figure 1. Write Strobe Generator Timing

If data is not to be written to the Triple Programmable Counter, U20, data bit 11 is not set high and the reset input of U28B is held low and the outputs are never changed. The LF Loop will not enter the High Slew Rate mode since it is also dependent on the active-low output, that is WSTR(L), being low.

Divide-By-N Circuits

Counter No. 1. The 60 to 110 MHz signal from the VCO is applied to VCO Buffer Q8 to isolate the VCO from Reset Enable Reclock Flip-Flop U26B (refer to Table 5) and Counter No. 1 U23. The wired OR to the D2 input U26B pin 10 are traces on the PC board. Any high from the active-low output of U26A, B or terminal count output U23 pin 4 will provide a high to the D2 input of U26B. Therefore, when U26B is clocked by the VCO input, the active-high output goes high and the active-low output low. The active-high output's high to Counter No. 1 pin 5 enables the counter to count. Counter No. 1 (refer to Table 6) is a binary counter and divides the VCO clock frequency by 16. The terminal count at pin 4 goes low when the counter has counted to binary 15 (HHHH). The divide-by-16 output from Counter No. 1 is applied to the Reload Transient Blanking Flip-Flop No. 1 U26A (refer to Table 7) and to Counter No. 2 (refer to Table 8) through the level translator U30D and Q10.

Table 5. U26B Reset Enable Reclock Flip-Flop Operation

R	S	C2	Cc	D2	Pin 15	Pin 14
L	L	↑	L	L	L	H
L	L	↑	L	H	H	L

Table 6. U23 Counter No. 1 Operation

CE	PE	MR	CP	Remarks
L	L	L	↑	Load Parallel
L	H	L	↑	Count

Table 7. U26A Reload Transient Blanking Flip-Flop No. 1

R	S	C1	Cc	D1	Pin 2	Pin 3
L	L	↑	L	L	L	H
L	H	X	L	L	H	L

On the VCO clock pulse to Counter No. 1 that clocks the binary 15 Count, the terminal count at pin 4 goes low. The active-low output of U26B is also low but the active-low output of U26A is high so the D2 input of U26B remains high. The active-high output remains high and disables the parallel load of U23 of the data bits in Shift Register U24A. At this point, the divide-by-16 cycle starts over. When the output of Counter No. 1 goes high, it will be high for half the divide-

Low Frequency Loop
Voltage Controlled Oscillator (VCO)

SERVICE SHEET 9 (Cont'd)

by-16 cycle. One input to U30D is high when bit eight of Counter No. 1 goes high. The other input is set low since a low-to-high transition input to U26A sets the active-high output low. The active-high output will remain low until U26A is set by the ÷N terminal count. With one input to U30D high, the output at pin 15 is low and at pin 9 is high. The inputs are coupled to the base and emitter of ECL-to-TTL Translator Q10. The emitter of Q10 will be at approximately +4.2 Vdc, an ECL high, and the anode of CR4 will be at approximately +3.3 Vdc. CR4 will be biased on and the base of Q10 will be at approximately +2.7 Vdc, also on. With Ql0 turned on heavily, its collector voltage will approximately equal the emitter voltage. When the output of Counter No. 1 goes low, the input to pin 13 of U30D goes low and its outputs change to +3.3 Vdc at pin 9 and +4.2 Vdc at pin 15. Therefore, the anode of CR4 will be approximately +4.2 Vdc (biased on) and the base of Q10 will be +3.6 Vdc. The emitter of Q10 will be at approximately +3.3 Vdc and Q10 is biased off. (With Q10 biased off the collector will go to approximately 0 Vdc.) The ECL 3.3 Vdc low and 4.2 Vdc high has been changed to a TTL level (+0.8 Vdc low and +2.0 Vdc high). The signal at J3 pin 2 is a poorly shaped square wave whose frequency is the VCO frequency divided-by-16.

Counter No. 2. ECL-to-TTL Translator output is the clock for Counter No. 2, for Reload Blanking Flip-Flop No. 2, and for Terminal Count Reset Flip-Flop U28A. Refer to Tables 8 and 9 for operation of Counter No. 2 and the Reload Transient Blanking Flip-Flop No. 2.

Table 8. U27 Counter No. 2 Operation

R	Enable P	Enable T	Load	Clk	Counter Mode
H	H	H	H	↑	Count
H	H	H	L	↑	Load Data

Counter No. 2 is a synchronous programmable binary counter. When pin 9 is low data is loaded. When it is high the counter is counted up on each clock pulse low-to-high transition. The counter output at pin 15, the ripple carry output, goes high at binary 15. Therefore, when pin 9 is low the four most significant bits latched into U24B are clocked into Counter No. 2. On each successive low to high transition of the clock the counter counts up by one.

The ripple carry output is pulsed high for appro imately 20 µs when the counter reaches 15. Ther fore, the counter divides-by-16 except on the fir count cycle after the input data has been loade Data is loaded every 10 or 4 ms. The output pulse from the counter are clocked through the Reloa Transient Blanking Flip Flop No. 2.

Table 9. U31A Reload Transient Blanking Flip-Flop No. 2 Operation

R	S	D1	C	Pin 5	Pin 6
L	H	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L

Counter 0. The output pulses of U31A clock the Triple Programmable Counter's Counter 0 on the low-to-high transition (positive going edge of pulse). The output of this counter triggers the Terminal Count Flip-Flop at a 100 Hz or 250 Hz rate. This sets a window for the ÷N pulse from Counter No. 2. The ÷N signal is compared with the TB 100 Hz or 250 Hz output of Triple Programmable Counter's Counter 1. TB is 1 MHz divided from the 50 MHz reference oscillator shown on Service Sheet 13.

With the reset input high, the 100 Hz or 250 Hz clock from Counter 0 clocks U31B on the low-to-high transition setting the active-high output high and the active-low output low. Refer to Table 10. The active-low output resets the Reload Transient Blanking Flip-Flop No. 2 and prevents it from being clocked. The active-high output high enables U14A every 10 or 4 ms which allows the output of Counter No. 2 to be gated to the ÷N output. This pulse is applied to U17B of the Phase to Charge Converter shown on Service Sheet 10 where it is compared to TB. The pulse is also coupled to the D input of U28A. The D input low is clocked to the active-high output by the output of Q10 which is equivalent to the output of Counter No. 1. When the active-high output of U28A is set low it resets U31B. The active-low output of U31B being high enables U31A to be clocked again. During this time the low output of U14A sets U27-Pin 9 Counter No. 2 low and it is reloaded on the same clock pulse that clocked U28A. The low output of Ul4A is coupled to the TTL-to-ECL Translator of VRl, CR7, R28 and R29 changing the input to U30B and C to a ECL high (greater than +4.2 Vdc). This changes the set input to U26A to a high

SERVICE SHEET 9 (Cont'd)

which changes the active-high output to a high and the active-low output to a low. This enables the D input to U26B so that when the carry output of Counter No. 1 goes low, Counter No. 1 is reloaded with the data stored in shift register U24A on the next VCO clock pulse.

Table 10. U31B Terminal Count Flip-Flop Operation

R	S	D	C	Pin 9	Pin 8
L	H	X	X	L	H
H	H	H	↑	H	L

Triple Programmable Counter's Counter 2 is clocked by the same 1 MHz as the Counter 1 and supplies a 20 μs pulse every 10 ms or 4 ms to U13D of the Phase to Charge Converter (refer to Service Sheet 10).

TROUBLESHOOTING

Procedures for checking the circuits of the A3 Low Frequency Loop Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g., ⟨√1⟩. Fixed voltages are shown on the schematic inside a hexagon, e.g., ⟨2V±0.2V⟩. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Frequency Counter	HP 5328A
Oscilloscope	
Storage Mainframe	HP 181A
Vertical Amplifier	HP 1801A
Time Base	HP 1820C

⟨√1⟩ Reset Enable Reclock Flip-Flop, Counter No. 1

1. Set the Signal Generators frequency to 80 MHz.

2. Set the Signal Generator to −10 dBm at 90 MHz without modulation.

NOTE

It is necessary to include step 1 so that the Low Frequency Loop frequency will be set to 60 MHz.

3. Check the frequencies and voltage levels shown in Table 11.

4. Check the waveforms for TP4, TP5 and J3-pin 2. Refer to Figures 2, 3 and 4. The frequency of the Signal Generator is 90 MHz and the VCO frequency is 60 MHz. Measurements are made using a 1:1 probe.

Table 11. Counter No. 1 Signals versus LF Loop Frequency

Frequency (MHz)			TTL Level at U23-Pins			
Signal Generator Output	LF Loop VCO Output at A3TP4	Output of Counter No. 1 at A3TP5 or J3-Pin 2	11	10	9	7
90.0000	60.0000	3.7500	L	L	L	H
80.0000	70.0000	4.3750	L	L	L	H
60.0000	90.0000	5.6250	L	L	L	H
50.0000	100.0000	6.2500	L	L	L	H
49.5000	100.5000	6.2813	H	L	L	H
49.0000	101.0000	6.3125	L	L	L	H
46.5555	103.4445	6.4653	L	H	L	L
46.5000	103.5000	6.4688	H	L	L	H
46.0555	103.9445	6.4966	H	H	L	L
46.0055	103.9945	6.4997	H	L	L	L
46.0050	103.9950	6.4997	L	L	H	H

SERVICE SHEET 9 (Cont'd)

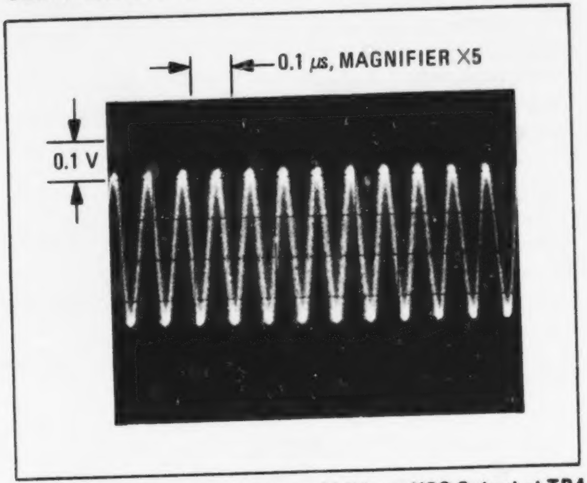


Figure 2. Oscilloscope Display of LF Loop VCO Output at TP4 (with ac coupling and internal triggering)

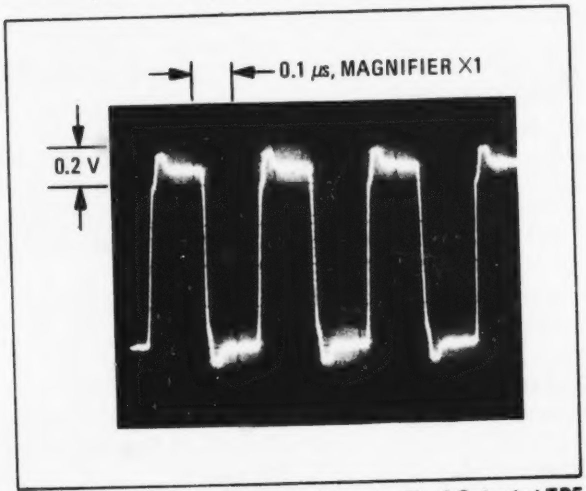


Figure 3. Oscilloscope Display of Counter No. 1 Output at TP5 (with ac coupling and internal triggering)

√2 Counter No. 2, Reload Transient Blanking Flip-Flop No. 2, P/O Triple Programmable Counter and Terminal Count Flip-Flop

1. Set the Signal Generator's frequency to 80 MHz. This allows 90 MHz to be set from a lower frequency.

2. Set the Signal Generator to -10 dB at 90 MHz without modulation.

3. Check the frequencies and voltage levels shown on Table 12. The frequency at J3-Pin 3 may be hard to count due to pulse width. If it is, measure the time of the period and calculate the frequency.

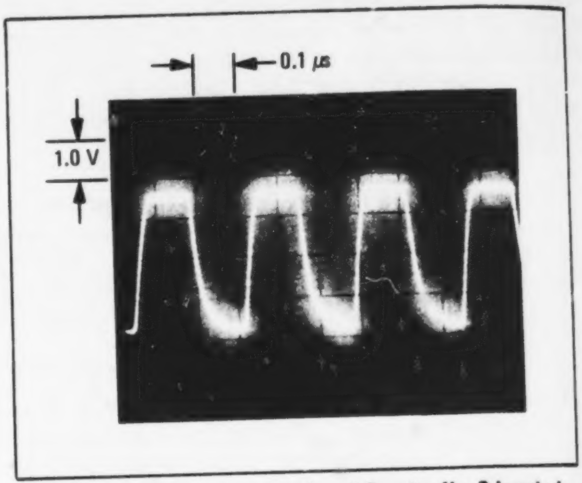


Figure 4. Oscilloscope Display of Counter No. 2 Input at J3-pin 2 (with ac coupling and internal triggering)

Table 12. Counter No. 2 Signals versus Signal Generator Frequency

FREQUENCY (MHz)		Level at U27-Pin no.			
Signal Generator Output	Counter 0 Input at J3-Pin 3	6	5	4	3
90.0000	234.4	L	H	L	H
80.0000	273.5	H	L	H	H
60.0000	351.5	L	H	H	H
50.0000	390.5	H	H	L	H
49.5000	392.6	L	H	L	L
49.0000	394.5	H	H	L	L
46.5555	404.0	L	L	L	H
46.5000	404.3	L	L	L	H
46.0555	406.0	L	L	L	H
46.0055	406.2	L	L	L	L
46.0050	406.2	L	H	H	L

4. Check the waveform for J3-Pin 3 as shown in Figure 5. The frequency of the Signal Generator is 90 MHz. Measurement is made using a 1:1 probe.

5. The Counter 0 output, Out 0, measured at test point J3-Pin 4 of Triple Programmable Counter U20 is a 100 Hz square wave for a Signal Generator frequency of 90 MHz (refer to Figure 6) and a 250 Hz square wave for a Signal Generator frequency of 90.00025 MHz.

SERVICE SHEET 9 (Cont'd)

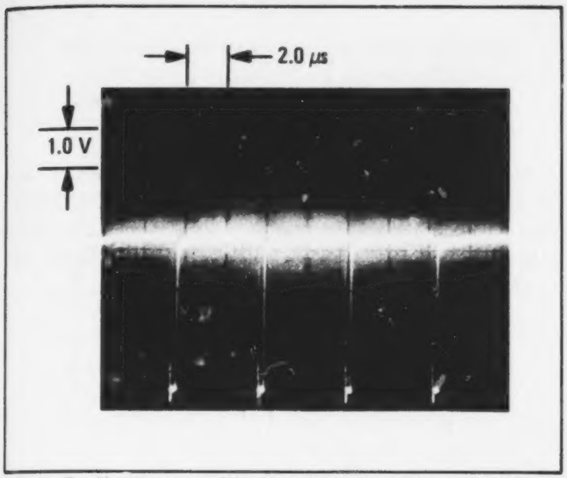


Figure 5. Oscilloscope Display of Counter 0 Input at J3-Pin3 (with ac coupling and internal triggering)

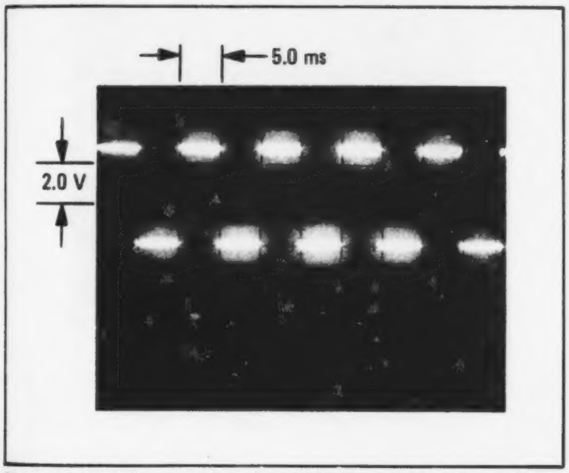


Figure 6. Oscilloscope Display of Counter 0 Output at J3-Pin 4 (with dc coupling and internal triggering)

6. The 100 or 250 Hz output of U20 clocks the Terminal Count Flip-Flop U31B to provide a time interval so the output of Counter No. 2 is gated to the ÷N line. Refer to Figure 7 for a display of the ÷N Terminal Count.

⟨√3⟩ P/O Triple Programmable Counter

1. The TB (Time Base) output at J3-Pin 7 of Triple Programmable Counter U20 is a 100 Hz square wave for a Signal Generator output frequency of 90 MHz and a 250 Hz squarewave for an output of 90.00025 MHz.

2. The square wave display at J3-Pin 7 will be the same as J3-Pin 4.

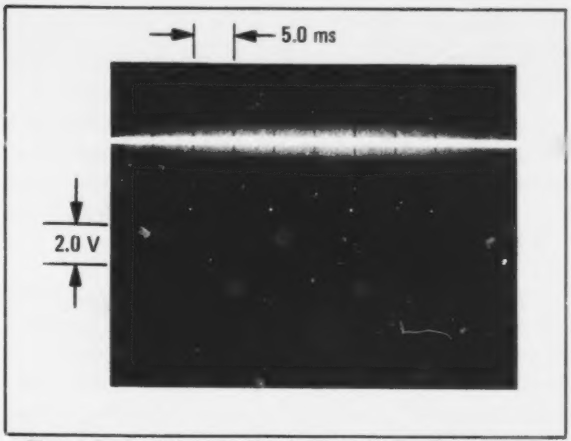


Figure 7. Oscilloscope Display of ÷N Counter Output at U14 Pin 3 (with dc coupling, internal triggering and a persistance display)

3. View the ϕ Offset waveform at J3-Pin 6 of Triple Programmable Counter U20 (refer to Figure 8). It is a 20 μs pulse at a 100 Hz rate for a Signal Generator output frequency of 90 MHz and a 20 μs pulse at a 250 Hz rate for a frequency of 90.00025 MHz.

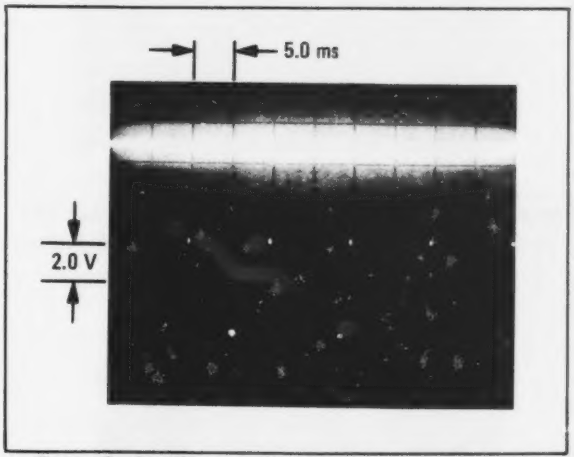


Figure 8. Oscilloscope Display of Counter 2 Output at J3-Pin 6 (with dc coupling and internal triggering)

4. Check the 1 MHz clock inputs for Counters 1 and 2 of Triple Programmable Counter. The clock is a 0 to 5 volt 200 ms pulse at the 1 MHz rate and can be checked at J3 pin 5.

⟨√4⟩ LF Loop Shift Registers, Write Strobe Generator

1. Check the waveform of Figures 9, 10 and 11 when all eight of the low frequency words are writ-

pages tightly bound

SERVICE SHEET 9 (Cont'd)

ten to the Low Frequency Loop (at power up or when the instrument is reset at the front panel).

NOTE

This action triggers the high slew rate and lets all seven data words be written to the Triple Programmable Counter. The remaining word is held in the shift registers.

2. Set the Signal Generator's output frequency to 500 MHz. Increment the frequency up 10 MHz. Three words are written to the LF Loop. Figure 12 shows that 16 bits are written for each word (only 12 bits are used). Figure 13 shows the write strobe signal WSTB(L).

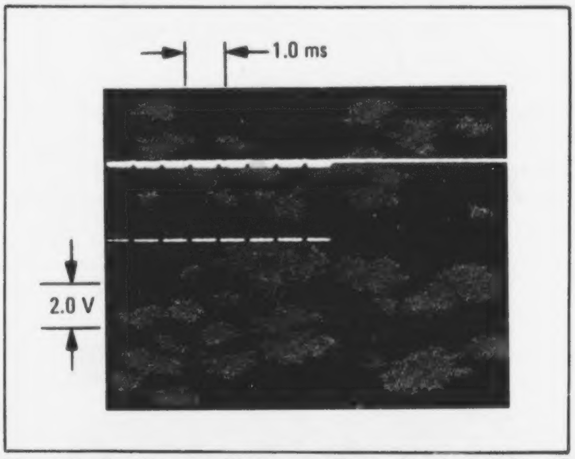


Figure 9. Oscilloscope Display of LF Loop Clock at J3-Pin 10 (with dc coupling and external triggering at J3-Pin 10)

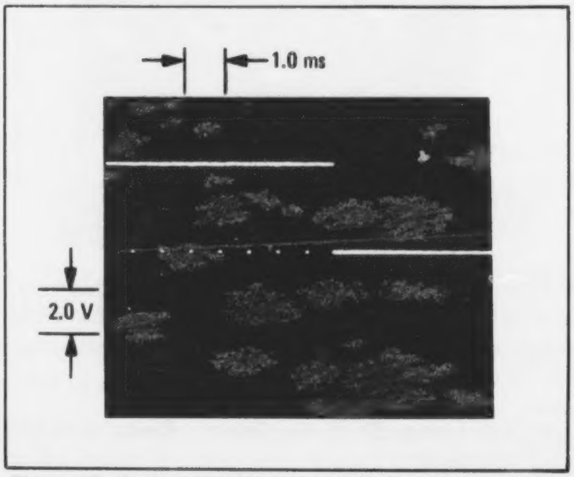


Figure 10. Oscilloscope Display of Shift Data Pulse at U21-Pin 13 (with dc coupling; external triggering from U21-Pin 13)

NOTE

The high slew rate is triggered which lets two data words be written to the Triple Programmable Counter. The third word is held in the shift registers.

3. Set the Signal Generator's frequency to 500 MHz. Increment the frequency up 1.00025 MHz to select 250 Hz resolution (TB and ÷N are 250 Hz). Four words are written to the LF Loop. Refer to Figures 14 and 15.

NOTE

High slew rate is triggered which lets three data words be written to the Triple Programmable Counter. The fourth word is held in the shift registers.

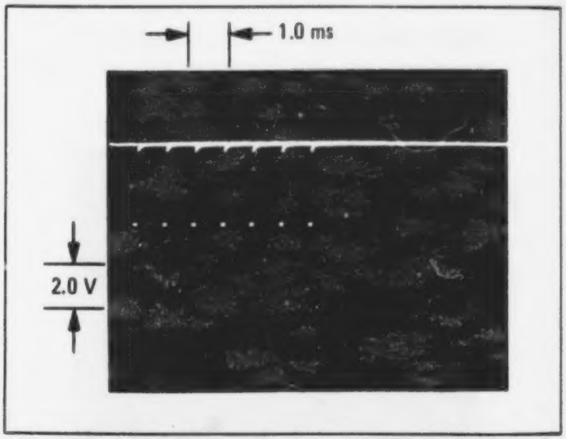


Figure 11. Oscilloscope Display of WSTB (L) at J3-Pin 9 (with dc coupling; external triggering from U21-Pin 13)

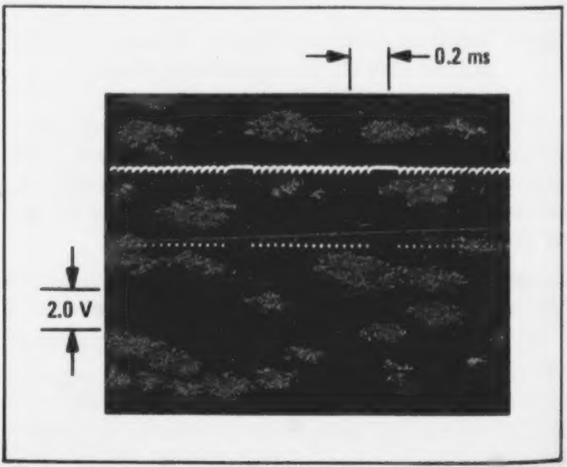


Figure 12. Oscilloscope Display of LF Loop Clock with 3 Data Words and a 10 MHz change at J3-Pin 10 (coupling is dc; triggering is external from J3-Pin 10)

SERVICE SHEET 9 (Cont'd)

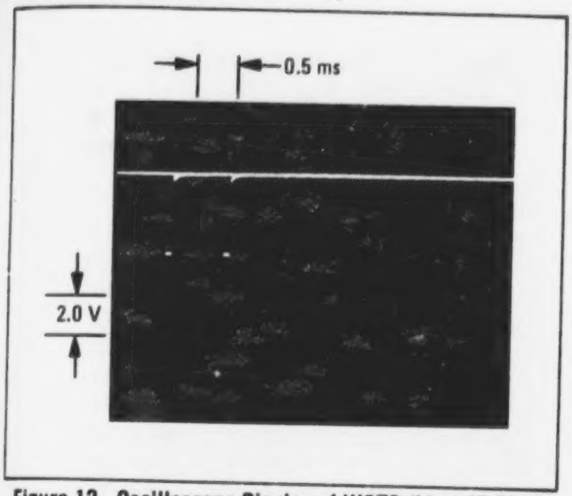


Figure 13. Oscilloscope Display of WSTB (L) at J3-Pin 9 (with dc coupling: external triggering from U21-Pin 13)

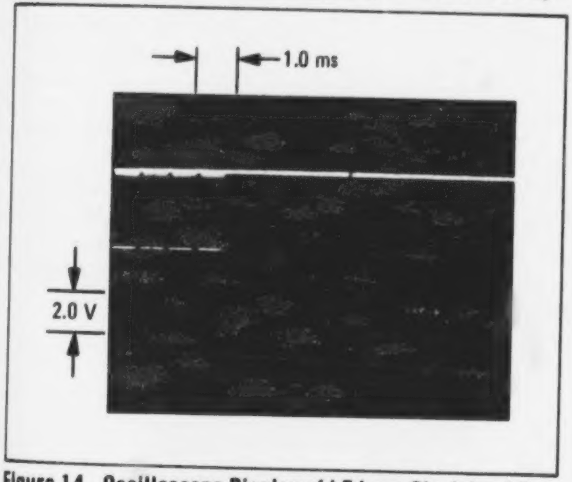


Figure 14. Oscilloscope Display of LF Loop Clock for 4 Data Words at J3-Pin 10 (with dc coupling; external triggering is from J3-Pin 10)

4. Set the Signal Generator to 250 MHz. Increment the frequency up 25 MHz. The LF Loop does not change frequency because U28B does not change state and no new data is stored in the shift registers for Counter Nos. 1 and 2. Only U21A changes state and then returns to its inactive state.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

This information provides an alternate method of troubleshooting Service Sheet 9 circuits. Service Sheet BD4 which leads to this information is used to troubleshoot from the digital (control) standpoint. If the signatures on these circuits are correct, the problem is probably in the controlled circuits. In this case, continue with the preceding troubleshooting information on this page. You may also refer to Service Sheet BD3. If the signatures are incorrect, recall that the digital signals pass through the circuits of Service Sheet 15 before arriving here.

NOTE

Signatures are not valid for Signal Generators with serial number prefixes of 2018A and below.

Purpose. Verify correct data transfer from the Microprocessor to the Low Frequency Loop.

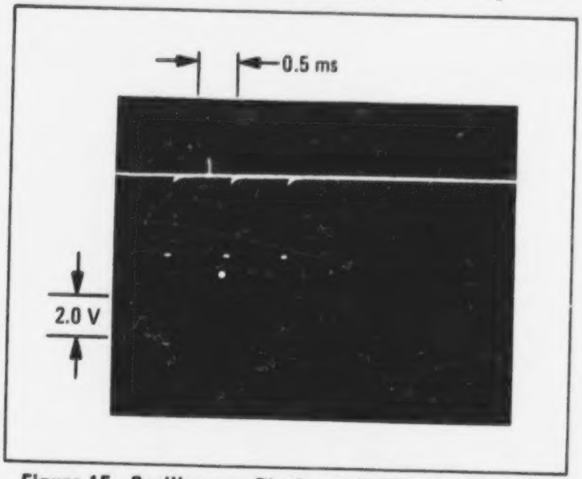


Figure 15. Oscilloscope Display of WSTB (L) at J3-Pin 9 (with dc coupling: external triggering is from U21-Pin 13)

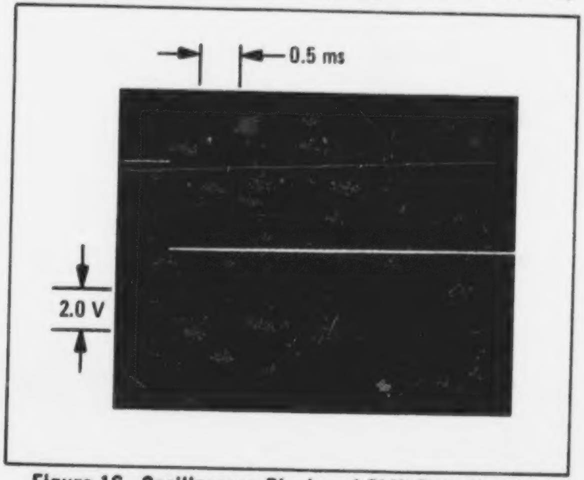


Figure 16. Oscilloscope Display of Shift Data (H) pulse (with dc coupling: external triggering from U21-Pin 13)

SERVICE SHEET 9 (Cont'd)

Setup. Set up the signature analyzer as follows:

1) GND to GND (close to the circuits being measured).
2) CLK to SA4 A11TP7
3) START to SA5 A11TP9
4) STOP to SA5 A11TP9

Set the signature analyzer controls as follows:

1) START IN
2) STOP OUT
3) CLK IN

Set up the Signal Generator as follows:

1) Set the LOGIC/RAM switch A11S1 to the LOGIC position.
2) Connect A3TP8 to A3TP9.

Initialize. Briefly short A11TP3 NMI to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

Probe. Connect to the node indicated in Table 13. Verify that each signature is correct and stable.

Table 13. LF Loop Shift Register Signatures

Node	Correct Signature	Comments
+5V	F84P	
U24-Pin 7	FUC5	SIPO DATA
U24-Pin 9	F84P *	LF CLK
U24-Pin 5	081F	LF D0
U24-Pin 4	040P	LF D1
U24-Pin 3	0207	LF D2
U24-Pin 10	F6AA	LF D3
U24-Pin 13	0895	LF D4
U24-Pin 12	044A	LF D5
U24-Pin 11	0225	LF D6
U24-Pin 2	0112	LF D7
U25-Pin 5	0089	LF A0
U25-Pin 4	0044	LF A1
U25-Pin 3	0022	WRT STROB
U25-Pin 10	F7C8	FM RANGE

*Signature is same as +5V but probe tip should blink.

Remove the jumper between A3TP8 and A3TP9. Reset the LOGIC/RAM switch to the RAM position. Reset the Signal Generator by setting the front panel RESET-STBY-ON switch to RESET and back to ON.

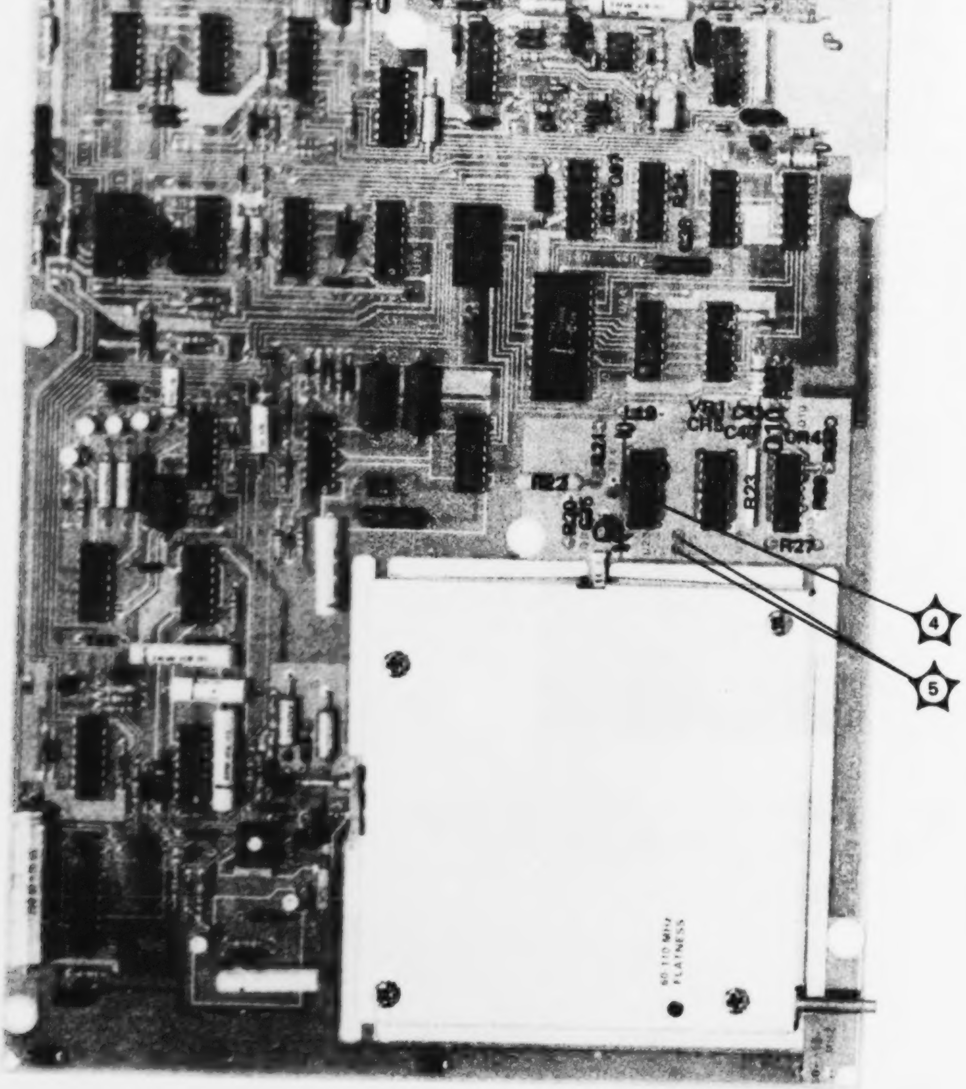

P/O A3 ASSEMBLY
L19
VR1
CR5
C49
CR4
R22
R20
R23
R27
4
5
60-110 MHz FLATNESS

Figure 8-67. LF Loop Data and Timing Control Component Locations

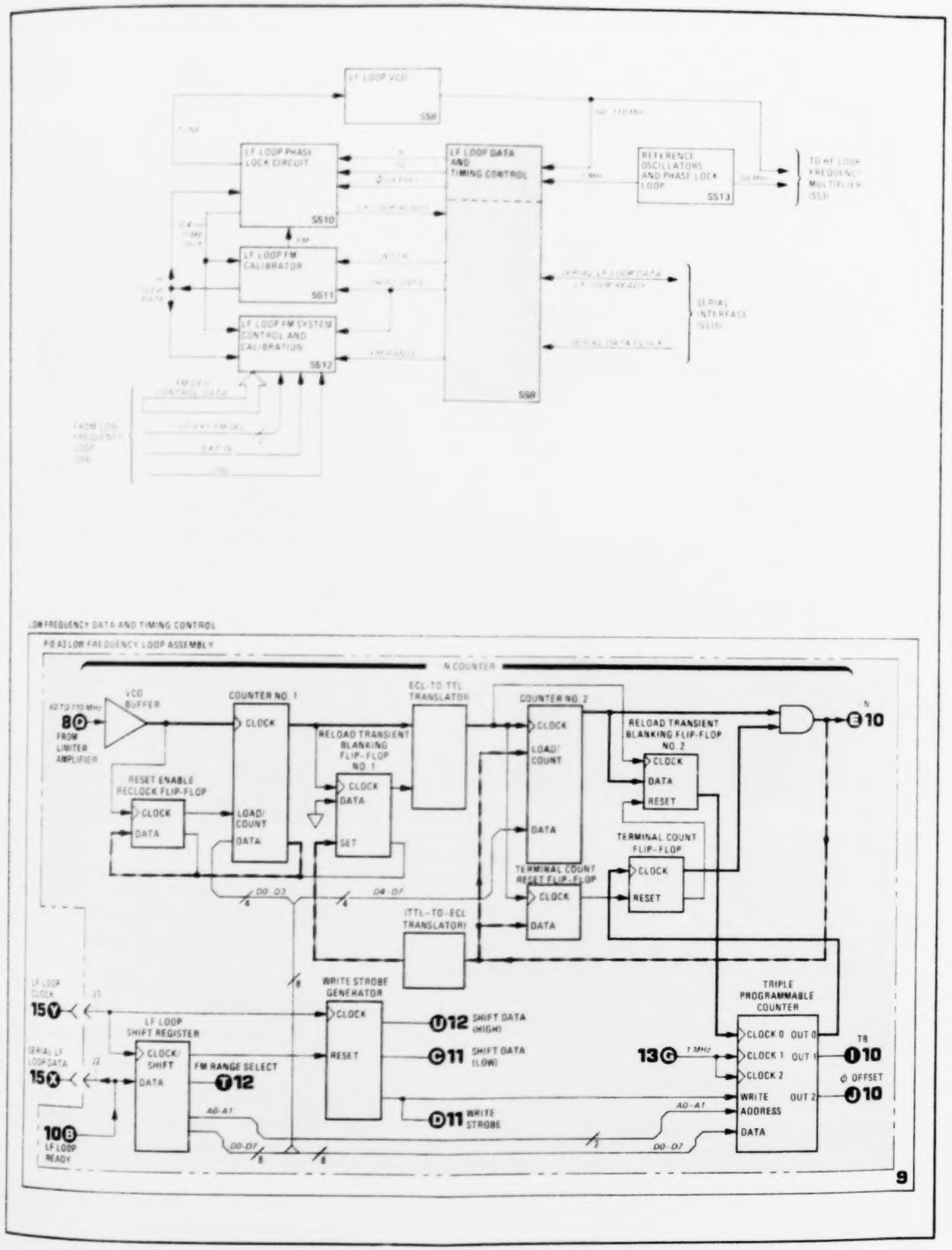
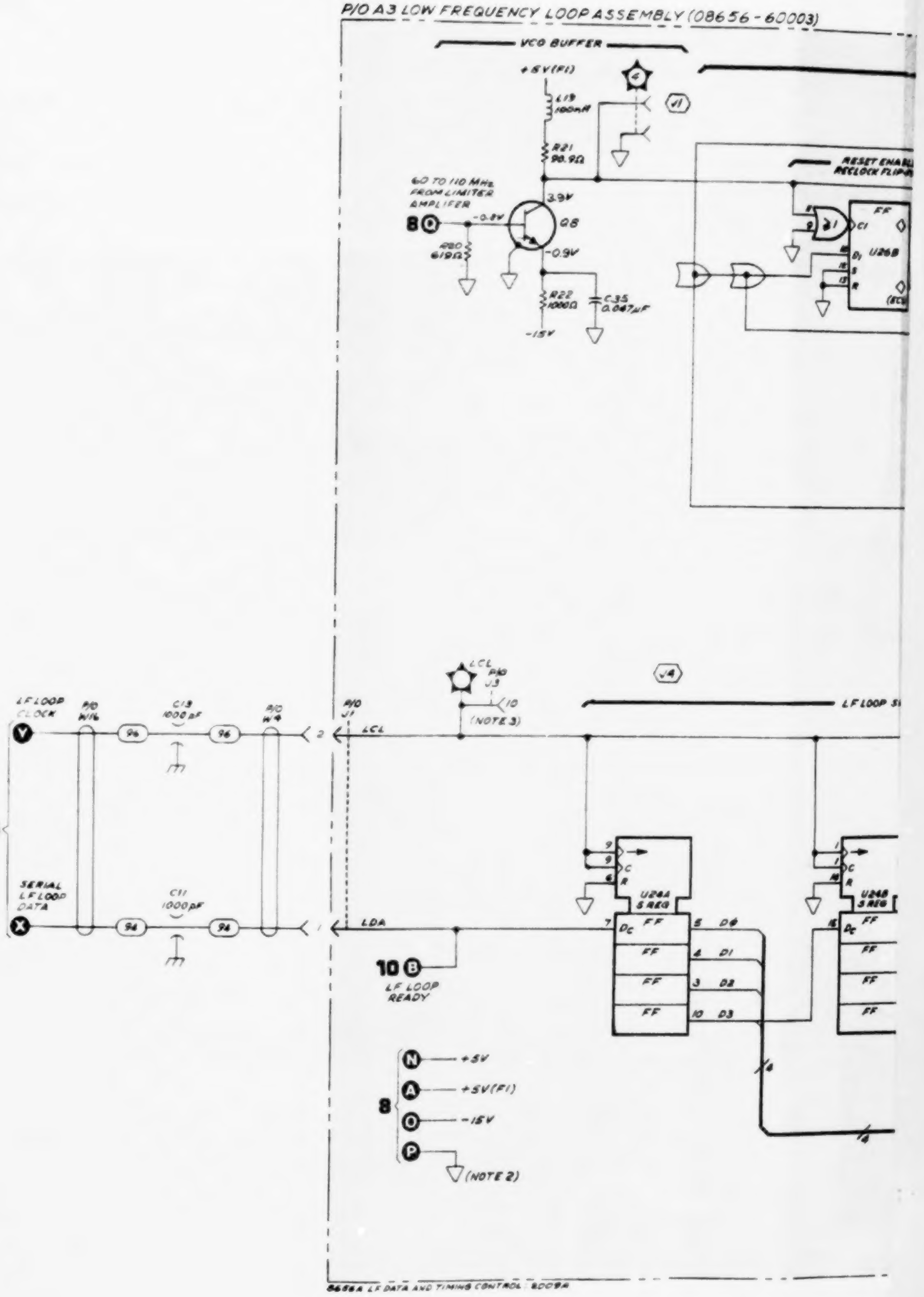
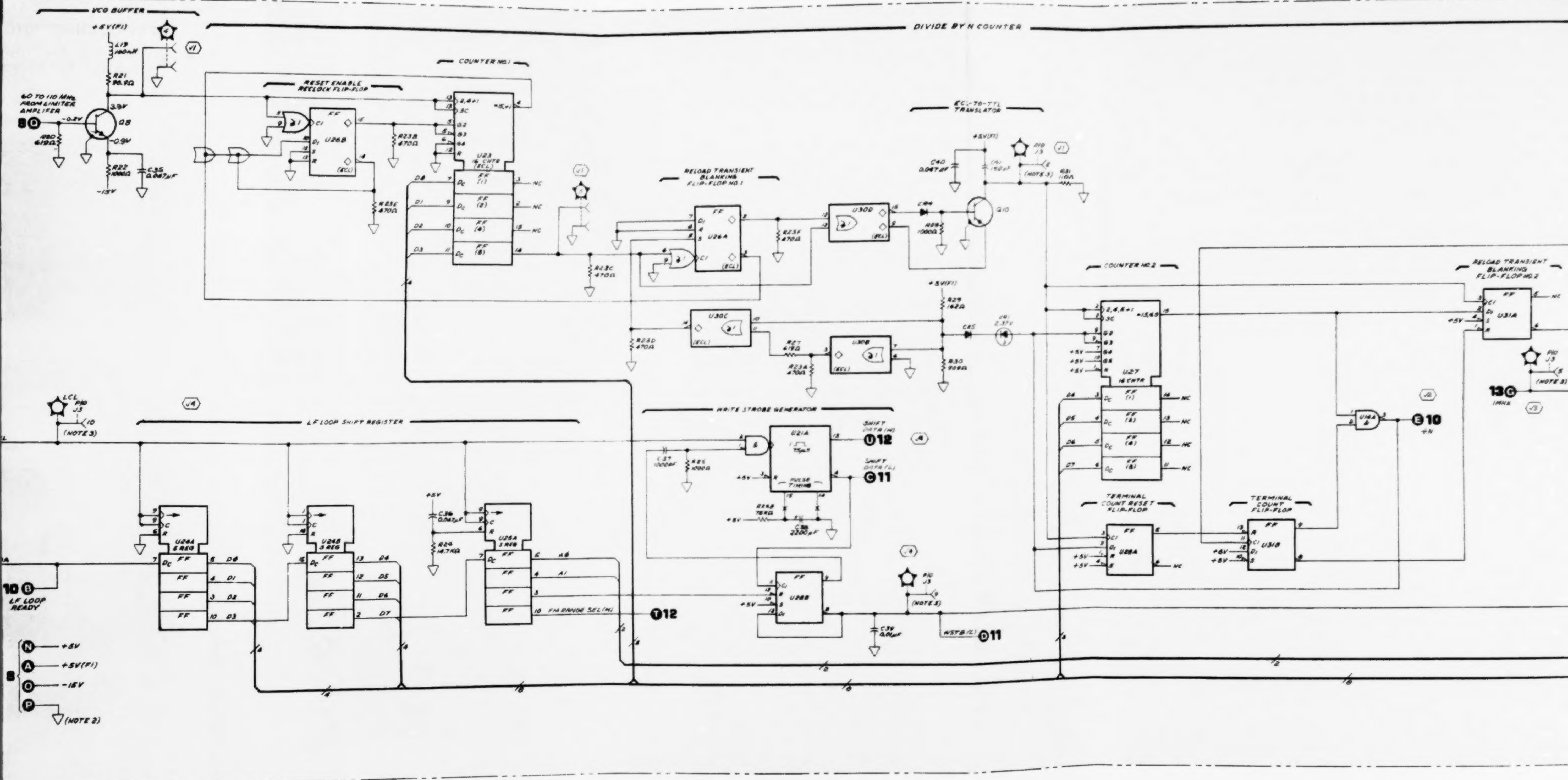

LF LOOP VCO
SS8
TUNE
LF LOOP PHASE LOCK CIRCUIT
SS10
LF LOOP DATA AND TIMING CONTROL
SS9
REFERENCE OSCILLATORS AND PHASE LOCK LOOP
SS13
TO HF LOOP FREQUENCY MULTIPLIER (SS3)
LF LOOP FM CALIBRATOR
SS11
FM
LF LOOP FM SYSTEM CONTROL AND CALIBRATION
SS12
SERIAL LF LOOP DATA
LF LOOP READY
SERIAL INTERFACE (SS15)
SERIAL DATA CLOCK
FM DEV CONTROL DATA
EXT IN
LOW FREQUENCY DATA AND TIMING CONTROL
P/O A3 LOW FREQUENCY LOOP ASSEMBLY
N COUNTER
60 TO 110 MHz
8P
FROM LIMITER AMPLIFIER
VCO BUFFER
COUNTER NO. 1
CLOCK
LOAD/COUNT
DATA
RESET ENABLE RECLOCK FLIP-FLOP
RELOAD TRANSIENT BLANKING FLIP-FLOP NO. 1
SET
ECL-TO-TTL TRANSLATOR
COUNTER NO. 2
RELOAD TRANSIENT BLANKING FLIP-FLOP NO. 2
RESET
TERMINAL COUNT FLIP-FLOP
TERMINAL COUNT RESET FLIP-FLOP
(TTL-TO-ECL TRANSLATOR)
N
E10
D0-D3
D4-D7
LF LOOP CLOCK
J1
15Y
SERIAL LF LOOP DATA
J2
15X
10B
LF LOOP READY
LF LOOP SHIFT REGISTER
CLOCK/SHIFT
FM RANGE SELECT
T12
WRITE STROBE GENERATOR
U12 SHIFT DATA (HIGH)
C11 SHIFT DATA (LOW)
D11 WRITE STROBE
A0-A1
D0-D7
TRIPLE PROGRAMMABLE COUNTER
CLOCK 0
CLOCK 1
CLOCK 2
WRITE
ADDRESS
OUT 0
OUT 1
OUT 2
13G
1 MHz
T8
I10
ϕ OFFSET
J10
9

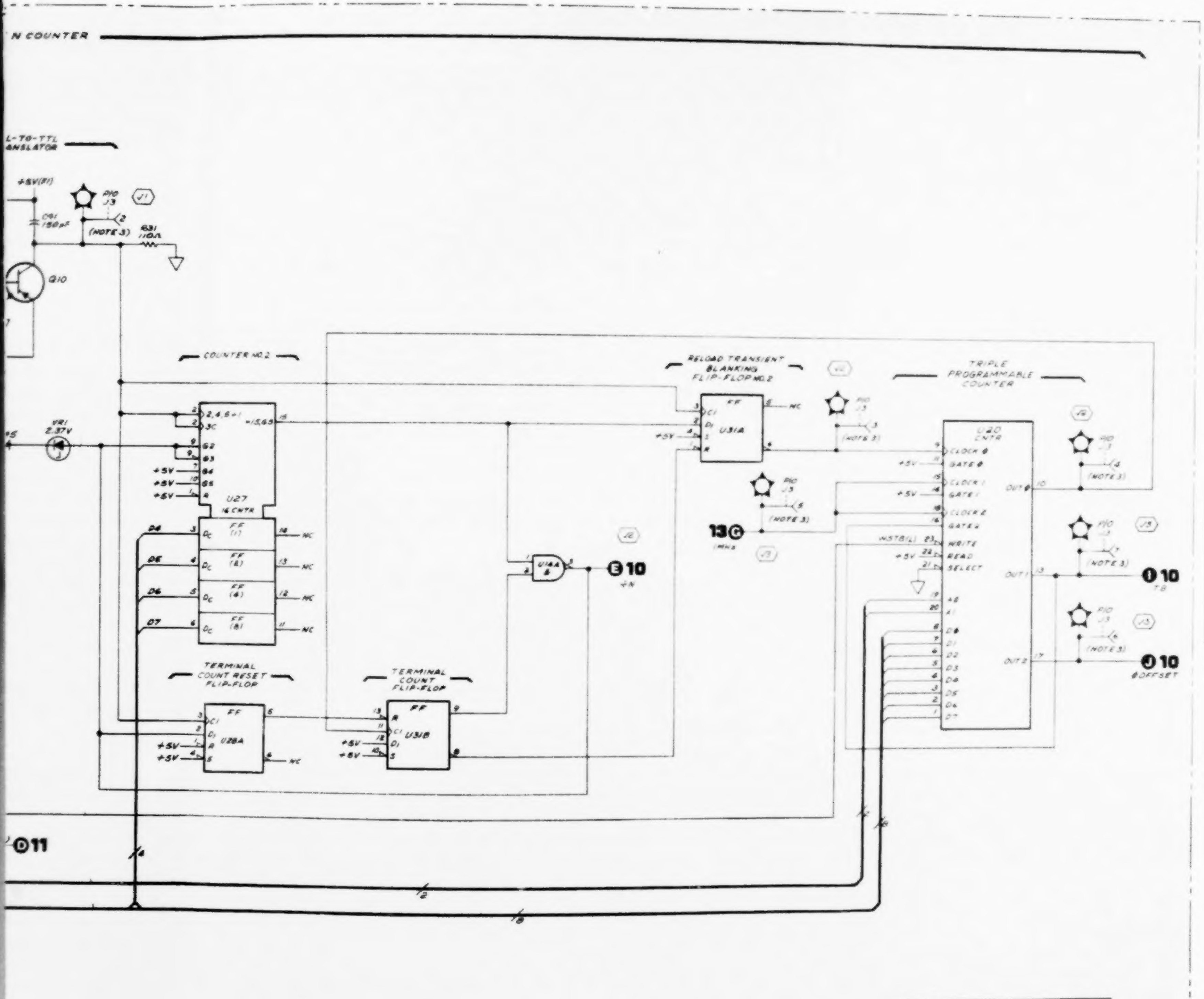
Figure 8-68. LF Loop Data and Timing Control Block Diagrams


P/O A3 LOW FREQUENCY LOOP ASSEMBLY (08656-60003)
VCO BUFFER
+5V(F1)
L19 100nH
R21 90.9Ω
J1
60 TO 110 MHz FROM LIMITER AMPLIFIER
8Q
-0.8V
3.9V
Q8
-0.9V
R80 619Ω
R22 1000Ω
C35 0.047μF
-15V
RESET ENABLE RECLOCK FLIP-FLOP
FF
U26B
LCL
P/O J3
10
(NOTE 3)
J4
LF LOOP
LF LOOP CLOCK
P/O W16
C13 1000pF
P/O W4
P/O J1
15
SERIAL LF LOOP DATA
C11 1000pF
LDA
10B
LF LOOP READY
U24A S REG
U24B S REG
D0
D1
D2
D3
8
N +5V
A +5V(F1)
O -15V
P (NOTE 2)
8656A LF DATA AND TIMING CONTROL 6009A

3 LOW FREQUENCY LOOP ASSEMBLY (08656-60003)


VCO BUFFER
DIVIDE BY N COUNTER
+5V(FI)
L19 100nH
R21 90.9Ω
60 TO 110 MHz FROM LIMITER AMPLIFER
8 D
-0.2V
3.9V
Q8
-0.9V
R20 619Ω
R22 1000Ω
C35 0.047μF
-15V
RESET ENABLE RECLOCK FLIP-FLOP
FF
U26B
(ECL)
R23B 470Ω
R23E 470Ω
COUNTER NO.1
U23
16 CNTR (ECL)
D0
D1
D2
D3
NC
R23C 470Ω
RELOAD TRANSIENT BLANKING FLIP-FLOP NO.1
U26A
R23F 470Ω
U30D
ECL-TO-TTL TRANSLATOR
C40 0.047μF
C41 150μF
(NOTE 3)
R31 118Ω
Q10
CR4
R28 1000Ω
U30C
U30B
R23D 470Ω
R27 619Ω
R23A 470Ω
R29 162Ω
R30 909Ω
C45
VR1 2.37V
COUNTER NO.2
U27
16 CNTR
D4
D5
D6
D7
TERMINAL COUNT RESET FLIP-FLOP
U28A
TERMINAL COUNT FLIP-FLOP
U31B
U14A
E 10
÷N
RELOAD TRANSIENT BLANKING FLIP-FLOP NO.2
U31A
P10 J3
13 G
1MHz
LCL
(NOTE 3)
LF LOOP SHIFT REGISTER
U24A 5 REG
U24B 5 REG
U25A 5 REG
C36 0.047μF
R24 14.7KΩ
A0
A1
FM RANGE SEL(H)
T12
WRITE STROBE GENERATOR
U21A
15μS
PULSE TIMING
SHIFT DATA (H)
U12
SHIFT DATA (L)
C11
C37 1000pF
R25 1000Ω
R26B 75KΩ
C38 2200pF
U28B
C39 0.01μF
WSTB(L)
D11
10 B
LF LOOP READY
N +5V
A +5V(FI)
O -15V
P (NOTE 2)
8

F DATA AND TIMING CONTROL: 8009A


N COUNTER
L-TO-TTL
ANSLATOR
+5V(F1)
C91
150pF
P10
J3
V1
(NOTE 3)
R31
110Ω
Q10
COUNTER NO.2
VR1
2.37V
U27
16 CNTR
2,4,5+1
3C
G2
G3
G4
G5
+15,G5
FF (1)
FF (2)
FF (4)
FF (8)
D4
D5
D6
D7
NC
TERMINAL COUNT RESET FLIP-FLOP
U28A
TERMINAL COUNT FLIP-FLOP
U31B
U14A
E 10
÷N
RELOAD TRANSIENT BLANKING FLIP-FLOP NO.2
U31A
FF
13 G
1MHz
TRIPLE PROGRAMMABLE COUNTER
U20
CNTR
CLOCK 0
GATE 0
CLOCK 1
GATE 1
CLOCK 2
GATE 2
WSTB(L)
WRITE
READ
SELECT
A0
A1
D0
D1
D2
D3
D4
D5
D6
D7
OUT 0
OUT 1
OUT 2
I 10
TB
J 10
0 OFFSET
D 11
+5V

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number, e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES
2. CHASSIS GROUND IS ACHIEVED THROUGH A3J1-4 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. SERVICE TEST POINT PIN OF DUAL IN-LINE TEST SOCKET J3.

REFERENCE DESIGNATIONS

NO PREFIX	A3 CONT.
[illegible]	L19 Q8,10 R20-31 TP4,5 U14,20,21, 23-28,30,31 VR1
A3	
C35-41 CR4,5 J1,3	

LOGIC LEVELS

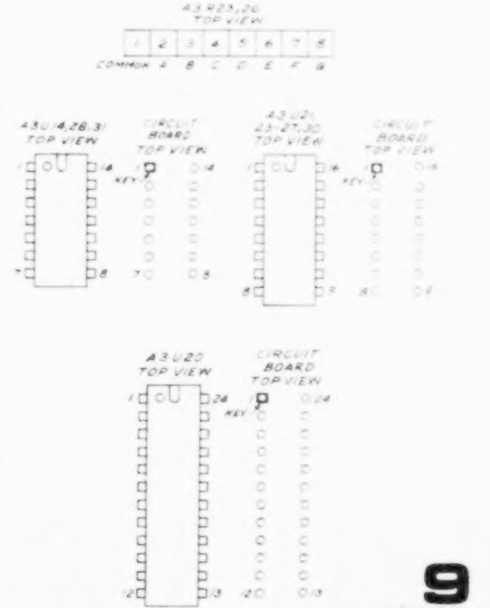
	TTL	ECL
HIGH	>2V	>+4.2V
LOW	<0.8V	<+3.3V
< IS MORE NEG THAN > IS MORE POS THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q8	1854-0696
Q10	1853-0018
U14	1820-0681
U20	1820-2005
U21	1820-1423
U23	1820-1788
U24,25	1820-2008
U26	1820-1225
U27	1820-1430
U28,31	1820-1112
U30	1820-0802

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U14,28,31	+5V - 14 ▽ - 7
U20	+5V - 24 ▽ - 12
U21,24,25,27	+5V - 16 ▽ - 8
U23,26,30	+5V(F1) - 16 ▽ - 8


A3 R23,26
TOP VIEW
1 2 3 4 5 6 7 8
COMMON A B C D E F G
A3U14,28,31
TOP VIEW
CIRCUIT BOARD TOP VIEW
A3U21
23-27,30
TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY
A3 U20
TOP VIEW
CIRCUIT BOARD TOP VIEW
1
14
7
8
16
9
24
12
13

9
P/O A3

Figure 8-69. LF Loop Data and Timing Control Schematic Diagram

SERVICE SHEET 10
P/O A3 LOW FREQUENCY LOOP ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The difference in phase between the ÷N and the TB signals is detected by the Phase-to-Charge Converter. The charge on C46 is converted to a voltage by U8C which is summed with the In-Band FM Correction Voltage by U12C. The Tune Voltage Output is sampled periodically and stored to tune the Low Frequency Loop VCO. If there is no change in phase, the sampled voltage remains constant and the VCO frequency does not change. The Tune Sample Monostable sets the tune sample duration of 0.4 ms. The rate is controlled by the signals that are phase compared, TB and ÷N. The Phase Detector Reset resets U8C, that is, the charge across C49 set by the Phase-to-Charge Converter output is discharged. A frequency change that passes the 25.6 kHz band edge enables the High Slew Rate mode. The HIGH SLEW RATE SEL signal to U16C controls a reduction in the gain of U8C and U6B that matches the reduction in attenuation into Q4. The effect of the attenuation decrease allows quicker response of the Tune Voltage change while the gain remains constant through the amplifier chain.

Phase-to-Charge Converter

The two D-type Flip-Flops U17A and B are clocked by the 100 Hz or 250 Hz time base pulse TB and the ÷N input respectively. The set and D inputs of U17A and B are tied high (+5 volts), therefore U17A and B are controlled by the reset and clock inputs. When reset is low it overrides the clock input. With the reset high, a low-to-high clock pulse clocks the active-high output high and the active-low output low (D1 is high). Depending on which pulse arrives first, either U17A or B is clocked first. After the second clock arrives both active-high outputs will be high and gate U14B output will go low resetting U17A and B. (Refer to Table 1.) Any phase difference between the TB and ÷N inputs will result in a correction voltage being applied to the VCO via the TUNE output. When the TB pulse arrives first, it clocks U17A active-high output high. This biases CR6 off. Current flows through CR9 to the input of the Charge-to-Voltage Converters.

Table 1. U17A and B operation

Set	Reset	D	Clock	Pins-5/9	Pins-6/8
+5V(H)	L	+5V(H)	X	L	H
+5V(H)	H	+5V(H)	↑	H	L

Charge-To-Voltage Converter

The current from CR9 is applied to the negative input of integrator U8C. This causes the output to change in the negative direction. The effect of charging C49 causes the output to take the form of a linear "ramp" voltage. If the ÷N pulse had clocked U17B the output going low turns off CR8 which turns on CR10, thus drawing current from C49 and the output of U8C is a "ramp" in the positive direction. When U17B is reset, its active-high output goes high and CR10 is reversed biased.

When both U17A and B are clocked simultaneously, there is no voltage change on C49. The other current source for integrator U8C is the ϕ Offset which is a low pulse for 20 μs. When the ϕ Offset is pulsed low, Exclusive-Or gate U13D's output is low for the 20 μs duration of the pulse. With U13D's output low and with 0.6 Vdc across CR12, CR11 is turned on and the integrator voltage is a positive "ramp". This small offset in voltage prevents the phase detector from operating in the non-linear zero region. The output of U8C is applied to the unity gain Loop Summing Amplifier and applied to the Tuning Voltage Sample and Hold Capacitor C51 by FET switch U7B.

Tune Sample Control

The output of gate U14B resets U17A and B and triggers the Tune Sample Monostable U15A on the high to low transition. Refer to Table 2.

Table 2. U15A Tune Sample Monostable Operation

Pin-3	Pin-1	Pin-2	Pin-13	Pin-4	Pulse Duration
H	.	H	H	L	0.4 ms

The active-high output is set high for 0.4 ms. The low active-low output is gated at U10B with the End of Conversion EOC(L) from the Successive Approximation Register (refer to Service Sheet 11). The EOC(L) is low unless the loop is calibrating the FM sensitivity of the VCO. During calibration it is high thus preventing the tune voltage from being sampled. With both inputs to U10B low, the output goes high. This allows the Tune Voltage Sample Control Comparator U9A to switch its output for 0.4 ms to +15 Vdc. This turns on FET switch U7B. Capacitor C50 introduces a small delay of the voltage charge. When U7B is on, the tune voltage is sampled for 0.4 ms.

The active-high output of U15A is inverted by U4A. This output is θapplied to the serial data input from the Microprocessor to signal the Microprocessor when the Low Frequency Loop is ready to have data written to it.

Phase Detector Reset Control

The active-high output from U15A is coupled to U15B Phase Detector Reset Monostable. It triggers U15B on the high-to-low transition of the pulse. Refer to Table 3. The active-high output of U15B goes

SERVICE SHEET 10 (Cont'd)

high for 1.5 ms to change the output of the Phase Detector Reset Control comparator U9C from −15 to +15 Vdc. Capacitor C44 introduces a small delay of the voltage charge. This change in voltage turns on FET switch U3B to discharge the integrator capacitor C49.

Table 3. U15B Operation

Pin-11	Pin-9	Pin-10	Pin-5	Pin-12	Pulse Duration
H	↓	H	⊓	⊔	1.5 ms

Slew Rate Control

The other control of Charge-to-Voltage Converter U8C is FET switch Q13. Q13 is closed when the Low Frequency Loop is in the High Slew Rate Mode and is activated by Slew Rate Control Comparator U16C. The comparator turns the FET switch on when the frequency of the Low Frequency Loop VCO passes the 25.6 kHz band edge. The output of High Slew Rate Monostable U21B (refer to Service Sheet 11) controls this operation. The High Slew Rate Mode lasts for approximately 500 ms. During this time the loop response is quicker than normal in order to reduce the time required for a large frequency change. This is accomplished by decreasing the gain of U8C and U6B while decreasing the attenuation of the signal into Q4. Q13 is turned on which places additional capacitance in parallel with C49 thereby reducing the gain. U7A is turned on which places additional resistance across R49, thus reducing the gain of U6B. Q2 is also turned on which places a low resistance in parallel with R52 to reduce the attenuation of the signal into Q4. The total reduction in gain equals the reduction in attenuation.

Summary

Every 10 or 4 ms (100 or 250 Hz resolution), any phase change between the ÷N and TB signals is sampled and held on CS1 to correct the VCO frequency. This voltage is applied to Loop Integrator U8B where the voltage is changed in the direction to correct the VCO's frequency (or to achieve lock if a frequency change has occurred). This action corrects for the VCO's frequency drift. The output of the Loop Integrator is applied to the Switchable Attenuator and then to the High Impedance Buffer Q4. FET switches Q3, U7A and Q2 are controlled by the Slew Rate Control Comparator U16C and are closed the same as Q13 when the VCO frequency change passes the 25.6 kHz band edge. When U7A is closed, R50, 31.6 kΩ is in parallel with R49, 18 MΩ, increasing the slew rate of the tune voltage. This moves the VCO to the correct frequency quicker. When FET switch Q2 is closed, the attenuation to the High Impedance Buffer Q4 is decreased to 1/500 of its previous value by paralleling R54 with R52. The reduced attenuation of the switchable attenuator compensates for the lower gain of integrator U8C (1/500th normal) during high slew rate. This keeps the overall gain of the loop constant. CR13, VR4, CR15, VR5 prevent the output from going too negative.

SERVICE SHEET 10 (Cont'd)

TROUBLESHOOTING

Procedures for checking the circuits of the A3 Low Frequency Loop Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g. ⟨√3⟩. Fixed voltages are shown on the schematic inside a hexagon, e.g. ⟨2V±0.2V⟩. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Frequency Counter	HP 5328A
Oscilloscope	
Storage Mainframe	HP 181A
Vertical Amplifier	HP 1801A
Time Base	HP 1820C

⟨√1⟩ Phase-to-Charge Converter, Charge-to-Voltage Converter

1. Set the Signal Generator to 500 MHz without modulation.

2. Check the following voltages in Table 4 and the waveforms of Figure 1 with the Low Frequency Loop locked.

Table 4. Phase-To-Charge Converter Voltages

Test Point	Voltage (Vdc)
J2 Pin 11	+2.6 to +3.2
J2 Pin 12	+0.6 to +1.2

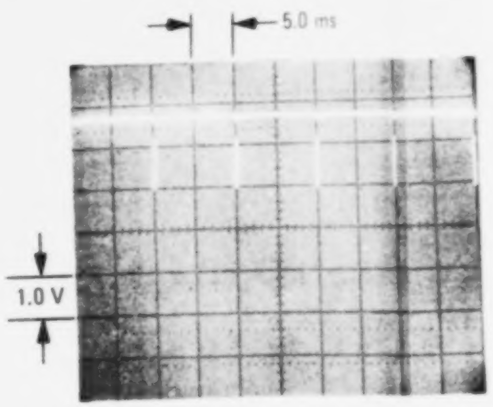


Figure 1. Display of Signal at J3-Pin 12 with LF Loop Locking (with dc coupling; external triggering to J2-pin 8)

SERVICE SHEET 10 (Cont'd)

3. Increment the frequency up 10 MHz and check Figures 2 through 5 as the LF Loop locks.

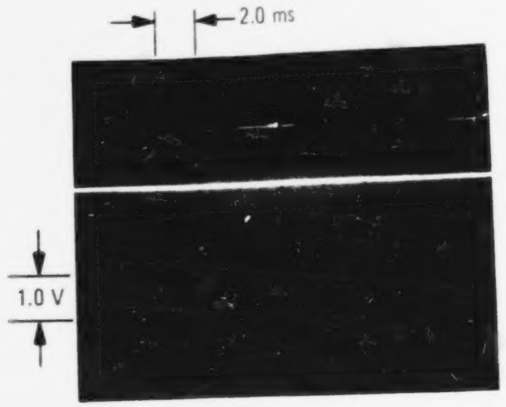


Figure 2. Display of Signal at J2-Pin 12 as the LF Loop is Locking (with dc coupling; external triggering to J3-Pin 4)

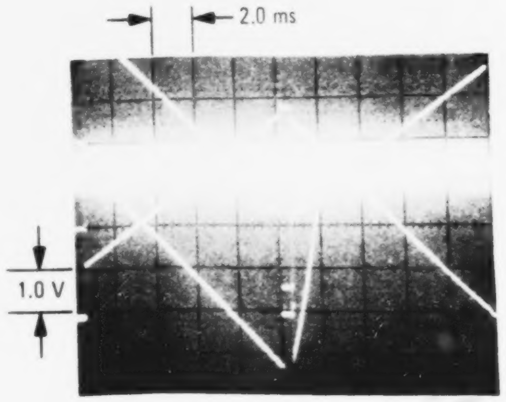


Figure 3. Display of Signal at J2-Pin 11 with the LF Loop Locking (with dc coupling; external triggering from J3-Pin 4)

SERVICE SHEET 10 (Cont'd)

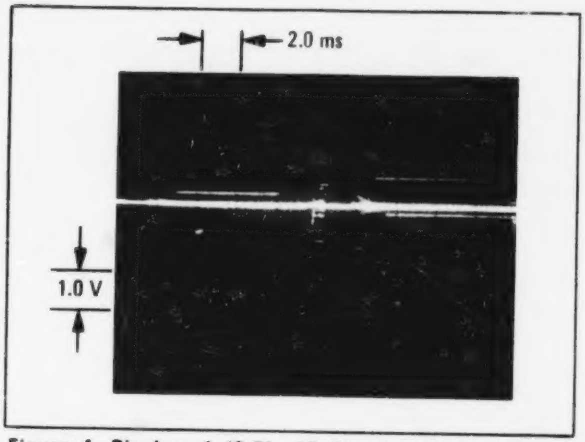


Figure 4. Display of J3-Pin 12 Signal with the LF Loop Locking (with dc coupling: external triggering from J3-Pin 4)

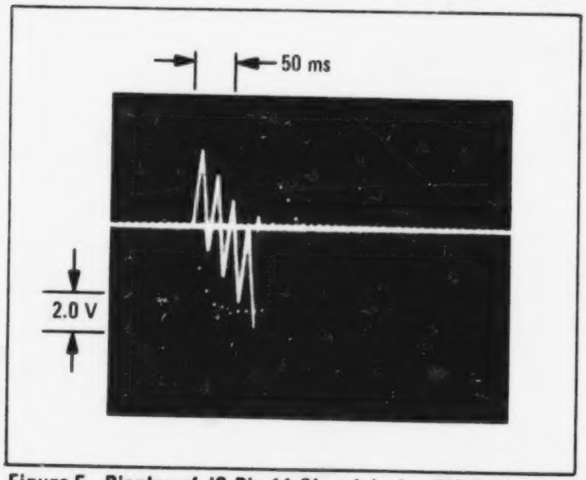


Figure 5. Display of J3-Pin 11 Signal during FM Calibration With LF Loop Locking (with dc coupling: external triggering from U2-Pin 7 SAR CLK)

√2 Tune Sample Monostable, Tune Voltage Sample Control, Phase Detector Reset Monostable, Phase Detector Reset Control

1. Set the Signal Generator to 500 MHz (÷N will be 100 Hz).

2. The Tune Sample Monostable will be triggered at the 100 Hz rate to store the correction voltage on the Tuning Voltage Sample and Hold Capacitor C51.

3. When the output pulse of the Tune Sample Monostable is completed, the active-high output goes low which triggers the Phase Detector Reset Monostable.

4. Verify that the signals are the same as those of Figures 6 and 7.

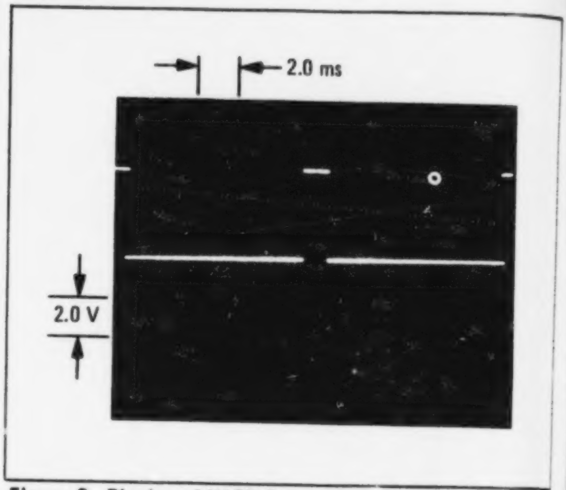


Figure 6. Display of U15B Output Pulse (with dc coupling to J2-Pin 8; external triggering from J3-Pin 4)

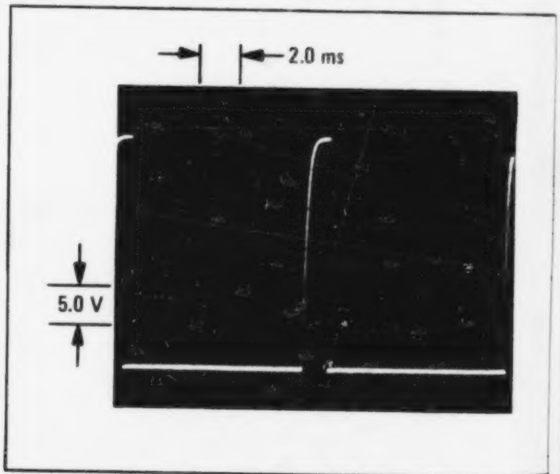


Figure 7. Display of Comparator Output Used To Close FET Switch U3B (dc coupling to J2-Pin 4; external triggering from J3-Pin 4)

√3 Slew Rate Control

1. Set the Signal Generator to 500 MHz.

2. Increment the frequency 10 MHz.

3. Verify that the output of comparator U16C Pin 13 is pulsed from −15 Vdc to +15 Vdc closing FET switches Q13, U7A and Q2.

√4 Loop Integrator, Switchable Attenuator, High Impedance Buffer

1. Set the Signal Generator to 500 MHz.

SERVICE SHEET 10 (Cont'd)

2. Verify that the voltages and VCO output frequencies shown in Table 5 are correct.

3. Increment the frequency from 500 MHz in 10 MHz steps. Verify that the waveforms of Figures 8 and 9 are correct.

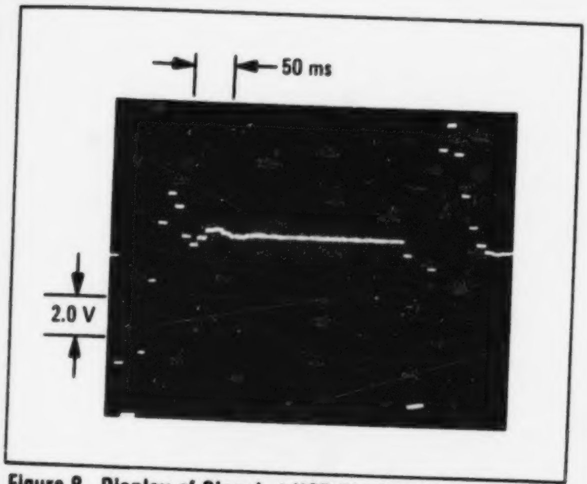


Figure 8. Display of Signal at U6B-Pin 6 (with dc coupling: external triggering from J2-Pin 7)

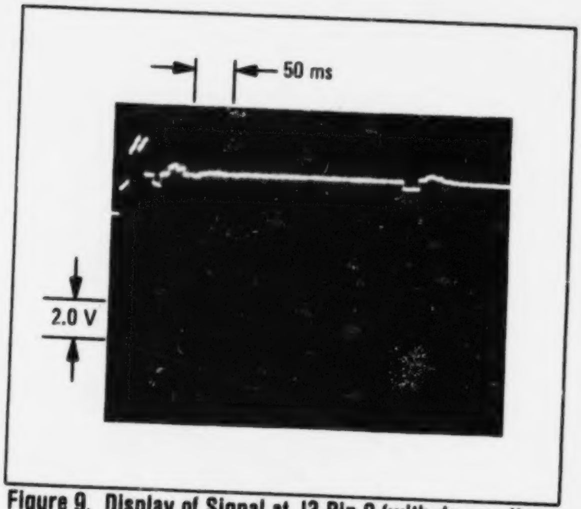


Figure 9. Display of Signal at J3-Pin 9 (with dc coupling: external triggering from J2-Pin 7)

Table 5. Loop Integrator and VCO Tune Voltage and Frequency Output

Frequency (MHz)		Check Voltage (Vdc) at	
Front Panel Setting	LF Loop VCO Output	J3 pin 14	TP2
500	100	0.0 to + 0.4	+0.4 to + 0.8
510	90	+2.3 to + 2.7	+2.6 to + 3.0
520	80	+5.0 to + 5.4	+5.0 to + 5.4
530	70	+7.3 to + 7.7	+7.5 to + 7.9
540	60	+9.8 to +10.2	+9.8 to +10.2
550	100	+0.0 to + 0.4	+0.4 to + 0.8

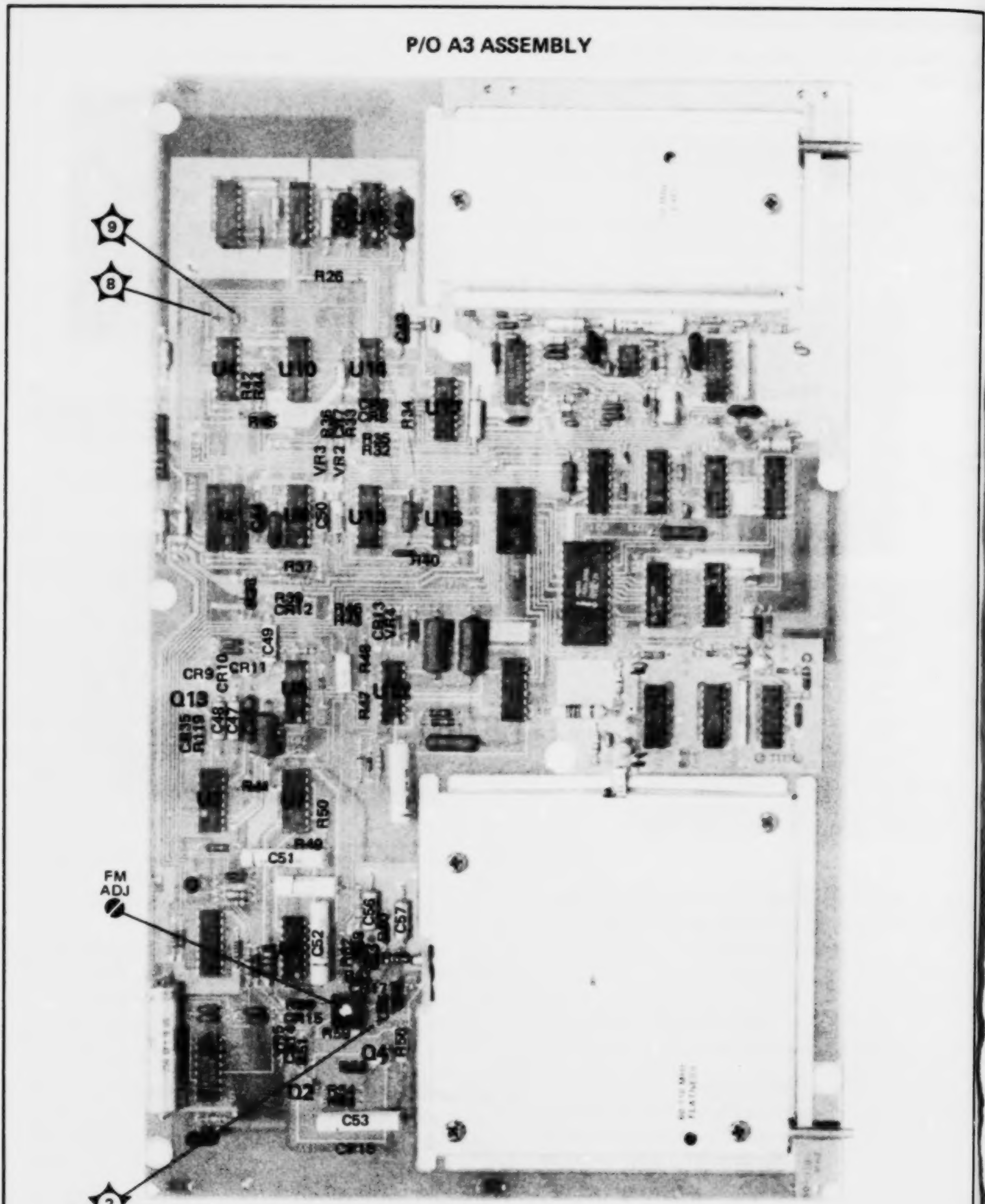

P/O A3 ASSEMBLY
9
8
R26
U10
U14
R34
R36
R32
VR3
VR2
C50
R57
R40
R39
CR12
R46
C49
CR9
CR10
CR11
Q13
CR35
R119
R48
R47
R50
R49
C51
FM ADJ
C56
C57
C52
CR15
Q4
R58
Q2
C53
CR16
2

Figure 8-70. LF Loop Phase Lock Circuit Component Locations

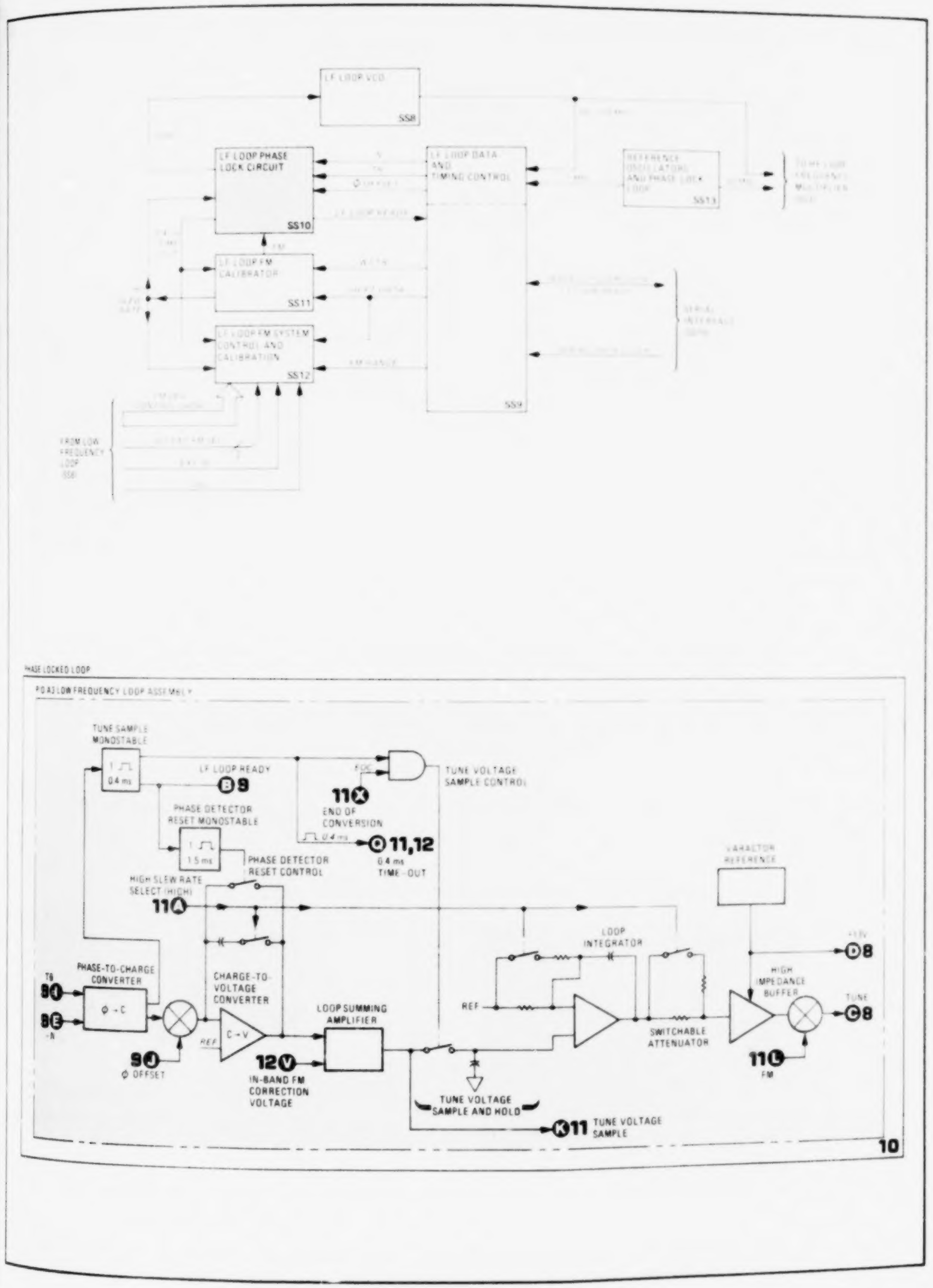
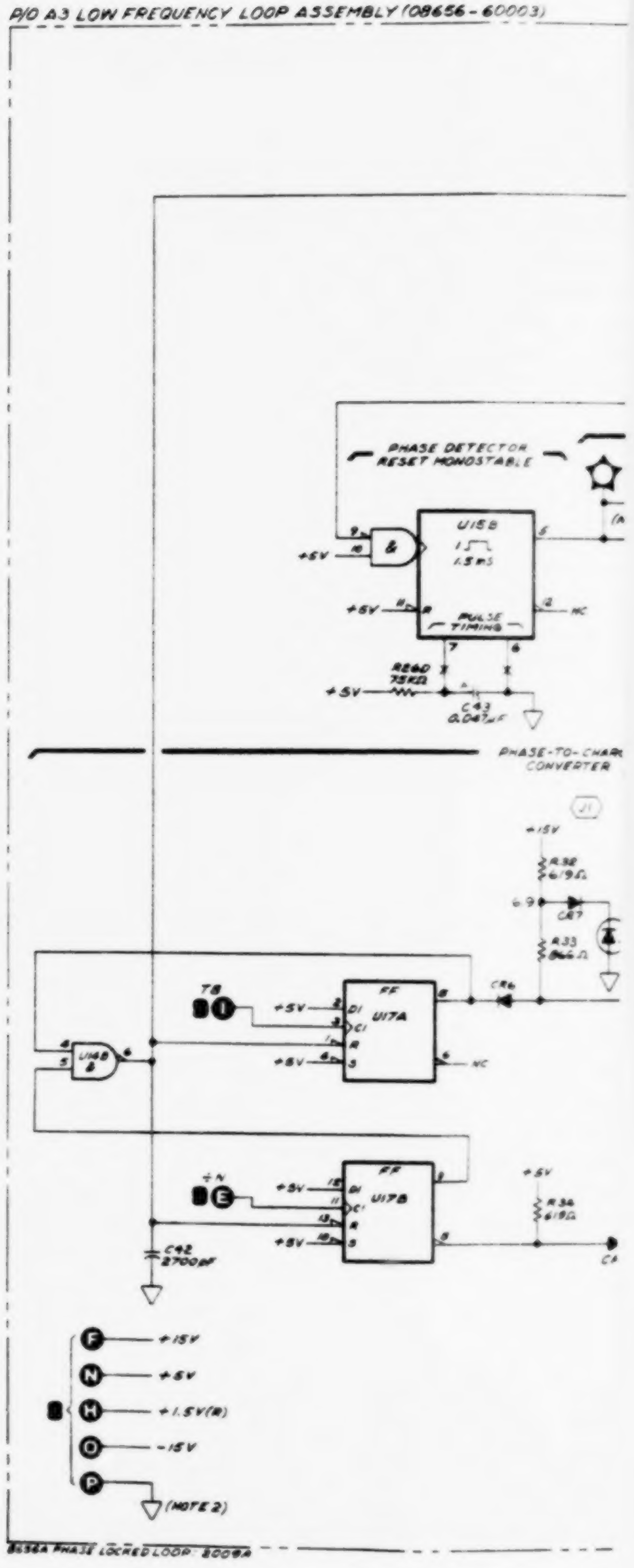
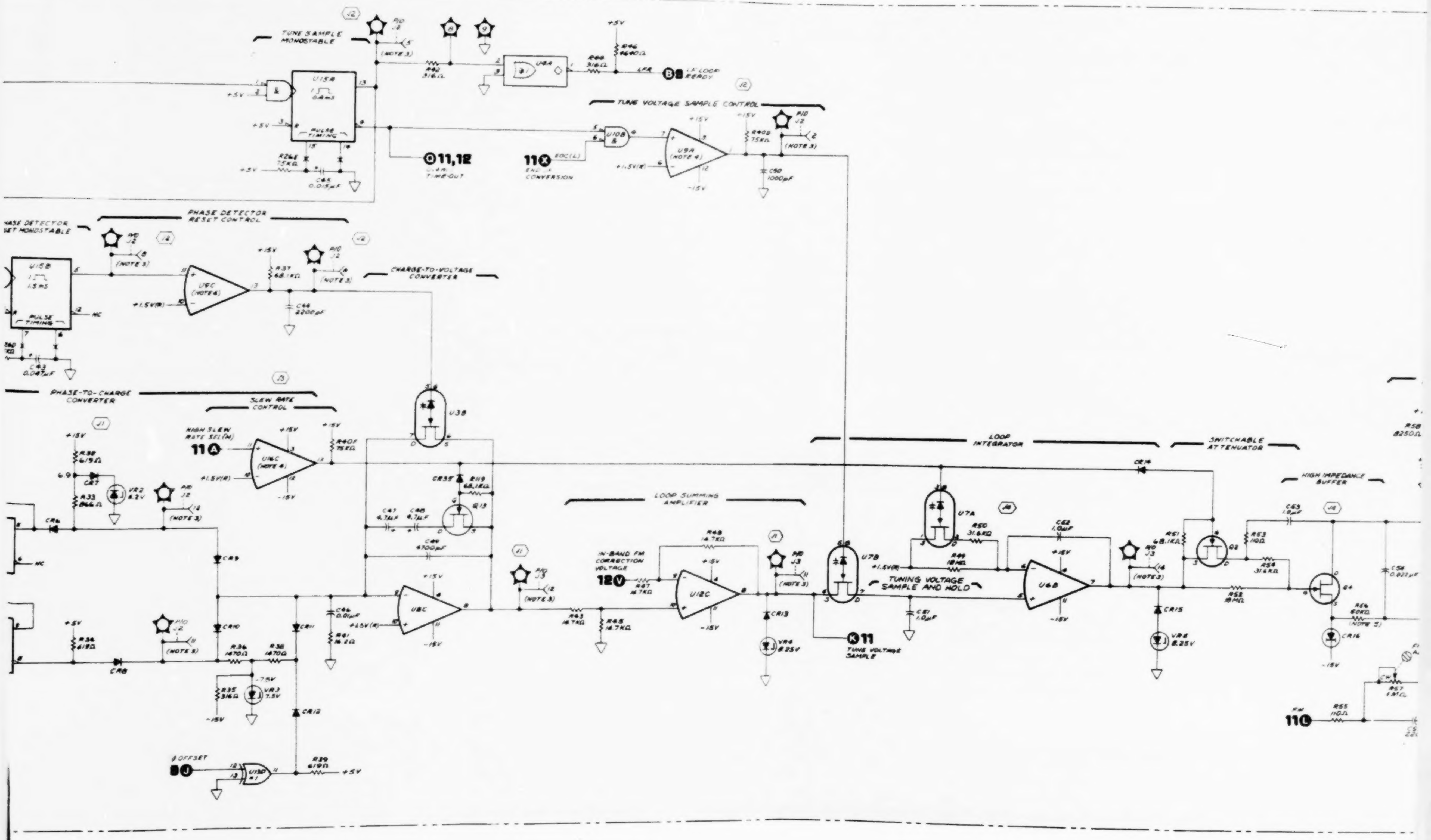
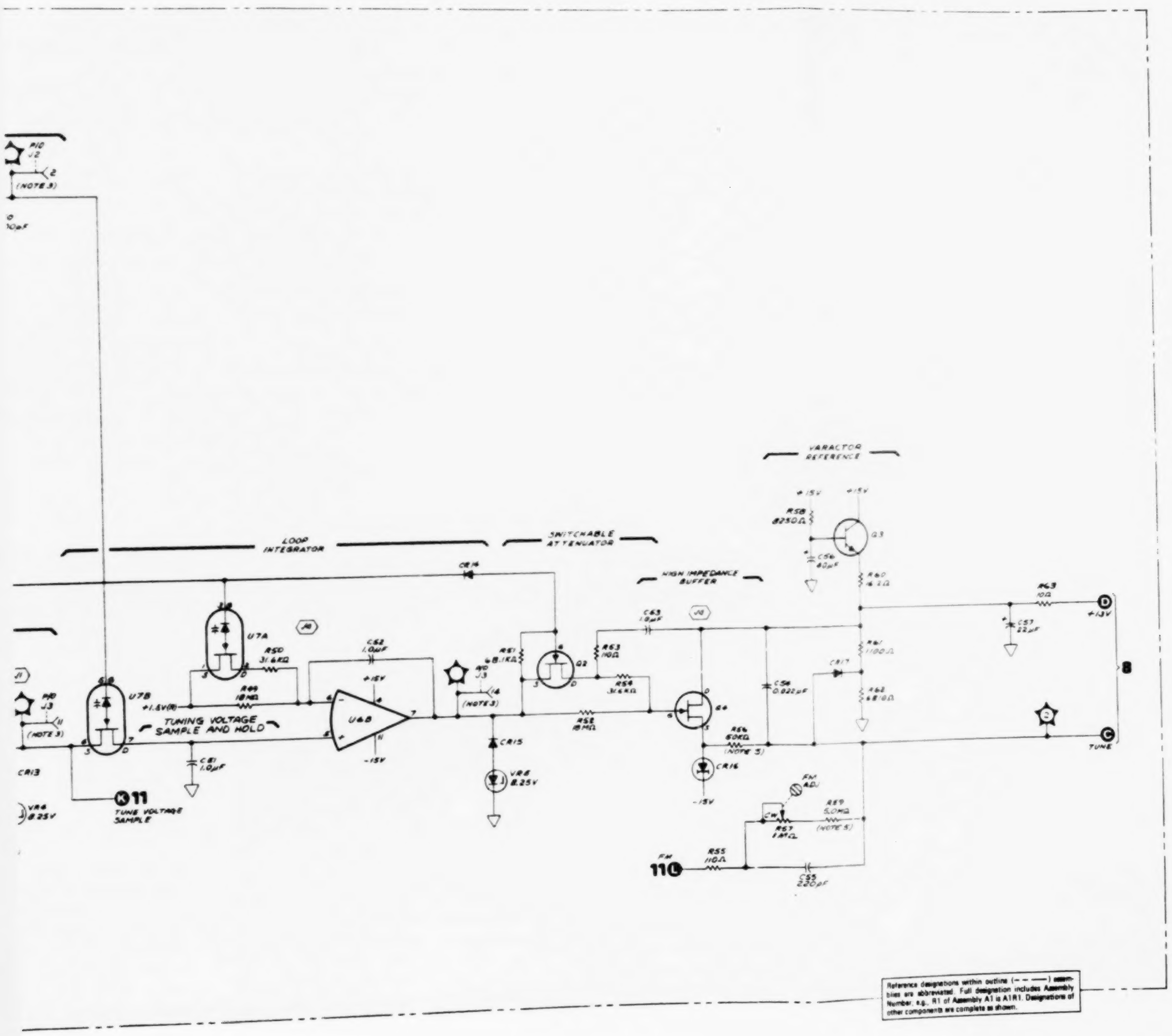

LF LOOP VCO
SS8
LF LOOP PHASE LOCK CIRCUIT
SS10
N
÷N
Φ OFFSET
LF LOOP READY
FM
LF LOOP DATA AND TIMING CONTROL
SS9
REFERENCE OSCILLATOR AND PHASE LOCK LOOP
SS13
TO HF LOOP FREQUENCY MULTIPLIER
LF LOOP FM CALIBRATOR
SS11
LF LOOP FM SYSTEM CONTROL AND CALIBRATION
SS12
FM RANGE
SERIAL INTERFACE
FROM LOW FREQUENCY LOOP
PHASE LOCKED LOOP
P/O A3 LOW FREQUENCY LOOP ASSEMBLY
TUNE SAMPLE MONOSTABLE
0.4 ms
LF LOOP READY
9
EOC
TUNE VOLTAGE SAMPLE CONTROL
11
END OF CONVERSION
PHASE DETECTOR RESET MONOSTABLE
1.5 ms
0.4 ms
11,12
0.4 ms TIME-OUT
PHASE DETECTOR RESET CONTROL
HIGH SLEW RATE SELECT (HIGH)
11
VARACTOR REFERENCE
LOOP INTEGRATOR
+11V
D8
T8
9
PHASE-TO-CHARGE CONVERTER
φ→C
9
÷N
CHARGE-TO-VOLTAGE CONVERTER
C→V
REF
9
φ OFFSET
12
IN-BAND FM CORRECTION VOLTAGE
LOOP SUMMING AMPLIFIER
REF
SWITCHABLE ATTENUATOR
HIGH IMPEDANCE BUFFER
TUNE
C8
11
FM
TUNE VOLTAGE SAMPLE AND HOLD
K11
TUNE VOLTAGE SAMPLE
10

Figure 8-71. LF Loop Phase Lock Circuits Block Diagrams


P/O A3 LOW FREQUENCY LOOP ASSEMBLY (08656-60003)
PHASE DETECTOR RESET MONOSTABLE
U15B
1.5ms
PULSE TIMING
+5V
R60 75KΩ
C43 0.047μF
PHASE-TO-CHARGE CONVERTER
+15V
R32 619Ω
CR7
R33 866Ω
CR6
T8
9
U17A
FF
U16B
NC
÷N
9
U17B
+5V
R34 619Ω
C42 2700pF
+15V
+5V
+1.5V(R)
-15V
(NOTE 2)
8656A PHASE LOCKED LOOP 2009A

'(08656-60003)


TUNE SAMPLE MONOSTABLE
U15A 0.4ms
PULSE TIMING
R26E 75KΩ
C45 0.015μF
R42 316Ω
U8A
R46 4640Ω
R44 316Ω
LFR
8B LF LOOP READY
(NOTE 3)
TUNE VOLTAGE SAMPLE CONTROL
11X EOC(L) END OF CONVERSION
U10B
U9A (NOTE 4)
R40D 75KΩ
C50 1000pF
D 11,12 LOOP TIME-OUT
PHASE DETECTOR RESET MONOSTABLE
PHASE DETECTOR RESET CONTROL
U15B 1.5ms
PULSE TIMING
C43 0.047μF
U9C (NOTE 4)
R37 68.1KΩ
C44 2200pF
CHARGE-TO-VOLTAGE CONVERTER
PHASE-TO-CHARGE CONVERTER
SLEW RATE CONTROL
HIGH SLEW RATE SEL(H)
11A
U16C (NOTE 4)
R40F 75KΩ
U3B
R32 619Ω
R33 866Ω
CR7
VR2 6.2V
CR6
CR9
CR35
R119 68.1KΩ
Q13
C47 4.7μF
C48 4.7μF
C49 4700pF
C46 0.01μF
R41 16.2Ω
U8C
CR10
CR11
R34 619Ω
CR8
R36 1470Ω
R38 1470Ω
R35 316Ω
VR3 7.5V
CR12
ϕ OFFSET
8J
U13D
R39 619Ω
LOOP SUMMING AMPLIFIER
IN-BAND FM CORRECTION VOLTAGE
12V
R47 14.7KΩ
R48 14.7KΩ
R43 14.7KΩ
R45 14.7KΩ
U12C
CR13
VR4 8.25V
U7B
K11 TUNE VOLTAGE SAMPLE
TUNING VOLTAGE SAMPLE AND HOLD
C51 1.0μF
LOOP INTEGRATOR
U7A
R50 31.6KΩ
R49 10MΩ
C52 1.0μF
U6B
CR14
CR15
VR6 8.25V
SWITCHABLE ATTENUATOR
R51 68.1KΩ
Q2
R53 110Ω
R54 31.6KΩ
R52 10MΩ
HIGH IMPEDANCE BUFFER
C53 1.0μF
C56 0.022μF
Q4
R56 60KΩ (NOTE 5)
CR16
R57 1MΩ
FM 11L
R55 110Ω
R58 8250Ω
+5V
+15V
-15V
-7.5V
+1.5V(R)
NC


P10
J2
2
(NOTE 3)
0
10µF
LOOP INTEGRATOR
SWITCHABLE ATTENUATOR
HIGH IMPEDANCE BUFFER
VARACTOR REFERENCE
CR14
U7A
A11
R50
31.6KΩ
C62
1.0µF
+15V
-15V
U7B
+1.5V(R)
R49
18MΩ
TUNING VOLTAGE SAMPLE AND HOLD
U6B
J11
P10
J3
11
(NOTE 3)
C61
1.0µF
CR13
K11
TUNE VOLTAGE SAMPLE
VR4
8.25V
P10
J3
14
(NOTE 3)
CR15
VR6
8.25V
R51
68.1KΩ
Q2
R52
18MΩ
R53
110Ω
R54
31.6KΩ
C63
1.0µF
J10
Q4
R56
60KΩ
(NOTE 5)
CR16
-15V
C54
0.022µF
+15V
+15V
R58
8250Ω
Q3
C56
40µF
R60
16.2Ω
R61
1100Ω
CR17
R62
6810Ω
FM ADJ
R59
5.0MΩ
(NOTE 5)
CW
R57
1MΩ
FM
11L
R55
110Ω
C55
220pF
R63
10Ω
C57
22µF
D
+13V
2
C
TUNE
8

Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number, e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A3J1-4 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. SERVICE TEST POINT PIN OF DUAL IN-LINE TEST SOCKET J2 OR J3.
4. OPEN COLLECTOR DEVICE.
5. MATCHED FOR TEMPERATURE CHARACTERISTICS.

REFERENCE DESIGNATIONS

A3
C42-57 CR6-17,35 J2,3 Q2-4,13 R26,32-63,119 TP2,8,9 U3,4,6-10,12-17 VR2-5

LOGIC LEVELS

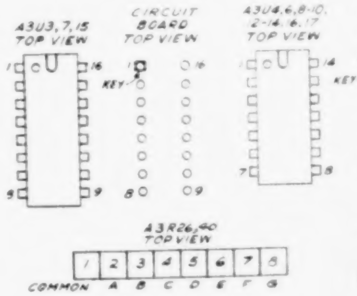
	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG THAN > IS MORE POS THAN	
OPEN	HIGH
GROUND	LOW

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q2,13	1855-0414
Q3	1854-0071
Q4	1855-0288
U3,7	1858-0066
U4	1820-1272
U6,8,12	1826-0522
U9,16	1826-0174
U10	1820-1144
U13	1820-1211
U14	1820-0681
U15	1820-1423
U17	1820-1112

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U4,10,13,14,17	+5V - 14 ▽ - 7
U15	+5V - 16 ▽ - 8


A3U3,7,15
TOP VIEW
1
16
9
9
CIRCUIT BOARD
TOP VIEW
1
KEY
16
8
9
A3U4,6,8-10,
12-14,16,17
TOP VIEW
1
14
7
8
CIRCUIT BOARD
TOP VIEW
1
KEY
14
7
8
A3R26,40
TOP VIEW
1
2
3
4
5
6
7
8
COMMON
A
B
C
D
E
F
G

10
P/O A3

Figure 8-72. LF Loop Phase Lock Circuits Schematic Diagram

SERVICE SHEET 11
P/O A3 LOW FREQUENCY LOOP ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The voltage-to-frequency sensitivity of the Signal Generator's VCO is non-linear. To guarantee calibrated frequency modulation, the gain of the audio modulation drive signal is varied by the FM Calibration circuits. Refer to Figure 1 for a simplified diagram of the calibration circuits. The FM Calibration Signal Generator (found on Service Sheet 12) provides the FM reference signal and the VCO modulation signal required to calibrate the modulation drive level. Passing the FM calibration signal through an integrator U12D (found on Service Sheet 12) provides the same signal as passing the frequency modulated VCO signal through the phase detector (found on Service Sheet 10). These signals are input to the Loop Summing (difference) Amplifier (of Service Sheet 10). This difference signal is input to the Low Offset Comparator. The output tells the SAR whether the DAC should increase or decrease in attenuation to cancel the signal from the Loop Summing Amplifier. In successive steps the signal is reduced until after 8 steps the DAC attenuation is calibrated with the data being held in the SAR, U2.

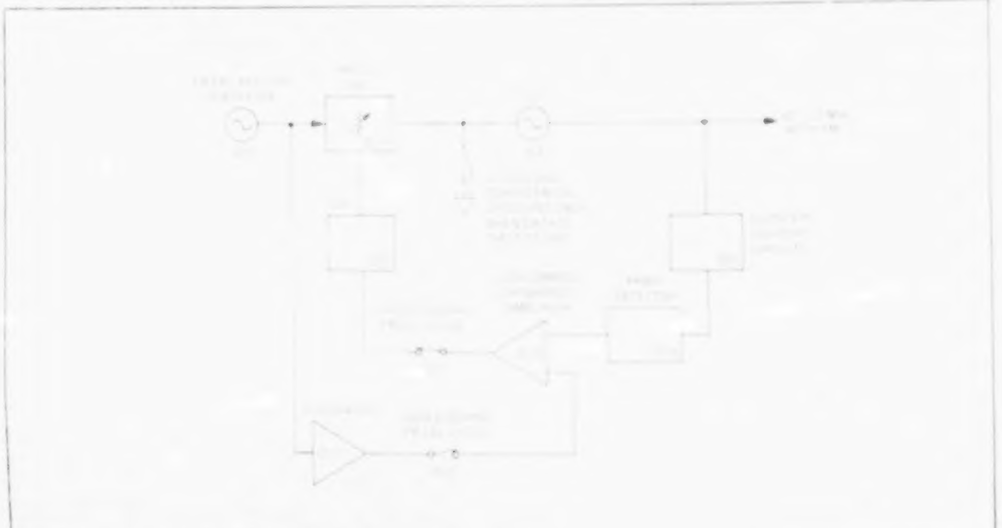


Figure 1. FM Calibration Simplified Block Diagram

If the Signal Generator's frequency is changed so the 25.6 kHz band edge is passed, WSTB(L) triggers the High Slew Rate Monostable U21B. The outputs of U21B inhibit the FM calibration circuits and enable the SAR Clock Generator by causing U5A to be set. At the end of the high slew rate mode, the Pre-Cal Settling Monostable is triggered. During the Pre-Cal Settling time the LF Loop is phase locked. When the settling time ends, the SAR Clock Generator's K input to U5A is set high and the Successive Approximation Register is enabled. The two lows to U13B cause a low to be output to the SAR's Feed Forward Input. The Start Conversion Monostable is triggered which couples a high to the Start Conversion input. The Conversion Cycle begins and the

SERVICE SHEET 11 (Cont'd)

EOC output from the SAR goes low. Serial data is input at U2-pin 6 and converted to the parallel data that drives the DAC.

High Slew Rate Mode

When the Low Frequency Loop VCO's frequency is changed so that the 25.6 kHz band edge is passed, the Microprocessor word written to the LF Loop Shift Register (refer to Service Sheet 9) contains a high bit at register U25A-Pin 3. This allows the Write Strobe Generator D Flip-Flop U28B to be set when it is clocked by monostable U21A's active-low output low-to-high transition. (Refer to Table 1). The low output of U28B then triggers the High Slew Rate Monostable U21B placing the instrument in the high slew rate mode for approximately 500 ms. Refer to Table 2.

Table 1. U28B (P/O Write Strobe Generator) Operation (refer to Service Sheet 9)

S	R	C	D	Pin-9	Pin-8	Remarks
H	L	X	X	L	H	
H	H	↑	H	H	L	Change passes 25.6 kHz band edge.
H	H	↑	L	L	H	

Table 2. U21B High Slew Rate Monostable Operation

Pin-9	Pin-10	Pin-11	Pin-5	Pin-12	Pulse Duration
↓	+5V	+5V	⎍	⊔	500 ms

The 500 ms pulse duration is determined by R26C 75 kΩ and C58 15 μF. The active-high output pulse is applied to the Slew Rate Control comparator U16C (shown on Service Sheet 10) to close the High Slew Rate FET switches. The active-high output is also applied to Exclusive-Or gate U13B whose output goes high since the other input is low. The high input to the Successive Approximation Register's Feed Forward input stops a conversion which may have been started or prevents a conversion from taking place.

Pre-Cal Settling Monostable

The active-low output (low) of U21B is applied to Pre-Cal Settling Monostable U11B-pin 10. U11B is triggered on the low-to-high transition of the 500 ms pulse. The active-high output goes high and the active-low output low for 1.1s. Refer to Table 3. It is during this time that the LF Loop finishes locking in the low slew rate mode. The active-high output of U11B is the second input to Exclusive-Or gate U13B. The first input (from the High Slew Rate Monostable) has just gone low. Therefore, U11B's active-high output being high keeps U13B's output high. The high input to the Feed Forward input of the Successive Approximation Register terminates and/or prevents conversion as noted.

SERVICE SHEET 1

Table 3. U

Pin-9	Pin-10
L	↑
↓	H

Calibration Cycle

At the end of the P
U11B goes low. The
and U11A. The outp
Forward input of U
triggered by the high
high at the Start C
Approximation Reg

Table 4. U

Pin-1	Pin-2
↓	+5V

The active-low outp
This is connected to
the SAR Clock Gene
the low active-low o
The set input return
mode.

Table 5.

S	R
L	H
H	H
H	H
T Toggles to ne	

At the end of the 1
making the K inpu
remain low forcing
Pin 11 is pulsed lo
Sample Monostable
input to comparato
10 or 4 ms, and the
mately -15 to +15
Register on the posi
pulse is received fr
clocked for eight su
of the SAR takes pla
kHz band edge is pa
precisely predictabl

SERVICE SHEET 11 (Cont'd)

Table 3. U11B Pre-Cal Settling Monostable Operation

Pin-9	Pin-10	Pin-11	Pin-5	Pin-12	Pulse Duration
L	↑	+5V	⎍	⊔	1.1s
↓	H	+5V	⎍	⊔	1.1s

Calibration Cycle

At the end of the Pre-Cal Settling cycle, the active-high output of U11B goes low. The active-high output of U11B is applied to U13B and U11A. The output from U13B goes low which enables the Feed Forward input of U2. The Start Conversion Monostable U11A is triggered by the high-to-low transition of the output of U11B. With a high at the Start Conversion Monostable's output, the Successive Approximation Register's conversion cycle is started.

Table 4. U11A Start Conversion Monostable Operation

Pin-1	Pin-2	Pin-3	Pin-13	Pin-4	Pulse Duration
↓	+5V	+5V	⎍	⊔	25 ms

The active-low output of Pre-Cal Settling Monostable is low for 1.1s. This is connected to the K input of the J-K Flip-Flop that is part of the SAR Clock Generator U5A. U5A's active-low output is set lowby the low active-low output of U21B during the high slew rate mode. The set input returns high after 500 ms at the end of high slew rate mode.

Table 5. U5A (P/O SAR Clock Generator) Operation

S	R	G	J	K	Pin-5	Pin-6
L	H	X	X	X	H	L
H	H	↓	L	H	L	H
H	H	↓	L	L	T	T
T-Toggles to next state						

At the end of the 1.1s Pre-Cal Settling time, U11B changes state making the K input to U5A high. U5A's active-low output will remain low forcing the input to U10D low. Every 10 or 4 ms, U10D-Pin 11 is pulsed low for 0.4 ms by the active-low output of Tune Sample Monostable U15A (shown on service sheet 10). The positive input to comparator U9D-Pin 9 will be pulsed high for 0.4 ms every 10 or 4 ms, and the output of U9D-Pin 14 switches from approximately −15 to +15 volts clocking the Successive Approximation Register on the positive edge of each pulse after the start conversion pulse is received from U11A. The calibration data to the SAR is clocked for eight successive clock pulses (about 80 ms). Calibration of the SAR takes place each time the frequency is changed if the 25.6 kHz band edge is passed. Since the FM sensitivity of the VCO is not precisely predictable with frequency it must be calibrated electronically. The data input to the SAR is the calibration input and sets the SAR's output. The SAR's output is used to set the FM CAL DAC U1. The FM CAL DAC is set to compensate for the FM sensitivity of the VCO. The End of Conversion EOC(H) output-Pin 11 of the SAR U2 goes high when the conversion is complete. The EOC(H) is normally high and is set low during the 80 ms calibration cycle. The EOC(L) from Nor gate U10C is normally low and is high during the calibration cycle. When EOC(L) goes low, the high-to-low transition clocks J-K Flip Flop U5A which outputs a high at the active-low output. The clock gate U10D is inhibited which disables the SAR clock generator.

SERVICE SHEET 11 (Cont'd)

Low Slew Rate Mode

If the frequency of the VCO is changed so that the 25.6 kHz band edge is not reached, the Signal Generator does not enter the high slew rate mode. (High Slew Rate Monostable U21B does not get triggered.) The Shift Data Output (low) of the Write Strobe Generator Monostable U21A (refer to Service Sheet 9) is set low for 75 µs. This input is applied to U4B. U4B stays low because the other input (from the active-low output of U5A) stays high. Therefore, the LF Loop stays in the low slew rate mode and FM calibration does not take place.

Data Entry During FM Calibration

If new frequency data is entered into the LF Loop while the LF Loop is in the FM calibration phase, the FM calibration is terminated. The shift Data Low output of Write Strobe Generator Monostable (shown on service sheet 9) is gated by Nor gate U4B. The active-low output of U5A is low during the FM Calibration of the LF Loop which enables U4B. When Shift Data (L) goes low for 75 µs, the output will go high for 75 µs. The high-to-low transition of U4B's output triggers the Pre Cal Settling Monostable U11B setting the active-high output high and the active-low output low. The active-high output of U11B to NOR gate U13B sets its output high since the other input is low. The high output of U13B to Feed Forward input of Successive Approximation Register U2 terminates and prevents conversion from taking place. This terminates the FM Calibration of the LF Loop until the active-high output of U11A Start Conversion Monostable goes low 35 ms after the Pre Cal Settling Monostable U11B goes low.

Low Offset Comparator Circuits

The Low Offset Comparator is enabled by the Low Offset Comparator Control during the Low Frequency Loop's FM Calibration Cycle. The Low Offset Comparator converts the difference between the VCO phase deviation and the integrated FM modulation drive signal (In-band FM Correction Voltage) to a digital input to the SAR. U13A controls the timing of the data input to the SAR based on the input from the FM Calibration Signal Generator. U5B, U9D of the SAR clock Generator and U16D of the Low Offset Comparator Control are all triggered by the 0.4 ms Time Out from the active-low output of Tune Sample Monostable U15A. The output is pulsed low for 0.4 ms every 4 or 10 ms.

SERVICE SHEET 11 (Cont'd)

The EOC(L) input to U14D is low except during the FM calibration period. The 0.4 ms Time Out is high and pulses low for 0.4 ms every 4 or 10 ms. With the EOC(L) input high, the output is high for 0.4 ms. The high input to the positive input of comparator U16D means the output is near +15 volts. The +15 volts controls the gate of FET switches U18B and C causes them to be closed. The positive input to the Low Offset Comparator is connected to ground. U12B becomes a unity gain amplifier because U18B shorts the output to the negative input and removes any offset voltage stored on C68. At this point, assume the frequency of the LF VCO is changed by selecting a new output frequency. Assume also that the VCO's frequency passes a 25.6 kHz band edge. The LF Loop will go into high slew rate mode for 500 ms moving the VCO frequency close to the correct frequency. The loop then enters the Pre-Cal Settling mode for 1.1 s to complete locking the LF VCO at the correct frequency. Then the LF Loop enters the FM Calibration mode for 80 ms. It is in this mode that the SAR is set. This, in turn, sets the FM Cal DAC to calibrate the FM modulation drive of the VCO. When FM calibration is started, the EOC(L) goes high until all bits of the SAR have been set. The EOC(L) input to U14D is high and the 0.4 ms Time Out is high except for the 0.4 ms pulses every 10 ms. Therefore, the output of U14D will be pulsed low. With the output low, comparator U16D's output is near −15 Vdc opening FET switches U18B and C. During this time the Tune Voltage to the LF VCO is fixed and the VCO frequency does not change. The VCO is frequency modulated by the FM Calibration Generator signal which is a function of the SAR Data Control. Any Tune Voltage Sample input to Low Offset Comparator U12B which is not ac grounded is applied to the positive input. Now the Tune Voltage Sample from the Loop Summing Amplifier U12C will control the Low Offset Comparator U12B. The output of the comparator and the SAR Data Control from J-K Flip-Flop U5B, part of FM Calibration Signal Generator, are the inputs to Exclusive-Or gate U13A. The output of U13A is the data input to the SAR which calibrates the FM sensitivity of the VCO by nulling the input to comparator U12B.

The output of the Low Offset Comparator is switched from near +15 to 0 Vdc and is connected through R68 to U13A. The output of U13A is the data input to the SAR whose output sets the FM CAL DAC. The SAR bits are set to control the DAC (which acts as a variable attenuator) to achieve a null on the Tune Voltage Sampler input during the FM calibration cycle.

FM Cal DAC, Converter, and Sample and Hold Buffer

The FM Reference input to the FM CAL DAC is the signal to FM the VCO using internal or external modulation signals or the FM calibration signal during the FM calibration cycle. The FM input signal is attenuated for VCO sensitivity and applied to the current to voltage converter U6A. The signal then is applied to the DAC Offset Sample and Hold Buffer U6C. The ac voltage from U6C is applied to the VCO Tune Voltage bus shown on Service Sheet 10. FET switches U7C and D are open (biased off) except during FM calibration.

SERVICE SHEET 11 (Cont'd)

During FM calibration the two FET switches are closed and the gate goes to near +15 Vdc when the SAR receives a clock pulse to input data. This effectively grounds the input to U6C during the time data is input to the SAR. The new SAR bit settings are loaded into the FM CAL DAC and then the FET switches are opened to let the adjusted FM cal signal be applied to the VCO thereby adjusting the VCO's FM sensitivity.

TROUBLESHOOTING

Procedures for checking circuits of part of A3 Low Frequency Loop Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g., √3 . Fixed voltages are shown on the schematic inside a hexagon, e.g. 2V±0.2V . Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Oscilloscope	
Storage Mainframe	HP 181A
Vertical Amplifier	HP 1801A
Time Base	HP 1820C

√1 High Slew Rate Monostable, Pre-Cal Settling Monostable, Start Conversion Monostable

1. Set the Signal Generator's frequency to 500 MHz without modulation.

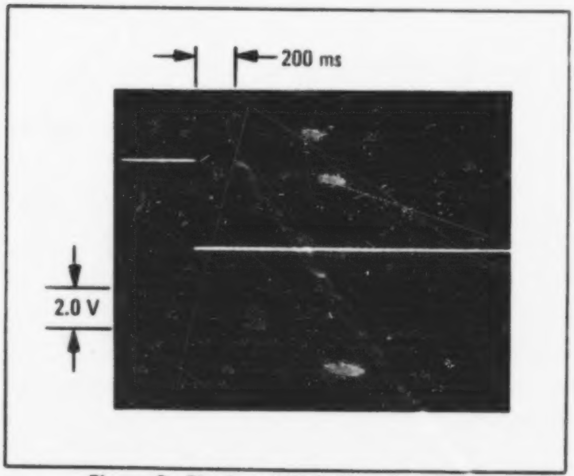


Figure 2. Display of High Slew Rate Pulse (coupling is dc toJ2-Pin 7: external trigger is from U21B-Pin 9)

2. Increase the frequency in 10 MHz steps. Verif that the waveforms are the same as those of Figures 2, 3 and 4. The loop is being phase locked.

NOTE

When the frequency change of the LF Loop passes a 25.6 kHz band edge, the high slew rate mode is triggered.

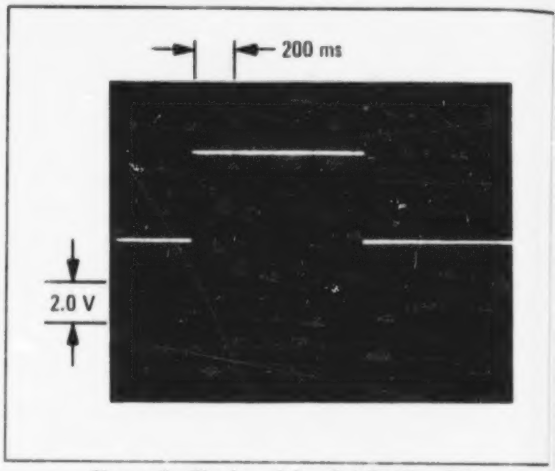


Figure 3. Display of Pre-Cal Settling Pulse (coupling is dc to J2-Pin 9; external trigger is from U21B-Pin 9)

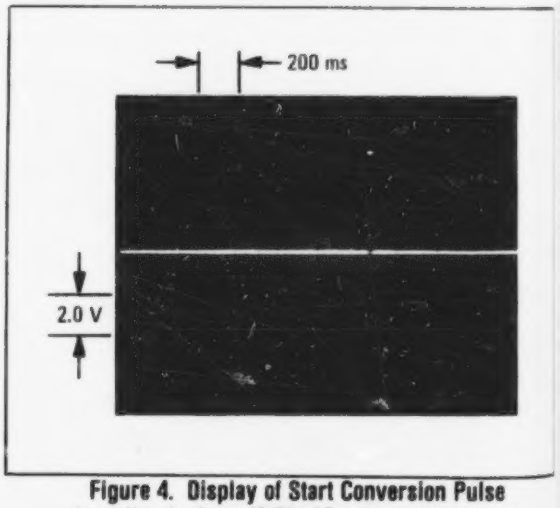


Figure 4. Display of Start Conversion Pulse (coupling is dc to J2-Pin 10; external trigger is from U21B-Pin 9)

NOTES

Pin 10 of the Successive Approximation Register U2 will be high until the active-high output pulse of the Pre-Cal Settling Monostable goes low.

SERVICE SHEET 11 (Cont'd)

NOTES (Cont'd)

The Successive Approximation Register's conversion cycle is started when the active-high output pulse of the Start Conversion Monostable is terminated, high to low.

⟨√2⟩ SAR Clock Generator, Successive Approximation Register

NOTES

The Successive Approximation Register's conversion cycle is started when the active-low output of J-K Flip-Flop U5A is low. A 0.5 ms clock pulse is generated every 10 or 4 ms by the Tune Sample Monostable's active-low output pulse.

On each clock pulse to the SAR, the SAR's outputs are set high or low depending on the Data in. As each of the bits are set, the FM Cal DAC gets set.

A total of eight clock pulses are required to set the Output of the SAR (to calibrate the system). Total time is approximately 80 ms.

Clock pulses are generated from the time the High Slew Rate Monostable's active-low output sets the active-low output of the J-K Flip-Flop U5A low.

1. Set the Signal Generator to 500 MHz without modulation.

2. Increment the frequency up 10 MHz and compare the displayed waveforms to those shown in Figures 5 and 6. Refer to ⟨√3⟩ to verify SAR Data input during the FM calibration cycle.

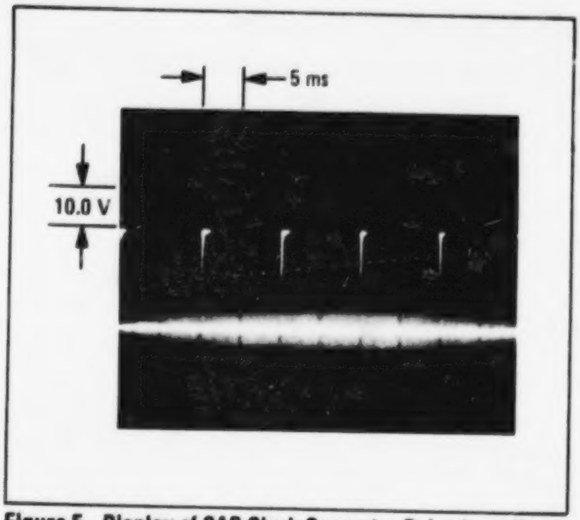


Figure 5. Display of SAR Clock Generator Pulse (coupling is dc to U9D-Pin 14; external trigger from J2-Pin 10)

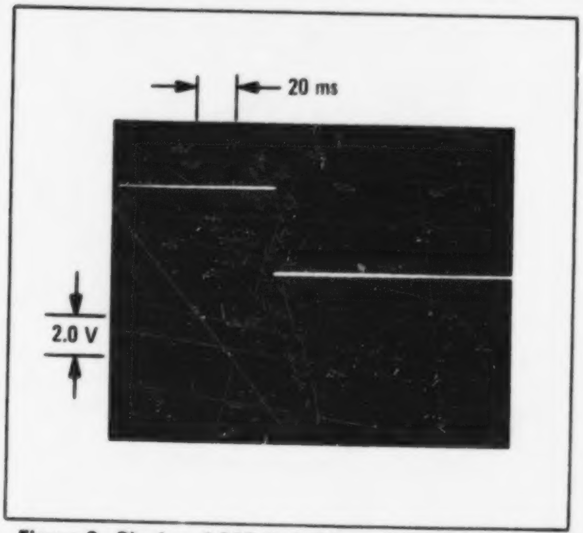


Figure 6. Display of SAR End of Conversion EOC(L) Level (coupling is dc to J2-Pin 6; external trigger from J2-Pin 10)

SERVICE SHEET 11 (Cont'd)

√3 Low Offset Comparator Control, Low Offset Comparator

NOTES

The correction Tune Voltage Sample input to the Low Offset Comparator will control the comparator's output.

The comparator's output is Exclusive-Or'ed with the integrated FM calibration signal to set the SAR bits high or low.

1. Increment the frequency up 10 MHz and check the oscilloscope displays, Figures 7 and 8 for typical FM calibration data.

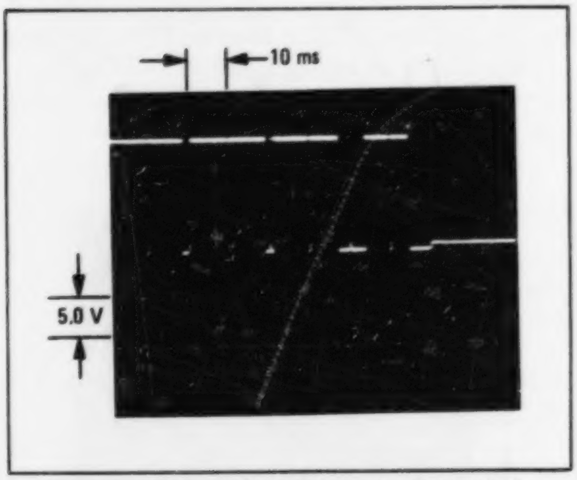


Figure 7. Display of Offset Comparator Output during FM Calibration Cycle (coupling is dc to J3-Pin 16 with external trigger from J2-Pin 10)

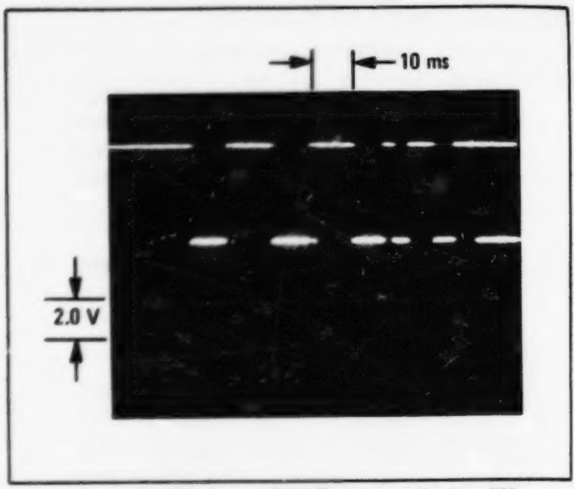


Figure 8. Display of SAR Data Input during FM Calibration Cycle (coupling is dc to U13A-Pin 3; external trigger from J2-Pin 10)

√4 FM Cal DAC, Current-to-Voltage Converter, DAC Offset Sample and Hold Buffer

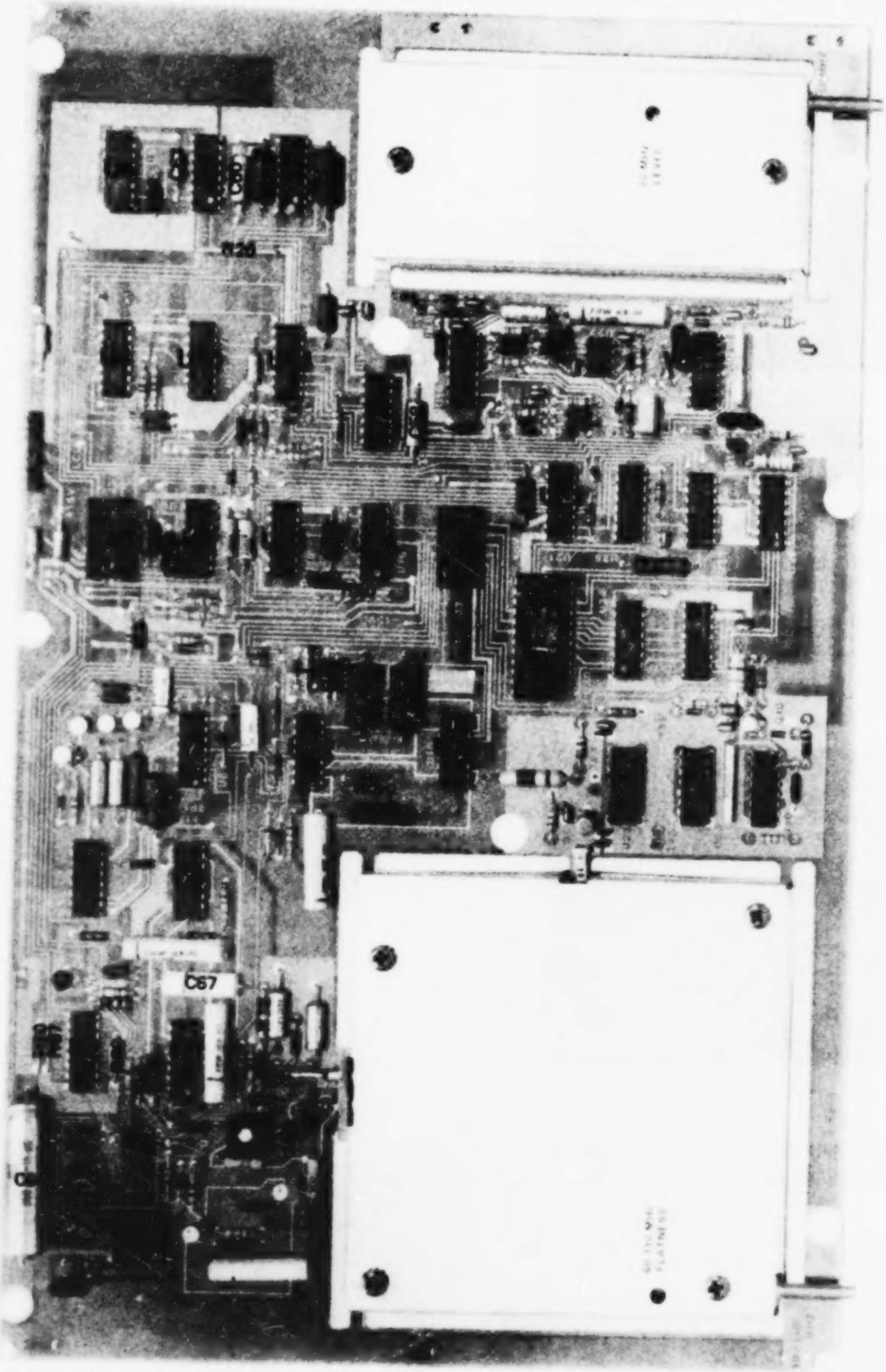
1. Set the Signal Generator frequency to 500 MHz, modulation source Internal 1 kHz, FM mode and 50 kHz deviation.

2. Check the following.

   a. J2-Pin 13, FM Reference, for a 1 kHz signal approximately 4.0 Vp-p.

   b. U6A-Pin 1 for a 1 kHz signal approximately 2.5 Vp-p.

   c. J3-pin 13 for a 1 kHz signal approximately 2.5 Vp-p.



P/O A3 ASSEMBLY

Figure 8-73. LF Loop FM System Calibrator Component Locations

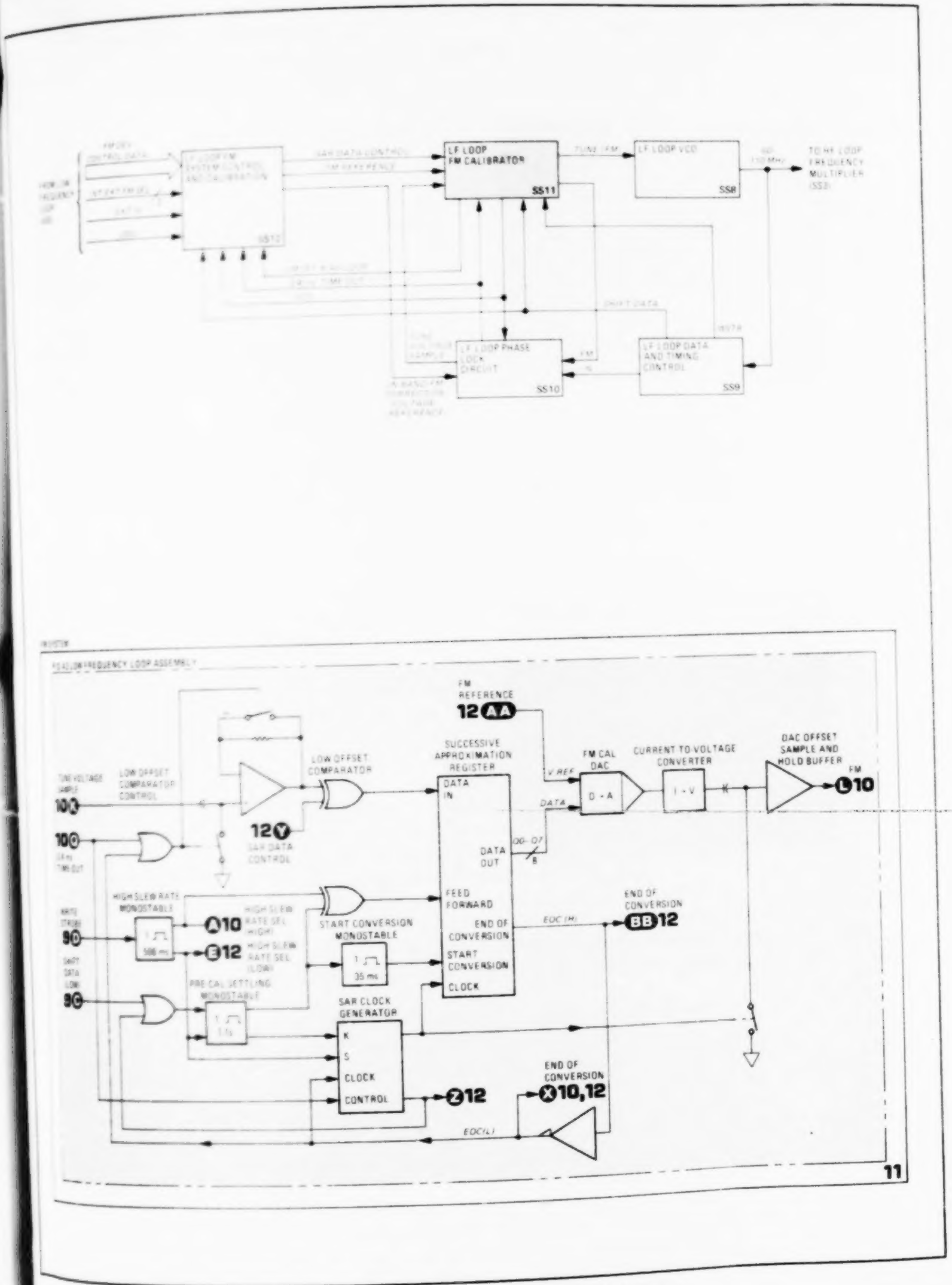
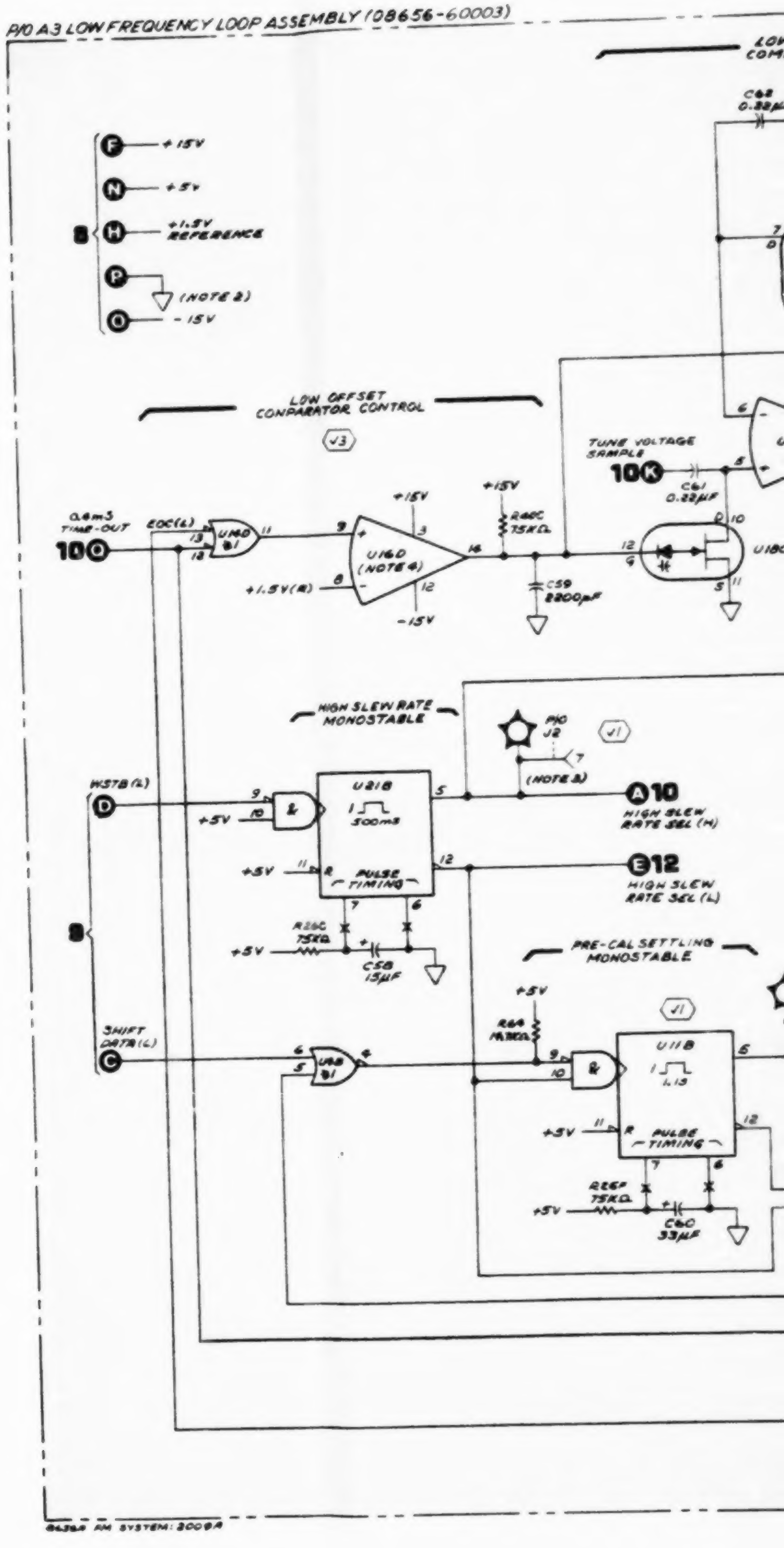
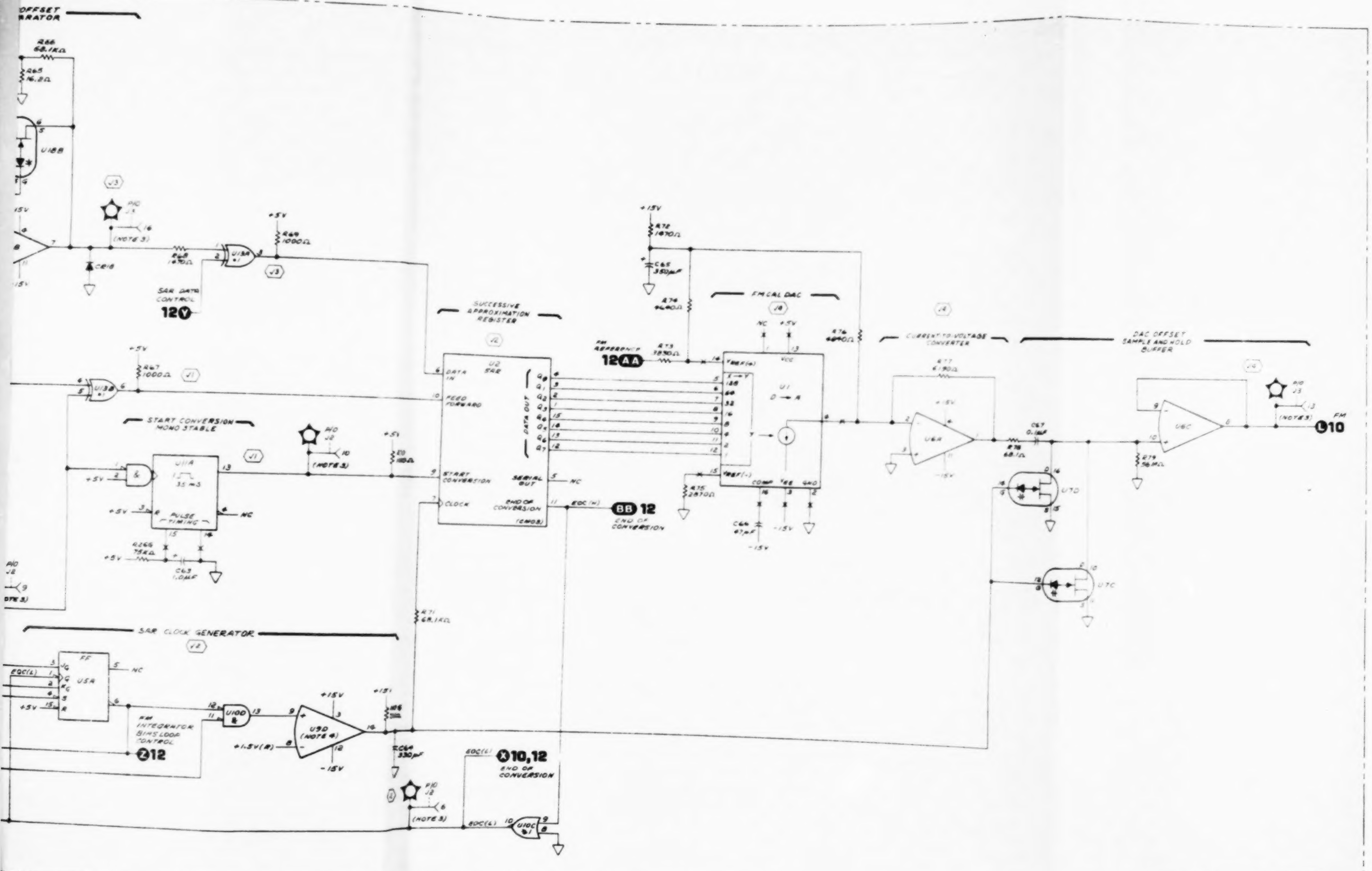

LF LOOP FM CALIBRATOR
SS11
LF LOOP VCO
SS8
TUNE (FM)
SAR DATA CONTROL
FM REFERENCE
TO HF LOOP FREQUENCY MULTIPLIER (SS3)
SS12
LF LOOP PHASE LOCK CIRCUIT
SS10
LF LOOP DATA AND TIMING CONTROL
SS9
SHIFT DATA
FM
TUNE VOLTAGE SAMPLE
A3 LOW FREQUENCY LOOP ASSEMBLY
TUNE VOLTAGE SAMPLE
10K
LOW OFFSET COMPARATOR CONTROL
LOW OFFSET COMPARATOR
12Y
SAR DATA CONTROL
10O
0.4 ms TIME OUT
FM REFERENCE
12AA
SUCCESSIVE APPROXIMATION REGISTER
DATA IN
DATA OUT
D0 - D7
8
FEED FORWARD
END OF CONVERSION
START CONVERSION
CLOCK
V REF
DATA
FM CAL DAC
D + A
CURRENT TO VOLTAGE CONVERTER
I + V
DAC OFFSET SAMPLE AND HOLD BUFFER
FM
L10
RATE STROBE
9D
HIGH SLEW RATE MONOSTABLE
500 ms
A10
HIGH SLEW RATE SEL (HIGH)
E12
HIGH SLEW RATE SEL (LOW)
START CONVERSION MONOSTABLE
35 ms
SHIFT DATA LOW
9C
PRE CAL SETTLING MONOSTABLE
1.1s
SAR CLOCK GENERATOR
K
S
CLOCK
CONTROL
Z12
EOC (H)
END OF CONVERSION
BB12
END OF CONVERSION
X10,12
EOC(L)
11

Figure 8-74. LF Loop FM System Calibrator Block Diagrams


P/O A3 LOW FREQUENCY LOOP ASSEMBLY (08656-60003)
F +15V
N +5V
H +1.5V REFERENCE
P (NOTE 2)
O -15V
8
LOW OFFSET COMPARATOR CONTROL
√3
0.4mS TIME-OUT
10O
EOC(L)
U14D
U16D (NOTE 4)
+1.5V(R)
+15V
-15V
R48C 75KΩ
C59 2200pF
TUNE VOLTAGE SAMPLE
10K
C61 0.22µF
C62 0.22µF
U18C
HIGH SLEW RATE MONOSTABLE
P/O J2
√1
(NOTE 3)
HSTB(L)
D
U21B
500mS
PULSE TIMING
A10
HIGH SLEW RATE SEL (H)
E12
HIGH SLEW RATE SEL (L)
R26C 75KΩ
C58 15µF
+5V
PRE-CAL SETTLING MONOSTABLE
SHIFT DATA(L)
C
U8B
R64 14.7KΩ
U11B
1.1S
R26F 75KΩ
C60 33µF
8656A FM SYSTEM: 2009A


OFFSET
RATOR
R66 68.1KΩ
R65 16.2Ω
U18B
J3
P/O J3
16
(NOTE 3)
15V
-15V
CR18
R68 1470Ω
U13A =1
+5V
R69 1000Ω
SAR DATA CONTROL
12V
SUCCESSIVE APPROXIMATION REGISTER
J2
+5V
R67 1000Ω
J1
U13B =1
START CONVERSION MONO STABLE
U11A
35 mS
PULSE TIMING
NC
R266 75KΩ
C63 1.0µF
P/O J2
10
(NOTE 3)
9
+5V
R70 118Ω
U2 SAR
DATA IN
FEED FORWARD
START CONVERSION
CLOCK
DATA OUT
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
SERIAL OUT
END OF CONVERSION
(CMOS)
EOC (H)
BB 12
END OF CONVERSION
R71 68.1KΩ
SAR CLOCK GENERATOR
FF
U5A
EOC(L)
FM INTEGRATOR BIAS LOOP CONTROL
Z12
U10D &
U9D (NOTE 4)
+15V
-15V
+1.5V(R)
R106
C64 330pF
P/O J2
6
(NOTE 3)
X10,12
END OF CONVERSION
U10C =1
+15V
R72 1470Ω
C65 350µF
R74 9640Ω
FM REFERENCE
12AA
R73 3830Ω
FM CAL DAC
J4
NC
+5V
VREF(+)
VCC
I → V
128 64 32 16 8 4 2 1
U1
D → A
VREF(-)
COMP
VEE
GND
R75 2870Ω
C66 47pF
-15V
R76 4640Ω
CURRENT-TO-VOLTAGE CONVERTER
R77 6190Ω
U6A
C67 0.1µF
R78 68.1Ω
U7D
U7C
DAC OFFSET SAMPLE AND HOLD BUFFER
R79 56MΩ
U6C
P/O J3
13
(NOTE 3)
FM
L10

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number, e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A3J1-4 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKET J2 OR J3.
4. OPEN COLLECTOR DEVICE.

REFERENCE DESIGNATIONS

A3
C58-67 CR18 J2,3 R26,40,64-79 U1,2,4-7,9-14,16,18,21

LOGIC LEVELS

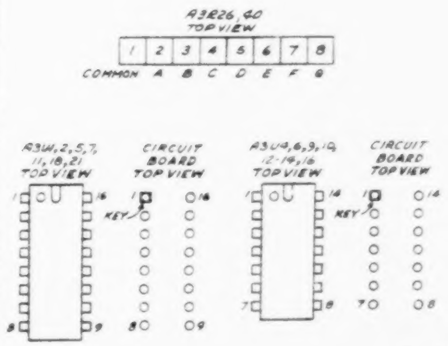
	TTL	CMOS
HIGH	>2V	>3.5V
LOW	<0.8V	<1.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1	1826-0188
U2	1820-1722
U4	1820-1272
U5	1820-1212
U6,12	1826-0522
U7,18	1858-0066
U9,16	1826-0174
U10	1820-1144
U11,21	1820-1423
U13	1820-1211
U14	1820-0681

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2,5,11,21	+5V - 16 ▽ - 8
U4,10,13,14	+5V - 14 ▽ - 7


A3R26,40
TOP VIEW
1 2 3 4 5 6 7 8
COMMON A B C D E F G
A3U1,2,5,7,11,18,21
TOP VIEW
CIRCUIT BOARD
TOP VIEW
KEY
A3U4,6,9,10,12-14,16
TOP VIEW
CIRCUIT BOARD
TOP VIEW
KEY

11
P/O A3

Figure 8-75. LF Loop FM Calibrator Schematic Diagram

SERVICE SHEET 12
P/O A3 LOW FREQUENCY LOOP ASSEMBLY
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The FM drive signals from internal or external sources are input to the FM Deviation Summing Amplifier. The signal level applied to the VCO may be varied in output level as it passes through the FM Deviation Digital-to-Analog Convertor (DAC). This allows setting the FM deviation of the RF output signal.

Some of the circuitry on the A3 assembly forms part of the FM Calibration circuits. Refer to Service Sheet 11 for a general discussion of these circuits. More specific information is included in the following paragraphs.

FM Deviation Circuits

The Internal 400 or 1000 Hz modulation signal and the External modulation signal are switched to the negative input of FM Deviation Summing Amplifier A10U17A by FET switches A10Q7 and Q6. The FET switches are biased off or on by comparators U21C and D. The comparators are controlled by data bits from the Microprocessor input to the Modulation Control Latches (refer to Service Sheet 6). The FM drive signal output of the FM Deviation Summing Amplifier is the positive Reference input to the FM Deviation DAC A10U14. This audio frequency modulation signal is attenuated by the DAC to the level required to frequency modulate the output signal to the deviation selected at the front panel. The FM Deviation DAC resistance ladder is set by the Microprocessor bits stored by the Modulation Control Latches (refer to Service Sheet 6). The output from the DAC is amplified by the FM Deviation Amplifier A10U17B. Any dc or ac output of the amplifier is connected to the FM Reference Summing Amplifier U6D. The gain of amplifier U6D is either 10 or 1 as determined by the FET switch Q1. The amplifier has a gain of one for the FM deviation range 0 to 9.9 kHz and 10 for the range 10 to 99 kHz. The FET switch is biased on or off by comparator U8A. U8A is controlled by a data bit from the Microprocessor latched in LF Loop Shift Register U25A (refer to Service Sheet 9).

The output of the FM Reference Summing Amplifier U6D is applied to the FM Cal DAC U1 shown on Service Sheet 11. This signal is the FM signal for modulation or the FM signal for calibration of the Low Frequency Oscillator's FM sensitivity. The other output of the amplifier is coupled to FM Integrator U12D. U12D integrates the FM signal to provide a reference for comparing with the detected FM VCO signal during the FM Calibration Cycle. The LF Loop has a narrow bandwidth, therefore, the Low Frequency Loop VCO must be modulated within the loop bandwidth. The output of the integrator is sampled by unity gain FM Integrator Sample and Hold Buffer U8D and C73. The output of the buffer is summed with the output of the Phase-to-Charge Converter shown on Service Sheet 10. The two voltages are out of phase and cancel the In-band FM Correction Voltage to the VCO. During FM Calibration, this voltage is summed with the phase-to-charge voltage and the difference is made equal to 0 by setting SAR bits (refer to Service Sheet 11). The sampling is controlled by FET switch

SERVICE SHEET 12 (Cont'd)

U3A opened every 10 or 4 ms for 0.4 ms by the Tune Sample Monostable active-low output to comparator U0B.

The FM Integrator Bias Loop Fast and Slow response are to zero the dc offset to the FM Integrator. The bias circuit looks at the output of the FM Integrator U12D to adjust out the dc drift and therefore keeps the negative input and output at 0.0 Vdc, the same as the positive input. The bias loop takes the output of the integrator and feeds it back to the input of U6D. Although the input of the integrator is held at 0.0 Vdc, there can still be a dc current at the input and voltage at the output. This is accomplished in the slow response mode by limiting the bandwidth to less than 1.0 Hz. The output of the integrator U12D is applied to the negative input of amplifier U12A through filter R92, 93 and C72. FET switch U18A is biased on by comparator U16B in the slow response mode. The End-of-Conversion EOC(L) from the SAR (shown on Service Sheet 11) is high (approximately +5.0 Vdc) setting the output to approximately +15.0 Vdc which turns the FET switch on. FET switch U18D is biased on or off by Fast Response Control comparator U16A. In the fast response mode, the output of integrator U12D is not filtered but connected directly to the input of amplifier U12A. Under both fast and slow response U12A will try to keep the negative input, pin 2, at 0.0 Vdc, the same as the positive grounded input pin 3. This will keep the output of U12D at 0.0 Vdc, the same as the input to U12A. The circuit would do the same for the audio modulation signals except that the narrow loop bandwidth will not let the circuit respond fast enough.

The fast response state is entered when the instrument's frequency is changed. For any change in frequency, the dc voltage from the FM Deviation DAC will change which forces a change at the output of the integrator U12D. The need to remove this voltage quickly from the integrator results in the use of the wider bandwidth of the fast response mode.

The negative input of Fast Response Comparator U16A is normally fixed at approximately 0.6 Vdc by diode CR19. The end-of-conversion, EOC(L), from U10C SAR (Service Sheet 11) is low except during the FM calibration of the LF Loop. The Shift Data (H) output of Write Strobe Generator U21A (Service Sheet 9) is low except when serial data is being written to the LF Loop. The FM Integrator Bias Loop Control active-low output of SAR clock generator J-K Flip-Flop U5A (Service Sheet 11) is high except during the FM calibration of the LF loop. When data is written to the Low Frequency Loop, Shift Data (H) goes high and the negative input to comparator U16A is driven to approximately −4.0 Vdc. The output of the comparator changes to approximately +15.0 Vdc and FET switch U18D is closed. During this time both FET switches U18A and D are closed. 75 μs after the last data bit has been written to the LF Loop, the Shift Data (H) goes low. If the high slew rate mode has been activated, the low active-low output of High Slew Rate Monostable U21B sets the J-K Flip-Flop U5A's active-low output low (refer to Service Sheet 11). This output from U5A will remain low for approximately 1.85s until

SERVICE SHEET 1

the FM calibration c
inputs to U10A will b
data is written until t
EOC(L) goes high a
complete. The high-t
low output of J-K F
written to the LF Lo
and its output is hig
bles the fast respons
EOC(L) goes high f
U10A low. The Shift
low and the EOC(L) i
negative input of co
This keeps the fast
switch U18A is open
calibration time.

The FM Calibration
calibration of the LF
Slew Rate Monostab
mately 500 ms while t
low resets the J-K Fli
low output high. One
low. One input to gat
high so its output is l
Slew Rate Monostab
the Reset input. U5B
the FM Calibration c
are controlled by th
enable the output of
transition of the outp
Service Sheet 10. The
0.4 ms every 10 or 4 m
output of U5B is set
active-low output goi
K input is high. Ther
high and repeat the c
calibration. The com
each time U5B is tog
between the pulses o
and U4C is 180°. Th
amplifier U8C. The o
the FM Calibration

S	R
H	L
H	H
H	H
T Toggles to nex	

2 (Cont'd)

ycle is completed. For approximately 1.60 s both e low and the output high. This is from the time he FM calibration cycle begins. At this time the nd remains high until the FM Calibration is -low transition of the EOC(L) clocks the active- lip-Flop U5A high. Therefore, when data is p (during the time both inputs to U10A are low) FET switch U18D will be closed which ena- mode. When the FM calibration is started the r approximately 80 ms setting the output of Data (H) input to Exclusive-Or gate U13C is s now high. The high output of U13C drives the mparator U16A to approximately +15.0 Vdc. response loop open. The slow response FET when the EOC(H) input is low during the FM

Signal Generator is activated only during FM Loop. The High Slew Rate Sel (L) from the High e (refer to Service Sheet 11) is low for approxi- he instrument is in the high slew rate mode. The -Flop U5B active-high output low and the active- input to gate U4D will be high so the output is U4C will be low and the other from U14C will be w. J-K Flip-Flop U5B will not change until High e U21B's active-low output goes high releasing an not be gated until the EOC(L) goes high when ycle is started. The outputs of the J-K Flip-Flop output of U14C. The EOC(L) being high will J14C to be controlled by the 0.4 ms high-to-low ut of Tune Sample Monostable U15A shown on monostable's active-low output is pulsed low for s. On the high-to-low transition at the gate, the with the active-high output going high and the g low. Refer to Table 1. The J input is low and the fore, the Flip-Flop will toggle when the gate goes ycle on each of the 0.4 ms pulses during the FM mon inputs to U4C and U4D enable the gates gled (every 10 or 4 ms). The phase relationship tput from U5B to the remaining inputs to U4D e pulse outputs of U4C and U4D are input to tput of U8C will be +15V or −15V and is used for ycle.

Table 1. U5B Operation

G	J	K	Pin-9	Pin-7
X	X	X	L	H
↓	H	L	H	L
H	L	H	T	T

t state

SERVICE SHEET 12 (Cont'd)

TROUBLESHOOTING

Procedures for checking circuits of the A10 Audio Power Supply Assembly and the A3 Low Frequency Loop Assembly are given below. The areas or points to check are marked on the schematic by a hexagon with a checkmark and a number inside, e.g., ✓1 . Fixed voltages are shown on the schematic inside a hexagon, e.g. 2V±0.2V . Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter . . . . HP 3465A
Oscilloscope
  Storage Mainframe . . . . HP 181A
  Vertical Amplifier . . . . HP 1801A
  Time Base . . . . HP 1820C

✓1 FM Deviation Amplifier

1. Set the Signal Generator to 500 MHz, modulation source to 1 kHz Internal, FM mode and 50 kHz deviation.

2. Check A10J6-Pin 8 for a 1 kHz signal of approximately 3.0 Vp-p.

✓2 FM Range Select, FM Reference Summing Amplifier

1. Set the Signal Generator to 500 MHz, modulation source 1 kHz Internal, FM mode and 50 kHz deviation.

2. Check A3J2-Pin 13 for a 1 kHz signal at approximately 3.2 Vp-p.

3. Change the FM deviation to 5 kHz.

4. Check J2-Pin 13 for a 1 kHz signal approximately 0.32 Vp-p.

✓3 FM Integrator, FM Integrator Sample and Hold Control, FM Integrator Sample and Hold Buffer

1. Set the Signal Generator's frequency to 500 MHz, modulation source 1 kHz internal, FM mode and 50 kHz deviation.

2. Verify that the waveform shown in Figure 1 is correct.

NOTE

The FET Switch is opened for 0.4 ms every 10 ms. This stores the FM Integrator's output on capacitor C73.

3. The FM Integrator Sample and Hold Buffer's output, checked at J3-Pin 15, should be approximately 0.1 Vp-p. The cosine of the FM Integrator input is seen at J2-Pin 13. Externally trigger the oscilloscope at J2-Pin 13 to see the phase difference.

4. External trigger the oscilloscope on the FM Integrator Sample and Hold Control (J2-Pin 3) to lock the sample and hold pulse for 0.4 ms every 10 ms.

SERVICE SHEET 12 (Cont'd)

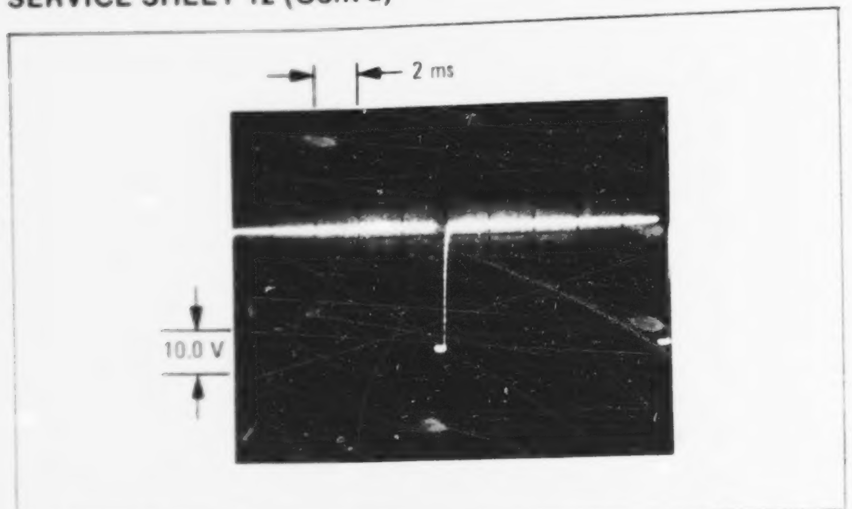


Figure 1. Oscilloscope Display of FM Integrator Sample and Hold Control (dc coupled to J2-Pin 3; internally triggered)

✓4 FM Calibration, FM Integrator Sample and Hold Buffer

1. Set the Signal Generator to 500 MHz in the CW mode.

2. Increment the frequency up 10 MHz. Figures 2, 3 and 4 show the correct signals for FM Calibration of the LF Loop's VCO.

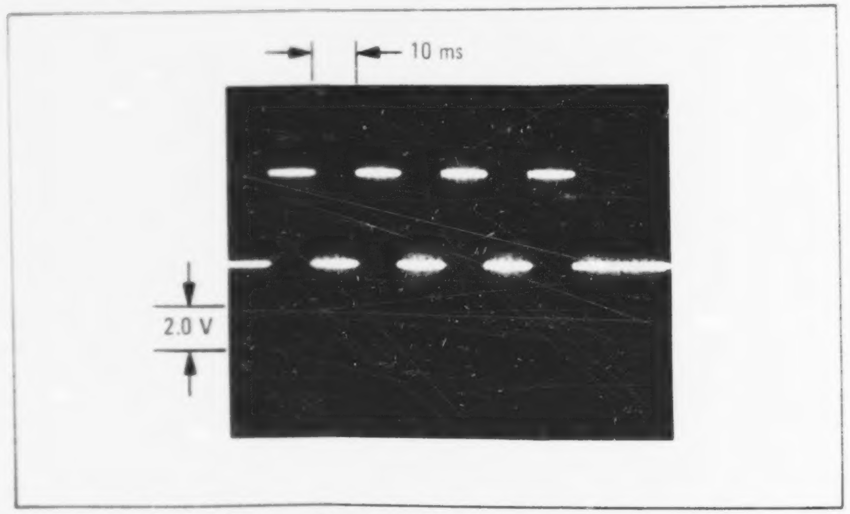


Figure 2. Oscilloscope Display of SAR Data Control Generated during FM Calibration (dc coupling to U5-Pin 7; external triggering from U5-Pin 13)

Low Frequency Loop
Frequency Modulation
Calibrator, P/O A3
SERVICE SHEET 11

SERVICE SHEET 12 (Cont'd)

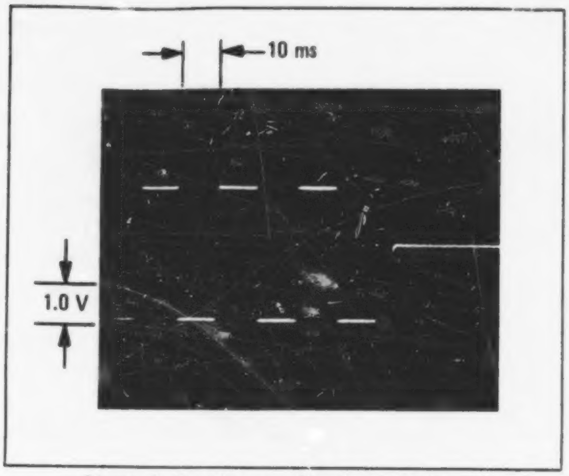


Figure 3. Oscilloscope Display at J2-Pin 13 during FM Calibration (dc coupling to J2-Pin 13; external triggering is from U5-Pin 7)

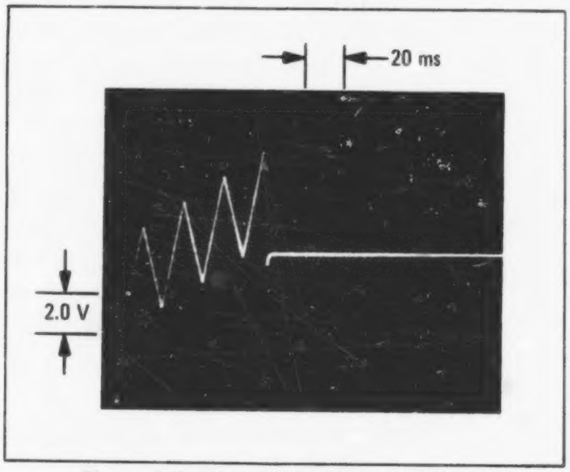


Figure 4. Oscilloscope Display of J3-Pin 15 during FM Calibration (dc coupling to J3-Pin 15; external triggering from U5-Pin 7)

$\sqrt{5}$ FM Integrator Bias Loop

1. Set the Signal Generator to 500 MHz without modulation.

2. Check the output at U16B-Pin 2, the Slow Response Control comparator. It should be approximately +15 Vdc. FET switch U18A is closed.

3. Check the output of the Fast Response Control comparator U16A-Pin 1. It should be approximately– 15 volts dc. FET switch U18D is open.

4. Increment the frequency up 10 MHz and check that U16B-Pin 2 goes to -15 Vdc during FM calibration approximately 80 ms. Check that U16A-Pin 1 goes to approximately +15 Vdc approximately 50 ms after FM calibration is terminated. Externally trigger the oscilloscope at U5-Pin 7. 50 ms is the time it takes to change the voltage at U16A from -4 to +0.6 Vdc.

P/O A10 ASSEMBLY

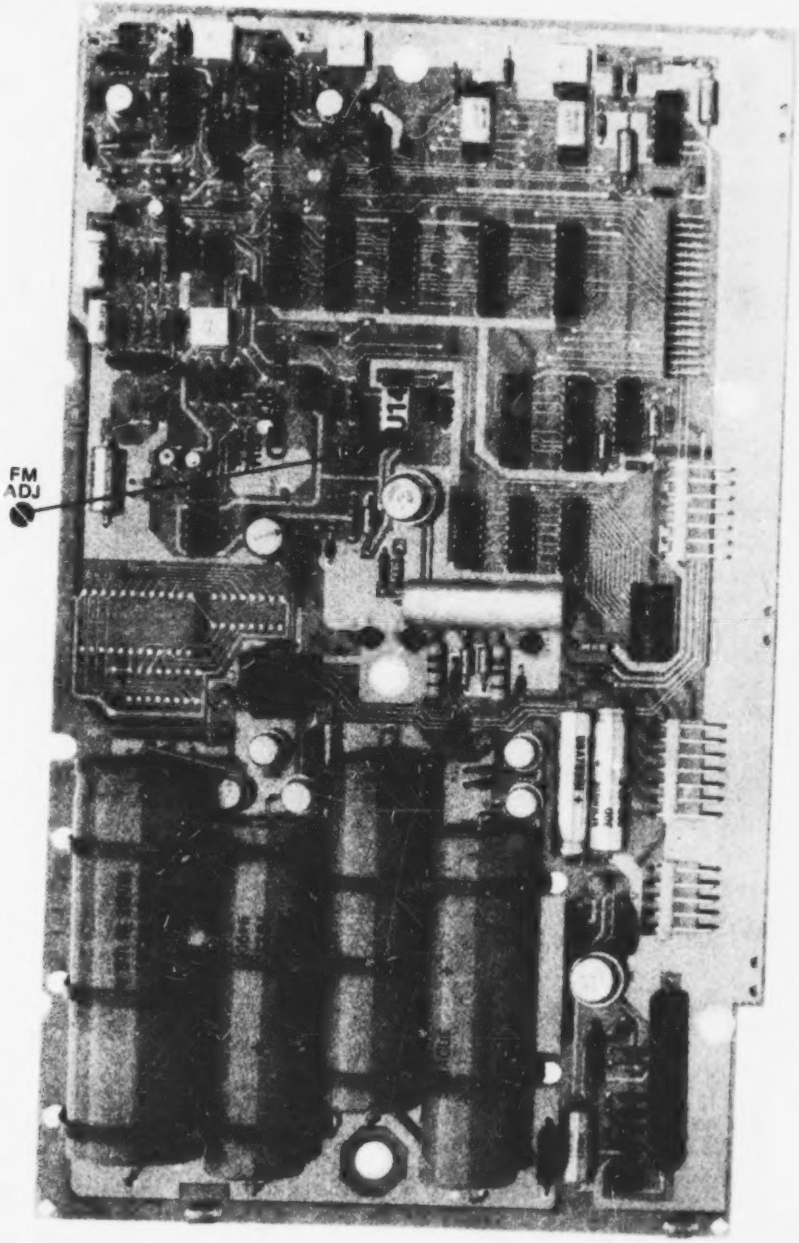


Figure 8-76. LF Loop FM System Control Component Locations

P/O A3 ASSEMBLY

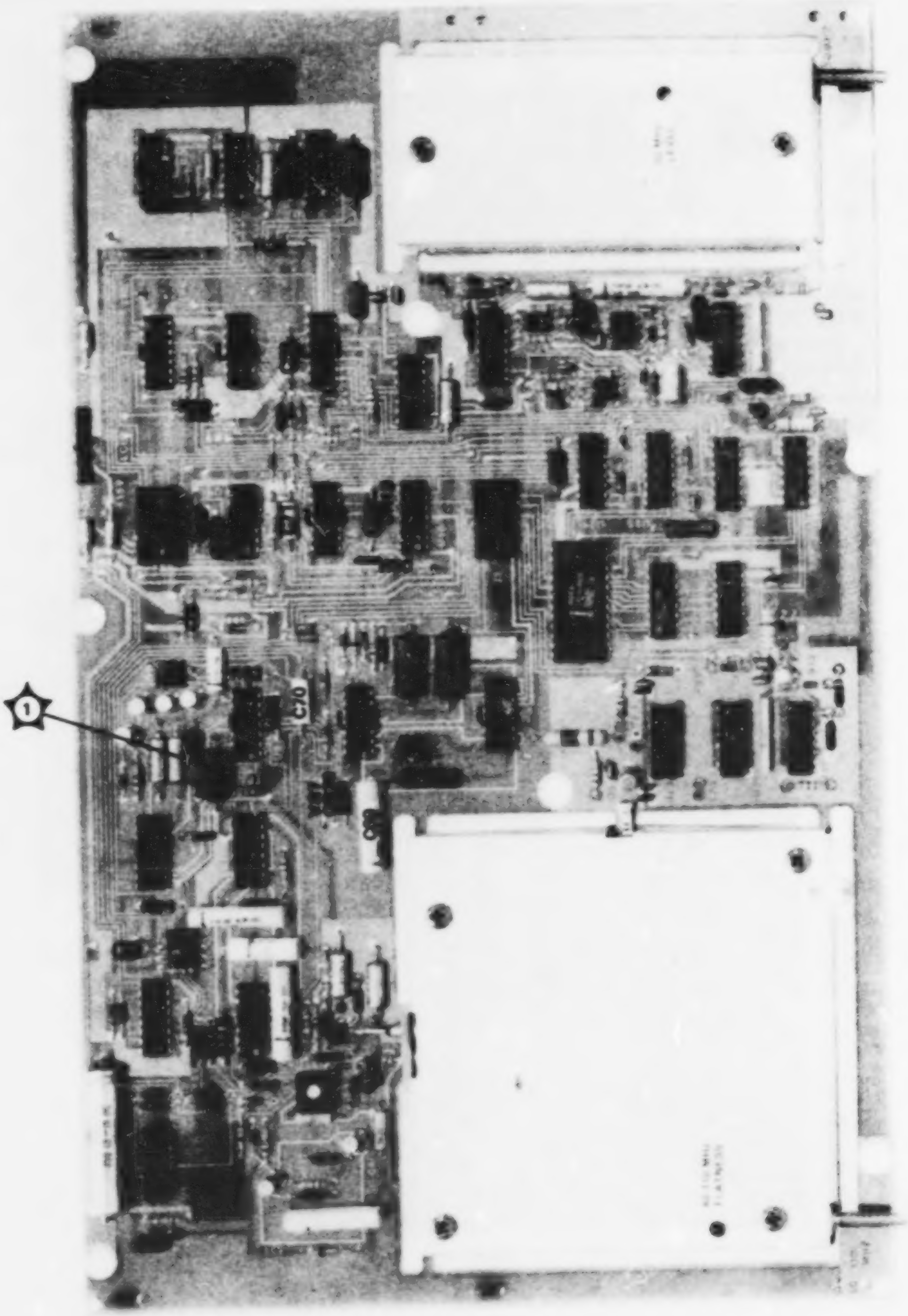


Figure 8-77. LF Loop FM System and Calibrator Component Locations

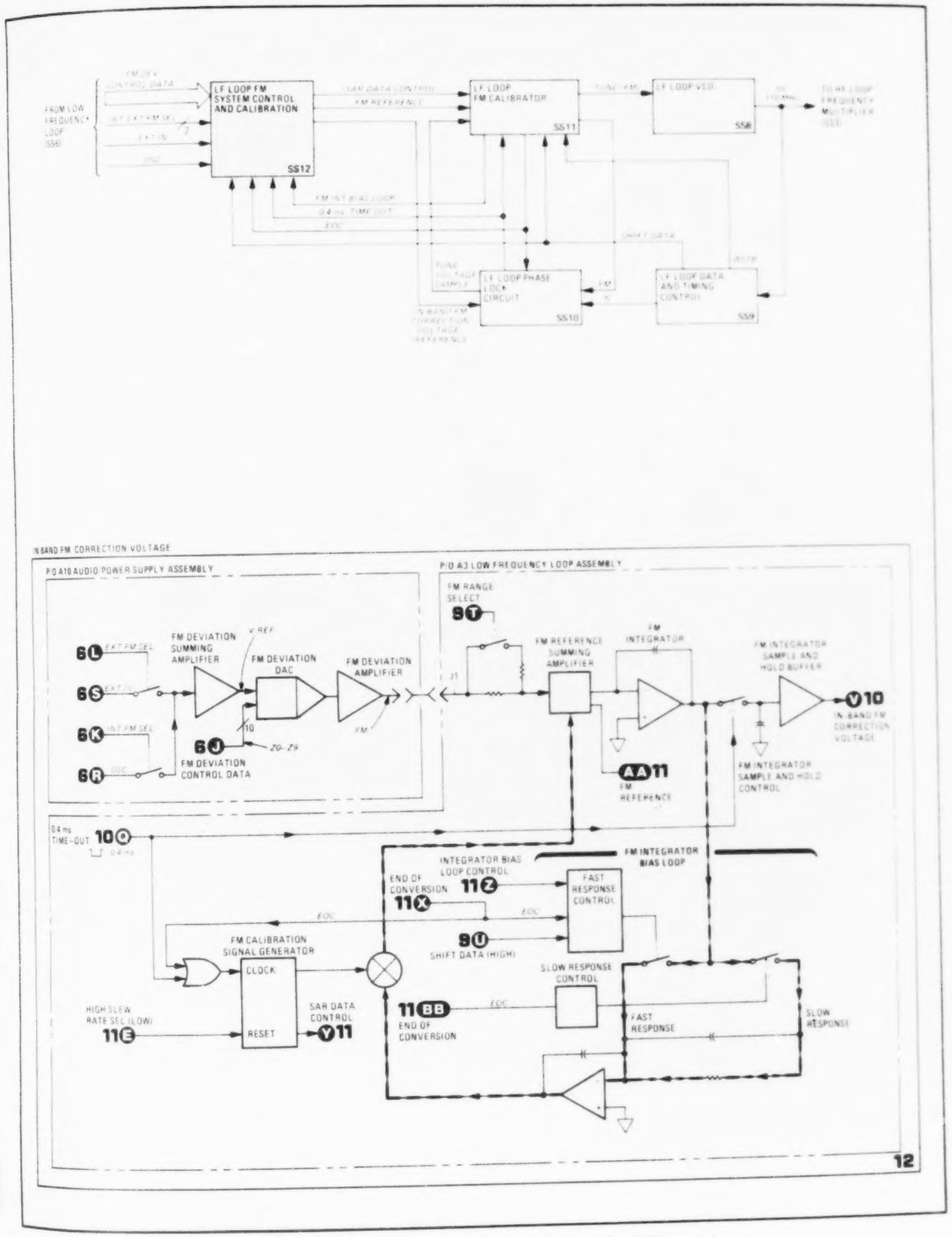
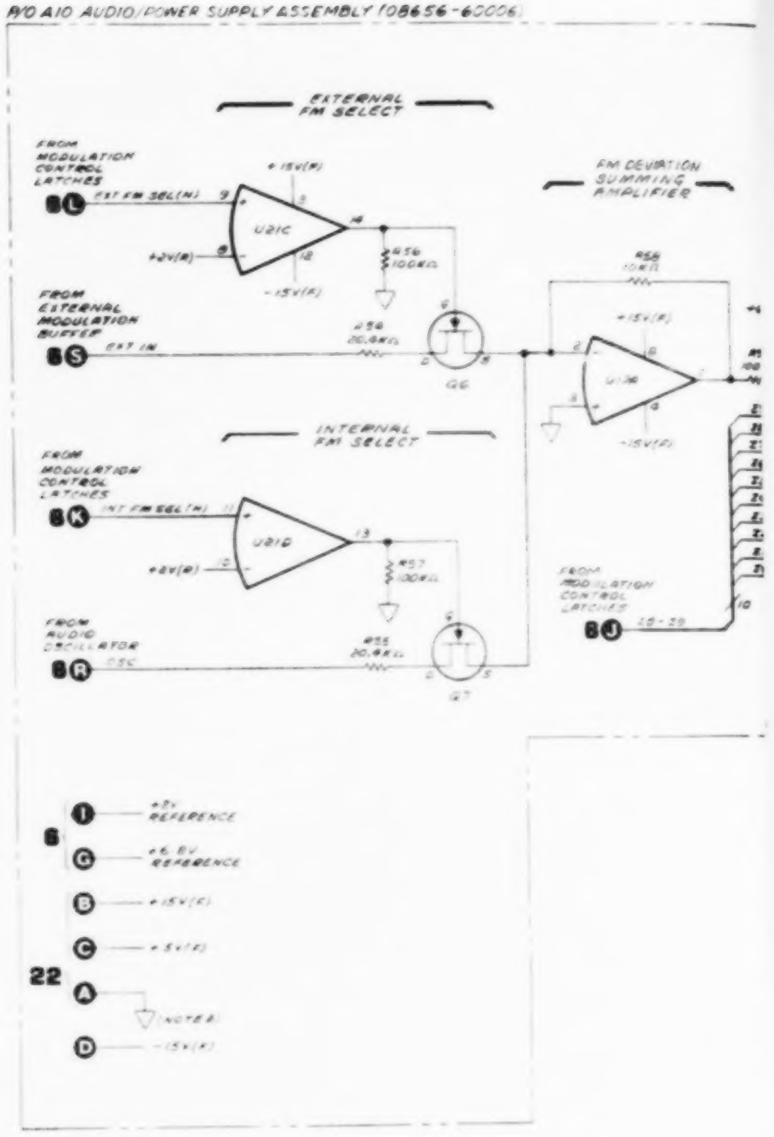
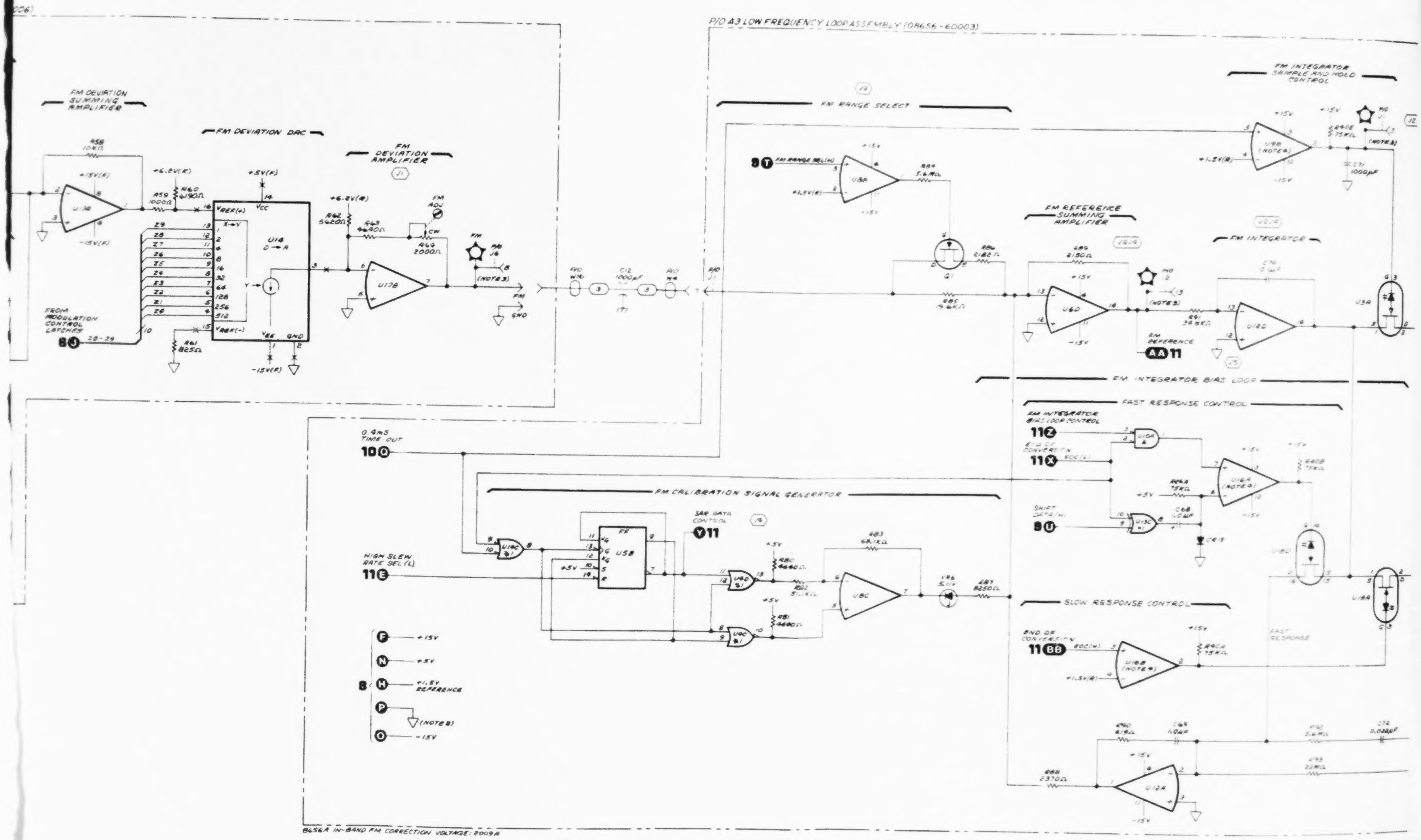
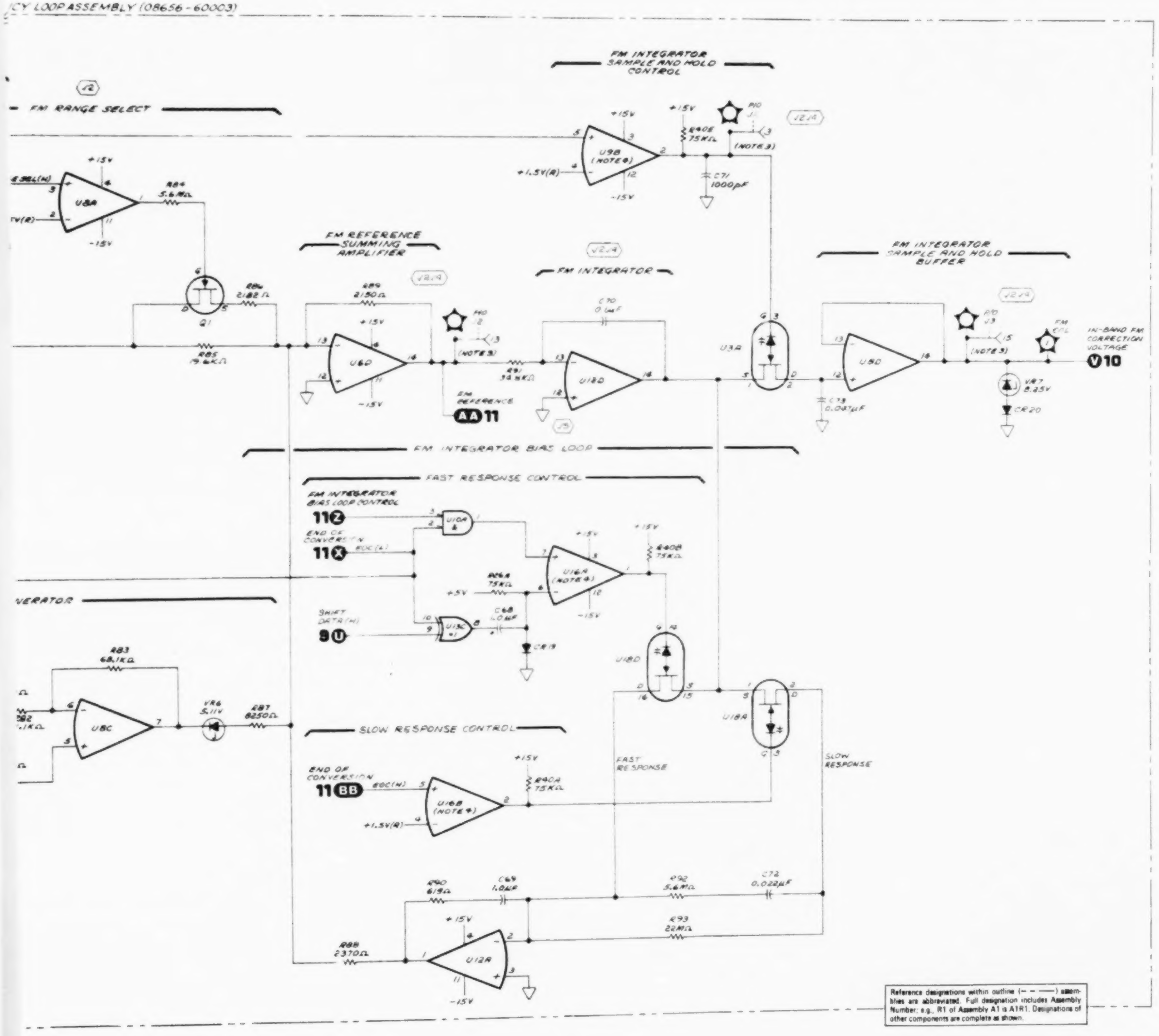

FROM LOW FREQUENCY LOOP (SS8)
FM DEV CONTROL DATA
INT EXT FM SEL
EXT IN
OSC
LF LOOP FM SYSTEM CONTROL AND CALIBRATION
SS12
SAR DATA CONTROL
FM REFERENCE
LF LOOP FM CALIBRATOR
SS11
TUNE (FM)
LF LOOP VCO
SS8
TO HF LOOP FREQUENCY MULTIPLIER (SS3)
FM INT BIAS LOOP
0.4 ms TIME OUT
EOC
SHIFT DATA
TUNE VOLTAGE SAMPLE
LF LOOP PHASE LOCK CIRCUIT
SS10
IN BAND FM CORRECTION VOLTAGE REFERENCE
FM
LF LOOP DATA AND TIMING CONTROL
SS9
IN BAND FM CORRECTION VOLTAGE
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY
P/O A3 LOW FREQUENCY LOOP ASSEMBLY
6L EXT FM SEL
6S EXT IN
6K INT FM SEL
6R OSC
FM DEVIATION SUMMING AMPLIFIER
V REF
FM DEVIATION DAC
FM DEVIATION AMPLIFIER
6J
FM DEVIATION CONTROL DATA
Z0–Z9
10
FM
J1
FM RANGE SELECT
9T
FM REFERENCE SUMMING AMPLIFIER
FM INTEGRATOR
FM INTEGRATOR SAMPLE AND HOLD BUFFER
V10
IN-BAND FM CORRECTION VOLTAGE
AA11
FM REFERENCE
FM INTEGRATOR SAMPLE AND HOLD CONTROL
0.4 ms TIME-OUT 10Q
0.4 ms
INTEGRATOR BIAS LOOP CONTROL
11Z
END OF CONVERSION
11X
FM INTEGRATOR BIAS LOOP
FAST RESPONSE CONTROL
EOC
9U
SHIFT DATA (HIGH)
FM CALIBRATION SIGNAL GENERATOR
CLOCK
RESET
HIGH SLEW RATE SEL (LOW)
11E
SAR DATA CONTROL
Y11
11BB
END OF CONVERSION
SLOW RESPONSE CONTROL
FAST RESPONSE
SLOW RESPONSE
12

Figure 8-78. LF Loop FM System Control and Calibrator Block Diagrams


P/O A10 AUDIO/POWER SUPPLY ASSEMBLY (08656-60006)
EXTERNAL FM SELECT
FROM MODULATION CONTROL LATCHES
6L
EXT FM SEL(H)
+15V(F)
U21C
+2V(R)
−15V(F)
R56 100KΩ
FROM EXTERNAL MODULATION BUFFER
6S
EXT IN
R54 20.4KΩ
Q6
FM DEVIATION SUMMING AMPLIFIER
R58 10KΩ
U17B
INTERNAL FM SELECT
FROM MODULATION CONTROL LATCHES
6K
INT FM SEL(H)
U21D
R57 100KΩ
FROM AUDIO OSCILLATOR
6R
OSC
R55 20.4KΩ
Q7
FROM MODULATION CONTROL LATCHES
6J
Z0 - Z9
10
6
+2V REFERENCE
+6.8V REFERENCE
+15V(F)
+5V(F)
22
(NOTE 8)
−15V(F)


P/O A3 LOW FREQUENCY LOOP ASSEMBLY (08656-60003)
FM DEVIATION SUMMING AMPLIFIER
FM DEVIATION DAC
FM DEVIATION AMPLIFIER
FM RANGE SELECT
FM INTEGRATOR SAMPLE AND HOLD CONTROL
FM REFERENCE SUMMING AMPLIFIER
FM INTEGRATOR
FM INTEGRATOR BIAS LOOP
FAST RESPONSE CONTROL
SLOW RESPONSE CONTROL
FM CALIBRATION SIGNAL GENERATOR
FROM MODULATION CONTROL LATCHES
0.4mS TIME OUT
HIGH SLEW RATE SEL (L)
SAR DATA CONTROL
FM INTEGRATOR BIAS LOOP CONTROL
END OF CONVERSION
SHIFT DATA (H)
FM REFERENCE
FM RANGE SEL (H)
U12A
U14 D→A
U17B
U8A
U6D
U12D
U9B
U3A
U10A
U16A
U13C
U16B
U8B
U12A
U5B
U4C
U4D
U8C
Q1
VR6 5.11V
R58 10kΩ
R59 1000Ω
R60 6190Ω
R61 825Ω
R62 5620Ω
R63 4640Ω
R64 2000Ω
R84 5.6kΩ
R85 19.6kΩ
R86 2182Ω
R89 2150Ω
R91 34.8kΩ
R80 4640Ω
R81 4640Ω
R82 51.1kΩ
R83 68.1kΩ
R87 8250Ω
R88 2370Ω
R90 619Ω
R92 5.6MΩ
R93 22MΩ
R40A 75kΩ
R40B 75kΩ
R40E 75kΩ
R26A 75kΩ
C12 1000pF
C68 1.0µF
C69 1.0µF
C70 0.1µF
C71 1000pF
C72 0.022µF
CR19
FM ADJ
FM
GND
(NOTE 3)
(NOTE 4)
8J
8T
9U
10D
11E
11Z
11X
11BB
AA11
Y11
8 F +15V
N +5V
H +1.5V REFERENCE
P (NOTE 8)
O −15V
8656A IN-BAND FM CORRECTION VOLTAGE: 2009A


CY LOOP ASSEMBLY (08656-60003)
J2
FM RANGE SELECT
+15V
SEL(H)
3
2
V(R)
U8A
4
11
1
-15V
R84
5.6MΩ
G
D
S
Q1
R86
2182Ω
R85
19.6KΩ
FM REFERENCE SUMMING AMPLIFIER
J2J4
R89
2150Ω
+15V
13
12
U6D
14
-15V
P10
J2
13
(NOTE 3)
FM REFERENCE
AA 11
FM INTEGRATOR SAMPLE AND HOLD CONTROL
+15V
5
4
+1.5V(R)
U9B
(NOTE 4)
3
12
2
-15V
+15V
R40E
75KΩ
P10
J1
3
(NOTE 3)
J2J4
C71
1000pF
J2J4
FM INTEGRATOR
C70
0.1µF
R91
34.8KΩ
13
12
U18D
14
J3
U3A
G
3
5
1
D
2
FM INTEGRATOR SAMPLE AND HOLD BUFFER
J2J4
13
12
U8D
14
C73
0.047µF
P10
J3
15
(NOTE 3)
FM CAL
IN-BAND FM CORRECTION VOLTAGE
V 10
VR7
8.25V
CR20
FM INTEGRATOR BIAS LOOP
FAST RESPONSE CONTROL
FM INTEGRATOR BIAS LOOP CONTROL
11 Z
END OF CONVERSION
11 X
EOC(L)
3
2
U10A
&
1
+15V
7
6
U16A
(NOTE 4)
3
12
-15V
+15V
R40B
75KΩ
R26A
75KΩ
+5V
SHIFT DATA(H)
9 U
10
9
U13C
=1
8
C68
1.0µF
CR19
U18D
G
14
D
16
S
15
1
2
S
D
U18A
G
3
FAST RESPONSE
SLOW RESPONSE
ERATOR
R83
68.1KΩ
R82
1KΩ
6
5
U8C
7
VR6
5.11V
R87
8250Ω
SLOW RESPONSE CONTROL
END OF CONVERSION
11 BB
EOC(H)
5
4
+1.5V(R)
U16B
(NOTE 4)
2
+15V
R40A
75KΩ
R90
619Ω
C69
1.0µF
R92
5.6MΩ
C72
0.022µF
R93
22MΩ
+15V
4
R88
2370Ω
1
U12A
2
3
11
-15V

Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A3J1-4 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKET J2 OR J3.
4. OPEN COLLECTOR DEVICE.

REFERENCE DESIGNATIONS

NO PREFIX	A10
C12 W4,16	J6 Q6,7 R54-64 U14,17,21
A3	
C68-73 CR19,20 J1-3 Q1 R26,40, 80-93 TP1 U3-6,8-10, 12-14,16,18 VR6,7	

LOGIC LEVELS

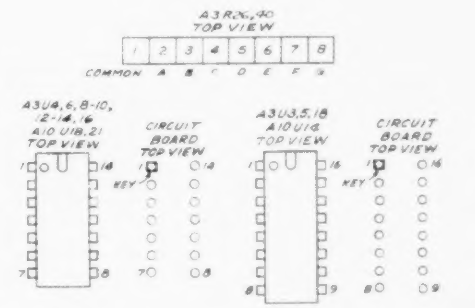
	TTL
HIGH	> 2V
LOW	< 0.8V
< IS MORE NEG THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
A3	
Q1	1855-0280
U3,18	1858-0066
U4	1820-1272
U5	1820-1212
U6,8,12	1826-0522
U9,16	1826-0174
U10	1820-1144
U13	1820-1211
U14	1826-0462
A10	
Q6,7	1855-0020
U14	1826-0462
U17	1826-0521
U21	1826-0138

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
A3	
U4,10,13,14	+5V – 14 ▽ – 7
U5	+5V – 16 ▽ – 8


A3R26,40
TOP VIEW
1
2
3
4
5
6
7
8
COMMON
A
B
C
D
E
F
G
A3U4,6,8-10,
12-14,16
A10 U18,21
TOP VIEW
1
14
7
8
CIRCUIT BOARD TOP VIEW
KEY
A3U3,5,18
A10U14
TOP VIEW
16
9
CIRCUIT BOARD TOP VIEW

12

P/O A3, P/O A10

Figure 8-79. LF Loop FM System Control and Calibrator Schematic Diagram

SERVICE SHEET 13
P/O A3 Low Frequency Loop Assembly
P/O A16 10 MHz Reference Oscillator

TROUBLESHOOTING HELP

Service Sheet BD3
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

50 MHz Reference Oscillator

The 50 MHz Reference Oscillator, Q9, is a common base crystal controlled oscillator. The amount of positive feedback is predetermined by the taps on the inductors. The inductors are spiral printed circuit board traces.

The base of Q9 is biased by resistor R111 at approximately 0 Vdc. The emitter is biased by resistors R112 and 113. Resistor R113 is connected to the −15 Vdc supply which biases on diodes CR30 and 31. This closes the dc current path for the emitter current of Q9 and also closes the tank circuit. The tank circuit consists of the crystal Y1, varactor diode CR33, the printed circuit board inductors and C86 and C89. The output frequency can be adjusted by the TB Adj R110 which controls the voltage across the varactor diode thereby changing the capacitance of the tank circuit. This tune voltage is applied through resistors R109, 115 and RF chokes L21 and 22. The output level is peaked by the 50 MHz Level Adj capacitor C86. Capacitors 83, 84, 90, 91, 92 and 97 are bypass capacitors.

Time Base Divider

The output of the Reference Oscillator is ac coupled by C93 to the Frequency Multiplier Assembly shown on Service Sheet 3. The output is also ac coupled by capacitor C77 to common base Time Base Buffer Q12. The output of Q12 clocks the Divide-by-5 circuit U32A. Note that the set and reset inputs are all tied low. The output, 10 MHz at pin 4, is taken from bit 2. This provides two outputs for every ten clock pulse inputs.

The output of U32A clocks the Divide-by-ten circuit U29B. This divider is made up of a divide-by-2 and a divide-by-5 circuit. Like U32, the set and reset inputs are tied to ground. The outputs are 5 MHz at pin 15 and 1 MHz at pin 4.

One of the three divided output frequencies, 10, 5, or 1 MHz may be selected to phase lock the reference oscillator to an internal (Option 001) or external time base. The resistor jumper is shipped in the 10 MHz position and must be moved to the 5 or 1 MHz position depending on the frequency of the external time base. The Time Base Output follows the frequency selected by the jumper.

SERVICE SHEET 13 (Cont'd)

The time base output is applied to pin 11 of Exclusive-or gate U19. Its other input is tied to +5 Vdc. The output from pin 14 is the input phase shifted 180 degrees. The signal is then detected by diode CR34 and ac coupled to the Time Base Output J4.

Crystal Phase Lock Circuit

The Time Base Input signal is ac coupled by C95 to resistor R94 and the positive and negative peak limiting diodes of CR21 and 22. The input is then ac coupled by capacitor C74 to pin 7 of Exclusive-Or gate U19. The input goes to ac ground by resistors R95 and 96 and capacitor C75. The output of the gate is connected to the input to bias on the ECL gate. The output is also connected through the resistor R98 to resistor R99D and diode CR23. CR23 detects the Time Base Input signal and applies the voltage to the positive input of comparator U22B. The positive input is increased so it is more positive than the negative input and the output of U22B switches to +15 Vdc, detecting the presence of a Time Base Input. When the output of U22B switches to +15 Vdc the phase lock operational amplifier U22A is activated by turning off diode CR25 and turning on diode CR29. The inputs of comparator U22B are connected to U19-Pin 3 the Exclusive-Or gate output. Diode CR24 temperature compensates CR23.

The Time Base Input signal from U19-Pin 3 is connected to U19-Pin 4. The other input, pin 5, is the divided output of the 50 MHz Reference Oscillator. The signal is divided to 10, 5 or 1 MHz depending on the Time Base Input frequency and the subsequent jumper placement. This Exclusive-or gate serves as a phase detector with its change in output voltage being proportional to the phase difference of the two inputs. The output is coupled to the 50 MHz Reference Oscillator which serves to phase lock the oscillator to the Time Base Input signal. The correction voltage to U22A is amplified and applied to the oscillator tank circuit through diode CR28. CR28 is turned on when comparator U22B turns CR25 off and the negative input of U22B changes to approximately +3 Vdc. The positive input is fixed and the output goes from +15 Vdc to approximately −7 Vdc. CR28 is turned on as are diodes CR26 and 27 when the phase difference is large enough. Resistor R106 is bypassed which moves the reference oscillator to the correct frequency.

TROUBLESHOOTING

Procedures for checking the circuits shown on Service Sheet 13 are given below. The area or points to check are marked on the schematic by a hexagon with a check mark and a number inside, e.g. ⟨✓3⟩. Fixed voltages are shown on the schematic inside a hexagon, e.g. ⟨2V±0.2V⟩. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Miltimeter	HP 3465A
Oscilloscope	HP 1222A

SERVICE SHEET 13 (Cont'd)

⟨✓1⟩ Crystal Phase Lock Circuit

Measure the voltage shown in Table 1. With an oscillator connected to the Time Base Input o reference oscillator installed, the 50 MHz oscilla locked.

Table 1. Crystal Phase Lock Circuit Vol

Operating Mode		Voltages Idc and ac					
		U19-Pin				U22B-Pi	
		7	5	2	3	5	6
Phase Locked	Vdc	+3.8	+3.8	+3.8	+4.0	+4.0	+0.7
	Vpk	0.4	0.4	0.4	0.4	0.01	0.01
Not Phase Locked	Vdc	+3.8	+3.8	+3.8	+3.8	+1.5	+4.7
	Vpk	0.02	0.4	0.2	0.05	0.01	0.01

⟨✓2⟩ 50 MHz Reference Oscillator

1. Verify that Q9's bias voltages are correct.
2. Measure the oscillator output at TP7.

⟨✓3⟩ Divided Time Base Signals

1. Measure the signals at J3-Pin 8 and J4.
2. Verify that the waveform shown in Figure

E SHEET 13 (Cont'd)

ystal Phase Lock Circuit

the voltage shown in Table 1. With an external reference : connected to the Time Base Input or with the internal oscillator installed, the 50 MHz oscillator should be phase

Table 1. Crystal Phase Lock Circuit Voltages

ting de		Voltages (dc and ac) on									
		U19-Pin				U22B-Pin			U22A-Pin		
		7	5	2	3	5	6	7	3	2	1
	Vdc	+3.8	+3.8	+3.8	+4.0	+4.0	+3.7	+13	+4	+4	-10
	Vpk	0.4	0.4	0.4	0.4	0.01	0.01	0.01	0.08	0	0.02
	Vdc	+3.8	+3.8	+3.8	+3.8	+3.5	+3.7	-13	+4	+3	+14
	Vpk	0.02	0.4	0.2	0.05	0.01	0.01	0.005	0.02	0	0.008

MHz Reference Oscillator

; that Q9's bias voltages are correct.

ure the oscillator output at TP7.

vided Time Base Signals

ure the signals at J3-Pin 8 and J4.

; that the waveform shown in Figure 1 is correct.

SERVICE SHEET 13 (Cont'd)

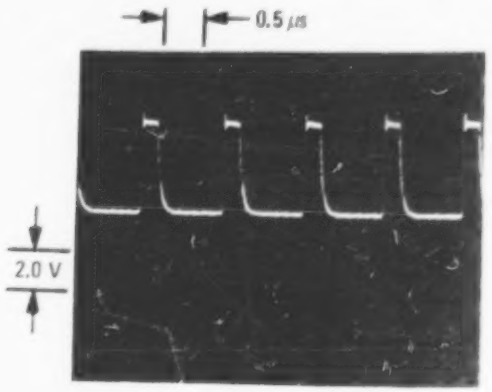


Figure 1. Display of 1 MHz Reference Signal (dc coupling to J3-Pin 5; internal triggering)

NOTE

A residual FM problem at the RF output may be due to residual FM from the 50 MHz Reference Oscillator. Measuring residual FM of the Reference Oscillator using the test setup found in Section IV may be inconclusive. The residual FM of the measuring instrument (HP 8901A Modulation Analyzer) is normally greater than that of a Reference Oscillator that is operating properly. Therefore the measurement would be meaningless.

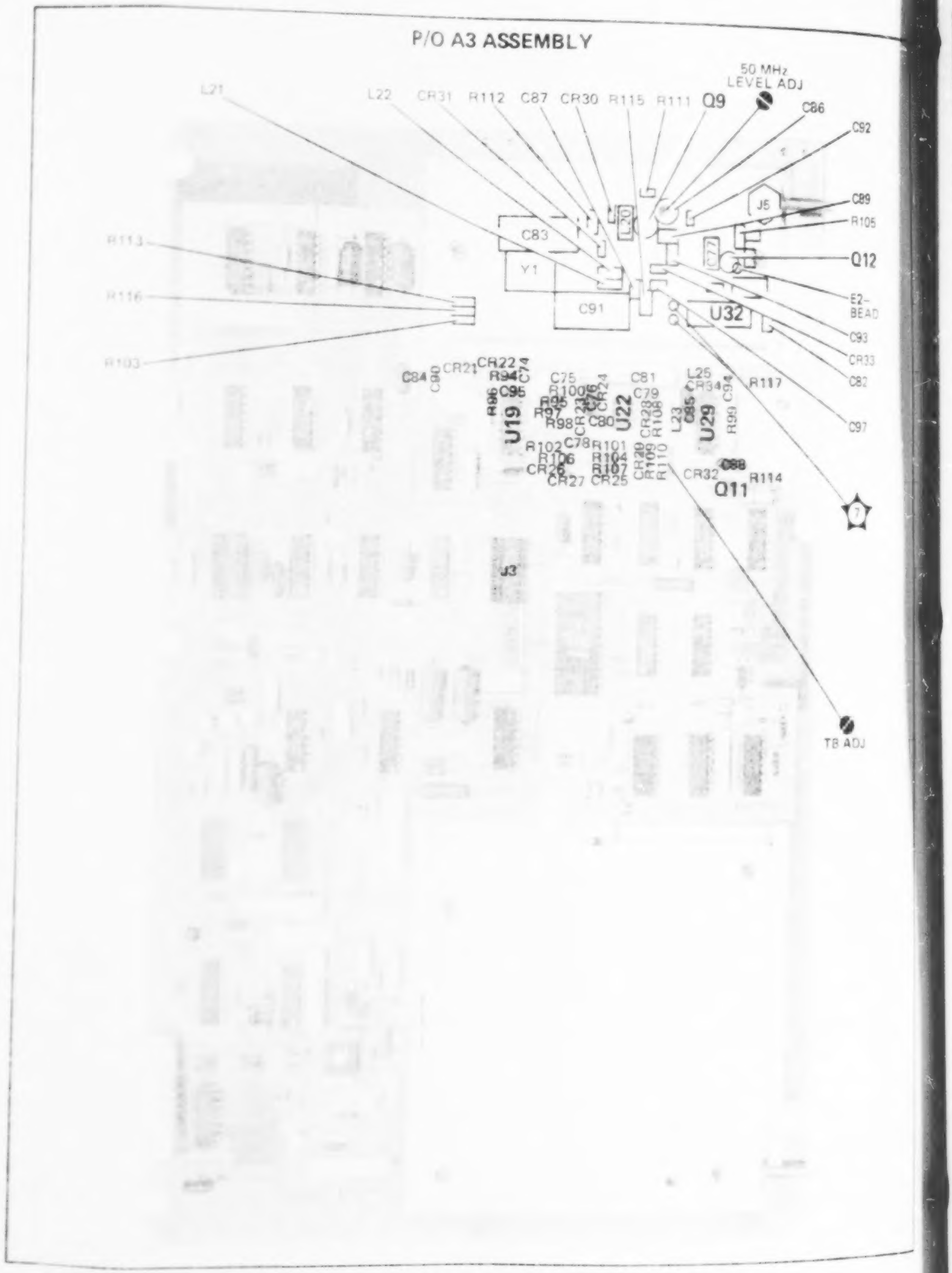
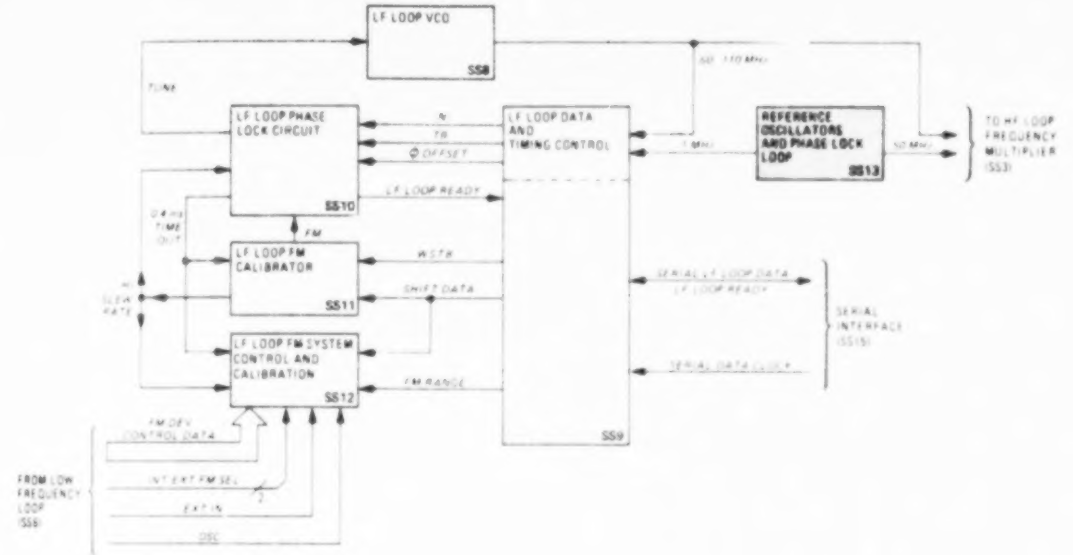

P/O A3 ASSEMBLY
L21
L22
CR31
R112
C87
CR30
R115
R111
Q9
50 MHz LEVEL ADJ
C86
C92
C89
R105
Q12
E2-BEAD
C93
CR33
C82
C97
R113
R116
R103
C83
Y1
C91
U32
J5
C84
C90
CR21
CR22
R94
C74
R96
C95
U19
C75
R100
R95
R97
R98
C76
CR23
CR24
C80
U22
C81
C79
CR28
R108
L25
CR34
L23
C85
U29
C94
R99
R117
R102
C78
R106
CR26
CR27
R101
R104
R107
CR25
CR29
R109
R110
CR32
C88
Q11
R114
7
J3
TB ADJ

Figure 8-80. Reference Oscillator and Phase Lock Loop Component Locations


LF LOOP VCO
SS8
TUNE
50 – 110 MHz
LF LOOP PHASE LOCK CIRCUIT
SS10
N
TB
Φ OFFSET
LF LOOP READY
LF LOOP DATA AND TIMING CONTROL
SS9
1 MHz
REFERENCE OSCILLATORS AND PHASE LOCK LOOP
SS13
50 MHz
TO HF LOOP FREQUENCY MULTIPLIER (SS3)
0.4 ms TIME OUT
FM
LF LOOP FM CALIBRATOR
SS11
WSTB
SHIFT DATA
HI SLEW RATE
LF LOOP FM SYSTEM CONTROL AND CALIBRATION
SS12
FM RANGE
SERIAL LF LOOP DATA
LF LOOP READY
SERIAL INTERFACE (SS15)
SERIAL DATA CLOCK
FM DEV CONTROL DATA
FROM LOW FREQUENCY LOOP (SS6)
INT EXT FM SEL
2
EXT IN
OSC

50 MHz REFERENCE OSCILLATOR AND TIME BASE DIVIDER

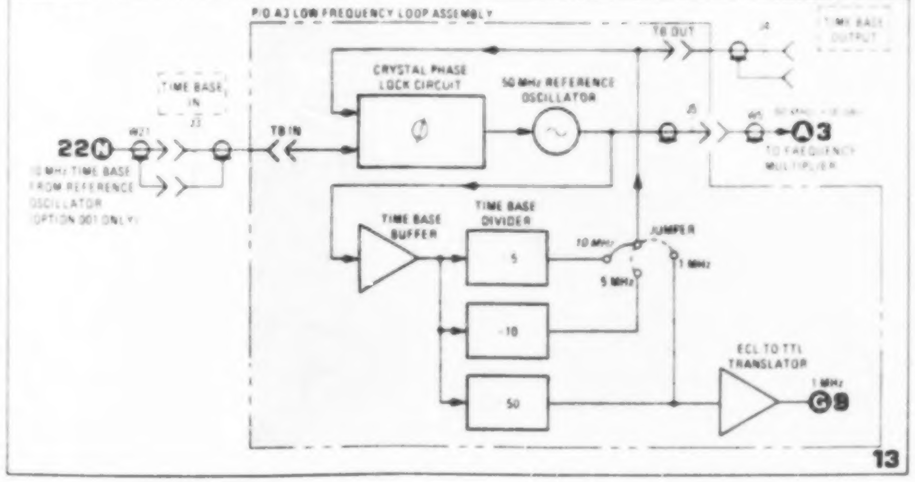
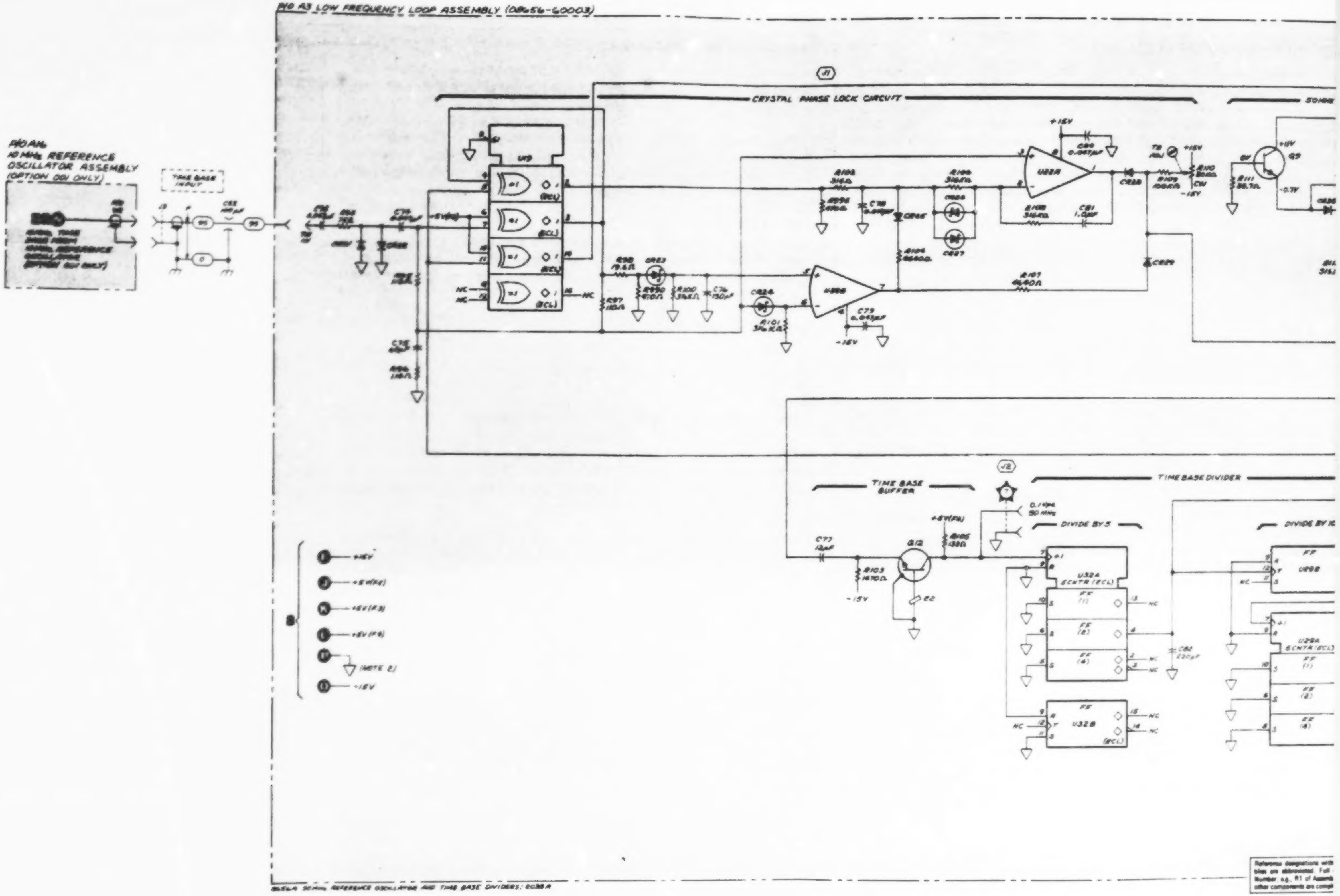
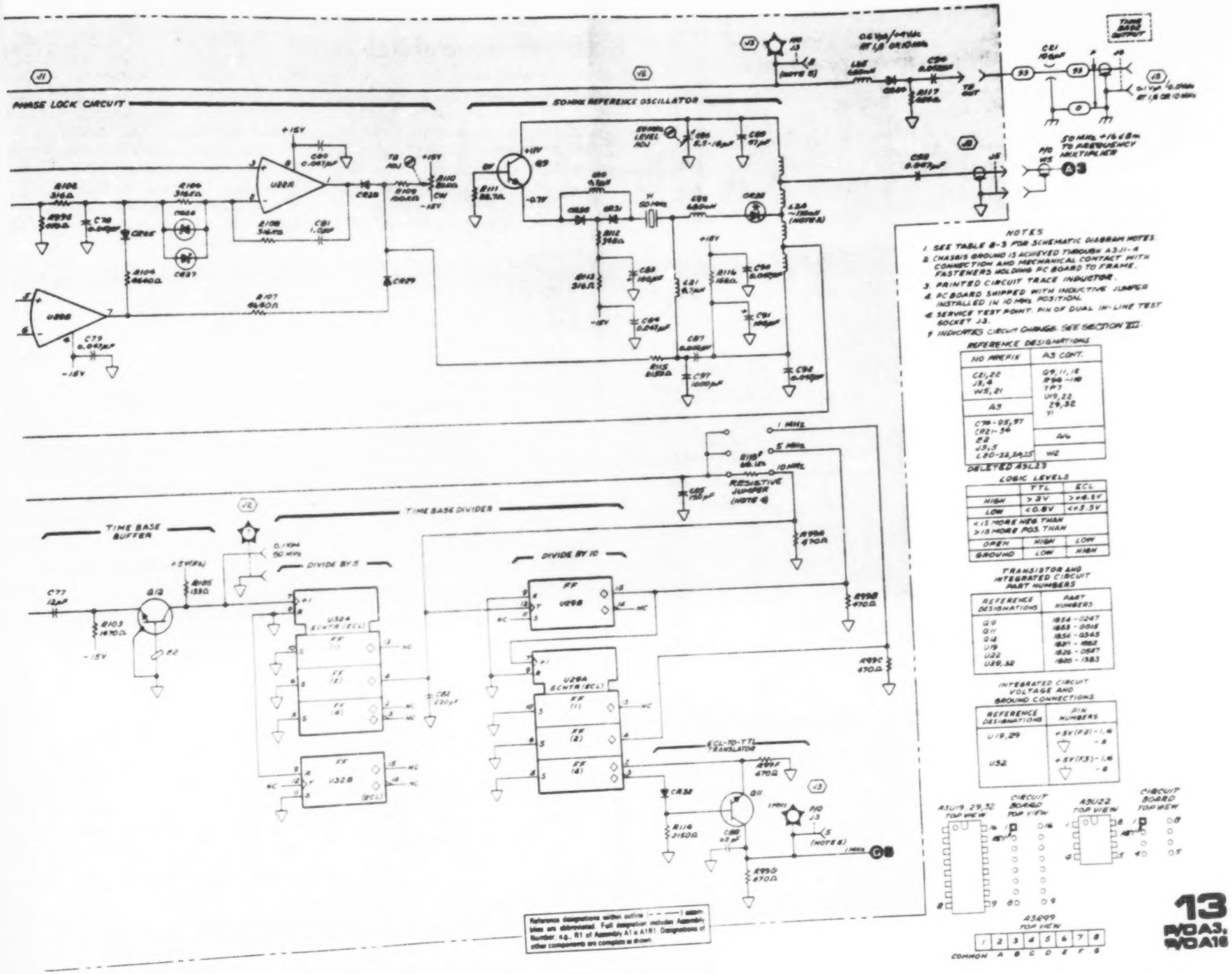

P/O A3 LOW FREQUENCY LOOP ASSEMBLY
TB OUT
J4
TIME BASE OUTPUT
CRYSTAL PHASE LOCK CIRCUIT
Φ
50 MHz REFERENCE OSCILLATOR
TIME BASE IN
J3
W21
22 N
10 MHz TIME BASE FROM REFERENCE OSCILLATOR (OPTION 001 ONLY)
TB IN
J5
W5
A3
TO FREQUENCY MULTIPLIER
TIME BASE BUFFER
TIME BASE DIVIDER
5
10
50
10 MHz
5 MHz
1 MHz
JUMPER
ECL TO TTL TRANSLATOR
1 MHz
C 9
13

Figure 8-81. Reference Oscillator and Phase Lock Loop Block Diagrams


A10 A3 LOW FREQUENCY LOOP ASSEMBLY (08656-60003)
A10 A16
10 MHz REFERENCE
OSCILLATOR ASSEMBLY
(OPTION 001 ONLY)
(OPTION 001 ONLY)
TIME BASE INPUT
J3
C55
CRYSTAL PHASE LOCK CIRCUIT
U19
(ECL)
NC
R97 110Ω
R98 19.6Ω
CR23
R99D 1100Ω
R100 316KΩ
C76 150pF
CR24
R101 316KΩ
U22B
C79 0.047µF
-15V
+15V
C80 0.047µF
U22A
R102 316Ω
R99E
C78
CR25
R106 316KΩ
CR26
CR27
R104 6640Ω
R108 316KΩ
C81 1.0µF
R107 6640Ω
CR28
TP ADJ
R109 100KΩ
R110
CW
CR29
R111 38.7Ω
Q9
-0.7V
C96
R96 110Ω
TIME BASE BUFFER
C77 12pF
R103 1470Ω
-15V
Q12
+5V(F4)
R105 133Ω
E2
0.1V
50 MHz
TIME BASE DIVIDER
DIVIDE BY 5
U32A
5CNTR (ECL)
FF (1)
FF (2)
FF (4)
FF
U32B
(ECL)
C82 220pF
DIVIDE BY 10
FF
U29B
U29A
5CNTR (ECL)
FF (1)
FF (2)
FF (4)
NC
+15V
+5V(F2)
+5V(F3)
+5V(F4)
(NOTE 2)
-15V
8656A 50 MHz REFERENCE OSCILLATOR AND TIME BASE DIVIDERS: 2038A
Reference designations with
bles are abbreviated. Full
Number, e.g., R1 of Assemb
other components are compl


PHASE LOCK CIRCUIT
50 MHz REFERENCE OSCILLATOR
TIME BASE BUFFER
TIME BASE DIVIDER
DIVIDE BY 5
DIVIDE BY 10
ECL-TO-TTL TRANSLATOR
U22A
U22B
R102 316Ω
R99E 619Ω
C78 0.047µF
CR25
R106 316kΩ
CR26
CR27
R104 4640Ω
R107 4640Ω
C79 0.047µF
R108 316kΩ
C81 1.0µF
C80 0.047µF
+15V
-15V
TB ADJ
R110
CW
R109 100kΩ
CR28
CR29
Q9
R111
+11V
-0.7V
CR30
CR31
R112
R113 316Ω
C83
C84
L21
R116
C90
C91
C87
R115
C97 1000pF
C92
Y1 50 MHz
CR32
50 MHz LEVEL ADJ
C86
C89
L24 (NOTE 3)
TB OUT
R117
C88 0.047µF
CR1
TIME BASE OUTPUT
50 MHz +16 dBm TO FREQUENCY MULTIPLIER
P/O W5
A3
J5
1 MHz
5 MHz
10 MHz
R118
RESISTIVE JUMPER (NOTE 4)
C85
R99A 470Ω
R99B 470Ω
R99C 470Ω
R99D 470Ω
R99F 470Ω
R99G 470Ω
C77 12pF
Q12
R103 1470Ω
R105 133Ω
+5V(F2)
0.1Vpk 50 MHz
U32A 5CNTR (ECL)
U32B
U29A 5CNTR (ECL)
U29B
FF
C82 220pF
NC
Q11
R114 2150Ω
C88
P/O J3
(NOTE 5)
1 MHz
A3U19, 29, 32 TOP VIEW
CIRCUIT BOARD TOP VIEW
A3U22 TOP VIEW
KEY
A3J99 TOP VIEW
COMMON A B C D E F G
13
P/O A3,
P/O A16

Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number, e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A3J1-4 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. PRINTED CIRCUIT TRACE INDUCTOR.
4. PC BOARD SHIPPED WITH INDUCTIVE JUMPER INSTALLED IN 10 MHz POSITION.
5. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKET J3.

† INDICATES CIRCUIT CHANGE. SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A3 CONT.
CR1,22 J3,4 W5,21	Q9,11,12 R96-118 TP7 U19,22 29,32 Y1
A3	A16
C78-95,97 CR21-34 E2 J3,5 L20-22,24,25	W2

DELETED A3L23

LOGIC LEVELS

	TTL	ECL
HIGH	>2V	>+4.1V
LOW	<0.8V	<+3.3V
< IS MORE NEG THAN > IS MORE POS. THAN		
OPEN	HIGH	LOW
GROUND	LOW	HIGH

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q9	1854-0247
Q11	1853-0016
Q12	1854-0345
U19	1820-1052
U22	1826-0587
U29,32	1820-1383

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U19,29	+5V(F2)-1,16 ▽ -8
U32	+5V(F3)-1,16 ▽ -8

Figure 8-82. Reference Oscillators and Phase Lock Loop Schematic Diagram

SERVICE SHEET 14
P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

Microprocessor

Instrument functions are controlled by the Microprocessor U13 as it executes the program instructions stored in ROM (read only memory). The function of the Microprocessor's data bus, address bus, and each of its input/output lines is discussed in the following paragraphs.

Data Bus. The data bus (D0 through D7) consists of eight bidirectional lines which are used to transfer an 8-bit positive-true data byte to and from the Microprocessor (pins 26 through 33). The 3-state lines can be high, low, or at the high impedance state depending on the individual data bit or its buffering conditions. The Microprocessor reads data from memory, the keyboard, its HP-IB interface, and so forth under program control via the data bus. Data is written onto the data bus for the displays, RF and modulation circuitry, and so forth. Information on the data bus is buffered as it enters or leaves the Microprocessor. For additional information, refer to the discussion on Data Bus Buffering.

Read/Write Control. The Read/Write signal from the Microprocessor (R/W at pin 34) is used to control the direction of data transfer on the data bus. When the Microprocessor is halted or available to accept data, this signal will be high indicating that the Microprocessor is in the "read" state. When data is being transferred out onto the data bus, this signal will be low indicating that the Microprocessor is in the "write" state. This signal is buffered by one of the Microprocessor Control Line Buffers U16 to control the direction of data transfer through the Data Bus Buffers U14, to or from RAM (Read/Write) memory (refer to Service Sheet 16), and to or from the HP-IB Interface Buffers U15 (refer to Service Sheet 17).

Address Bus. The address bus (A0 through A15) consists of sixteen unidirectional lines which are used to transfer a 16-bit positive-true address from the Microprocessor (pins 9 through 20 and 22 through 25). Information on the address bus is buffered as it leaves the Microprocessor. These buffered address bits are decoded to produce level and modulation, attenuator, and serial I/O control strobes (refer to Service Sheet 15). In addition, these buffered address bits are decoded to select one of 256 external RAM memory locations, one of 12,288 ROM memory locations (refer to Service Sheet 16), or one of the HP-IB General Purpose Interface Adapter U19 ports (refer to Service Sheet 17).

Valid Memory Address. The Valid Memory Address signal from the Microprocessor (VMA at pin 5) is used to indicate that a valid address is on the address bus. When VMA is active (high), the information on the address bus will be valid. This signal is buffered by one of the Microprocessor Control Line Buffers U16 to enable decoding of those addresses that produce the level and modulation, attenuator, and serial I/O control strobes (refer to Service Sheet 15). In addition, this buffered signal enables the decoding and selection of ROM and RAM memory locations (refer to Service Sheet 16).

SERVICE SHEET 14 (Cont'd)

System Clock. An external 4 MHz crystal Y1 is directly connected to the Microprocessor (pins 38 and 39). An internal divide-by-4 circuit is used to develop the 1 MHz system clock E (pin 37). Capacitors C16 and C22 are used to keep the clock frequency stable. This clock signal is buffered by one of the Microprocessor Control Line Buffers U16 to enable the decoding of those addresses that produce the level and modulation, attenuator, and serial I/O control strobes (refer to Service Sheet 15). In addition, this buffered clock signal enables the decoding and selection of ROM and RAM memory locations (refer to Service Sheet 16) and clocks the HP-IB General Purpose Interface Adapter U19 (refer to Service Sheet 17).

Memory Ready. The Memory Ready signal input to the Microprocessor (MR at pin 3) is tied high to enable the 1 MHz system clock rate.

RAM Enable. The RAM Enable signal input to the Microprocessor (RE at pin 36) is directly tied to the +5V supply to power the 128 bytes of internal RAM. These bytes are addressed at hexidecimal memory locations 0000 through 007F.

Standby. The Standby signal input to the Microprocessor (STBY at pin 35) is directly tied to the +5V supply to separately power the first 32 bytes of internal RAM. These bytes are addressed at hexidecimal memory locations 0000 through 001F.

Halt. The Halt signal input to the Microprocessor (HALT at pin 2) is used to halt program execution. When HALT is active (low), the Microprocessor will finish executing its current instruction, the address bus will remain fixed at the address of the next instruction, and all 3-state lines will go to their high impedance state (including the data bus). Program execution will continue when HALT goes inactive (high). For additional information on how this line is controlled, refer to the discussion on Restart Circuitry.

Reset. The Reset signal input to the Microprocessor (RESET at pin 40) is used to start the Microprocessor from a power-down condition. This condition exists during initial start-up of the instrument, after a power failure has occurred and when the front panel switch has been momentarily set to RESET. When RESET is active (low), the Microprocessor becomes inactive. When RESET is inactive (high), the internal program counter will be loaded with the contents of hexidecimal memory locations FFFE and FFFF. These contents direct program execution to the power-up subroutine. For additional information on how this line is controlled, refer to the discussion on Restart Circuitry.

Non-Maskable Interrupt. The Non-Maskable Interrupt signal input to the Microprocessor (NMI at pin 6) is one of two signals used to interrupt program execution. When NMI is active (low), the Microprocessor will finish executing its current instruction, save its current status, and then its internal program counter will be loaded with the contents of hexidecimal memory locations FFFC and FFFD. These contents direct program execution to the non-maskable interrupt subroutine. For this Signal Generator, the non-maskable interrupt

SERVICE SHEET 14 (Cont'd)

is used for the signature analyzer's signature analysis subrouti For additional information on how this line is controlled, refer to discussion on Interrupt Processing.

Maskable Interrupt Request. The Maskable Interrupt Request sig input to the Microprocessor (IRQ at pin 4) is the other signal use interrupt program execution. When IRQ is active (low) and interrupt mask bit of the internal condition code register is not the Microprocessor will finish executing its current instruct Then its internal program counter will be loaded with the conte of hexidecimal memory locations FFF8 and FFF9. These conte direct program execution to the maskable interrupt subroutine. additional information on how this line is controlled, refer to discussion on Interrupt Processing.

Data Bus Buffering

Data is transferred positive-true to and from the Microprocessor the bidirectional, 8-bit data bus. Information on the data bus buffered as it leaves or enters the Microprocessor. The 3-state, bi rectional Data Bus Buffers U14 provides this asynchronous, t way communication between the data bus and the Microprocess During normal operation, rocker switch S1D is set to NRM. W S1D in this position, the enable input of U14 (pin 19) will be pull low through the open-collector inverter U21A. The enable input the 3-state buffer U31B is also pulled low through U21A (refer to discussion on Interrupt Processing).

The direction of data transfer through U14 is controlled by the st of the buffered read/write line from the Microprocessor. When direction input of U14 (pin 1) is high, information will be transfer from the data bus to the Microprocessor (a "read" operation). Wh this input is low, information will be transferred from the Microp cessor to the data bus (a "write" operation).

Sixteen bits of serial keyboard data are transferred from the stora registers on the Display Assembly - A2 to the Microprocessor via 0 of the data bus (refer to Service Sheet 18). During program exe tion of the keyboard read subroutine, the Keyboard Serial Data Buffer U31D will be enabled to couple the serial keyboard data to bit 0 input of U14. Buffer enabling occurs when the Microproces issues and decodes hexidecimal address 01FA (refer to Service Sh 15).

One of the service features of this instrument is the hard-wired N (no operation) instruction. This 8-bit instruction is used to step Microprocessor through its ROM addresses during ROM testing troubleshooting. When the Microprocessor receives a NOP inst tion, its program counter will be advanced once for each clock c without affecting any other operations. The eight inputs to 3-state buffer U18 are hard-wired in a configuration to provide NOP instruction to the Microprocessor, that is, bit D0 is tied h and bits D1 through D7 are tied low (00000001). During nor operation, rocker switch S1D is set to NRM. With S1D in this

nnected to
ply-4 circuit
citors C16
This clock
ne Buffers
e the level
es (refer to
nables the
ns (refer to
Interface

croproces-
clock rate.

processor
128 bytes
l memory

(STBY at
r the first
xidecimal

t pin 2) is
low), the
tion, the
struction,
ncluding
ALT goes
ne is con-

ET at pin
ondition.
ent, after
itch has
low), the
e (high),
ntents of
contents
dditional
ssion on

al input
used to
Microp-
s current
with the
). These
nterrupt
nterrupt

is used for the signature analyzer's signature analysis subroutine. For additional information on how this line is controlled, refer to the discussion on Interrupt Processing.

Maskable Interrupt Request. The Maskable Interrupt Request signal input to the Microprocessor (IRQ at pin 4) is the other signal used to interrupt program execution. When IRQ is active (low) and the interrupt mask bit of the internal condition code register is not set, the Microprocessor will finish executing its current instruction. Then its internal program counter will be loaded with the contents of hexidecimal memory locations FFF8 and FFF9. These contents direct program execution to the maskable interrupt subroutine. For additional information on how this line is controlled, refer to the discussion on Interrupt Processing.

Data Bus Buffering

Data is transferred positive-true to and from the Microprocessor on the bidirectional, 8-bit data bus. Information on the data bus is buffered as it leaves or enters the Microprocessor. The 3-state, bidirectional Data Bus Buffers U14 provides this asynchronous, two-way communication between the data bus and the Microprocessor. During normal operation, rocker switch S1D is set to NRM. With S1D in this position, the enable input of U14 (pin 19) will be pulled low through the open-collector inverter U21A. The enable input of the 3-state buffer U31B is also pulled low through U21A (refer to the discussion on Interrupt Processing).

The direction of data transfer through U14 is controlled by the state of the buffered read/write line from the Microprocessor. When the direction input of U14 (pin 1) is high, information will be transferred from the data bus to the Microprocessor (a "read" operation). When this input is low, information will be transferred from the Microprocessor to the data bus (a "write" operation).

Sixteen bits of serial keyboard data are transferred from the storage registers on the Display Assembly - A2 to the Microprocessor via bit 0 of the data bus (refer to Service Sheet 18). During program execution of the keyboard read subroutine, the Keyboard Serial Data Bus Buffer U31D will be enabled to couple the serial keyboard data to the bit 0 input of U14. Buffer enabling occurs when the Microprocessor issues and decodes hexidecimal address 01FA (refer to Service Sheet 15).

One of the service features of this instrument is the hard-wired NOP (no operation) instruction. This 8-bit instruction is used to step the Microprocessor through its ROM addresses during ROM testing or troubleshooting. When the Microprocessor receives a NOP instruction, its program counter will be advanced once for each clock cycle without affecting any other operations. The eight inputs to the 3-state buffer U18 are hard-wired in a configuration to provide the NOP instruction to the Microprocessor, that is, bit D0 is tied high and bits D1 through D7 are tied low (00000001). During normal operation, rocker switch S1D is set to NRM. With S1D in this posi-

tion, the two enable inputs of U18 (pins 1 and 19) will be pulled high to disable its outputs. During ROM testing, S1D is set to ROM to enable the outputs of U18 which places the hard-wired NOP instructions on the data bus. U14 is disabled during this time because its enable input (pin 19) is pulled high through resistor R9D and the input to U21A is pulled low. Disabling U14 inhibits the NOP instruction from being transferred to any circuitry but the Microprocessor.

Restart Circuitry

Three methods are employed to reset or halt the Microprocessor. They occur:

1. During power-up initialization.

2. During manual operation via the front panel RESET/STBY/ON switch A1S49.

3. During service via rocker switch S1A.

During normal operation, rocker switch S1A is set to RUN. With S1A in this position, the RC network of R4 and C5 will begin to charge as soon as Mains power is applied and the +5V supply comes up. Zener diode VR1 will begin to conduct as soon as the charge across C5 reaches +4.22V. When VR1 conducts, transistor Q1 will be biased on to pull the input to the monostable U28 (pin 1) low. Resistors R6 and R7 set the bias conditions for Q1. With U28 pin 1 low, the output at pin 6 will go low for 30 ms to reset the Microprocessor. Capacitor C10 is used to set the pulse timing for U28. When the Microprocessor is reset, it will enter its power-up subroutine to initialize the instrument. The Schottky diode CR1 across R4 causes the RC network to quickly discharge in the event of a power supply transient. Once the power supply has recovered, another reset will be issued to initialize the instrument. Similarly, if the +5V supply voltage drops below +4.22V, Q1 will be biased off to halt the Microprocessor through the open-collector inverter U21E.

The Microprocessor can also be manually halted and reset by the front panel RESET/STBY/ON switch A1S49 (refer to Service Sheet 18). When A1S49 is momentarily set to RESET, the base of Q1 will be forced low. This will bias Q1 off to halt the Microprocessor through U21E. When A1S49 is released, Q1 is again biased on to initiate another 30 ms Microprocessor restart operation.

In much the same manner, rocker switch S1A can be manually set to cause the Microprocessor to halt. When S1A is set to the HLT/RST position, Q1 will be biased off to halt the Microprocessor through U21E. When S1A is set to RUN, Q1 will be biased on to initiate another 30 ms Microprocessor reset operation.

Interrupt Processing

As previously mentioned, there are two methods employed to interrupt normal program execution, namely maskable, and non-maskable interrupts. When either type of interrupt is detected, the

Microprocessor will finish executing its current instruction before program execution is directed to the respective interrupt subroutine.

Maskable interrupts occur whenever a key on the keyboard is pressed, a reverse power condition is detected, or an active low switch closure is applied through the rear panel sequence connector J5. Whenever one of these conditions is detected and latched the Interrupt Request signal input to the Microprocessor (IRQ at pin 4) will be forced active (low). The Microprocessor will then issue and decode hexidecimal address 01FC so that it can examine the contents of the Status (Service Request) Register U10 via the data bus to determine which one of the three maskable interrupts has occurred. U10 is hard-wired (pin 11 tied high) to function as a 3-state buffer. During program execution of the maskable interrupt subroutine, the Microprocessor first checks for a reverse power interrupt (D7 active low), then a sequence interrupt (D1 and D2 active low), and finally a keyboard interrupt (D2 active low). The methods used to detect and latch the three maskable interrupts are discussed in the following paragraphs.

Keyboard Interrupt. Whenever one of the keys on the Keyboard Assembly - A1 is pressed, a keyboard interrupt (KIN) is detected by the circuitry on the Display Assembly - A2 and issued to the Microprocessor/Memory/HP-IB Assembly - A11 (refer to Service Sheet 18). This active low interrupt is applied to connector J5 at pin 14. It is gated through U25D and U25B to direct-set flip-flop U29A causing the output at pin 6 to go low. This Flip-Flop debounces the leading edge of KIN and latches the occurrence of the keyboard interrupt. The latched keyboard interrupt is gated through U25C and the enabled, 3-state buffer U31B to generate an interrupt request (IRQ). U31B is enabled at pin 4 through the open-collector driver U21A as long as rocker switch S1D is set for normal (NRM) operation.

When the key is released, KIN will be high and U25D pin 12 will be pulled high by resistor R1. After an approximate 33 ms delay produced by the RC network of R2 and C2, capacitor C2 will charge to pull U25D pin 13 high. This delay debounces the trailing edge of KIN. Once the keyboard interrupt is processed, the Microprocessor will issue and decode hexidecimal address 01FB to clock U29A clear. Clearing U29A clears the keyboard interrupt.

Reverse Power Interrupt. A reverse power interrupt (RPI) occurs when a reverse power condition is detected and latched by the reverse power sense circuitry on the Output Assembly - A6 (refer to Service Sheet 7). This active low interrupt is applied through the LC filter of L7 and C7 on the RFI Assembly - A7 and the feedthrough capacitor C16 to connector A11J5 pin 10. Normally with no interrupt present, U25C pin 10 is pulled high through resistor R8. When a reverse power interrupt occurs, it is gated through U25C and the enabled tri-state buffer U31B to generate an interrupt request

SERVICE SHEET 14 (Cont'd)

(IRQ). U31B is enabled at pin 4 through the open-collector driver U21B as long as rocker switch S1D is set for normal (NRM) operation.

Sequence Interrupt. A sequence interrupt (SQI) occurs when an active low switch closure is applied through the rear panel connector J5 and feedthrough capacitor A14C8 to connector A11J5 pin 3. This interrupt is handled in much the same manner as the keyboard interrupt. Normally with no interrupt present, U25B pin 4 will be pulled high through resistor R5. A 33 ms delay is produced by the RC network of R3 and C4 to debounce the leading edge of SQI. When a sequence interrupt occurs, it is gated through U25B pin 4 to direct-set flip-flop U29A causing the output at pin 6 to go low. This flip-flop latches the occurrence of the sequence interrupt. The latched sequence interrupt is gated through U25C and the enabled, 3-state buffer U31B to generate an interrupt request (IRQ). U31B is enabled at pin 4 through the open-collector driver U21B as long as rocker switch S1D is set for normal (NRM) operation.

When the switch closure is removed, U25B pin 4 will be pulled high as soon as capacitor C4 charges. The delay produced by the RC network of R5 and C4 debounces the trailing edge of SQI. Once the sequence interrupt is processed, the Microprocessor, will issue and decode hexidecimal address 01FB to clock U29A clear. Clearing U29A clears the sequence interrupt.

The Non-Maskable Interrupt signal (NMI) input to the Microprocessor (pin 6) is normally pulled high through resistor R10. During signature analysis troubleshooting, this edge-triggered line is momentarily grounded to abort normal program execution and to direct program execution to the non-maskable interrupt subroutine.

In addition to buffering the three maskable interrupts, the Status (Service Request) Register U10 also buffers five status lines which monitor various instrument conditions. These conditions include the setting of the front panel RESET/STBY/ON switch (refer to Service Sheet 18), the state of the LF Loop Ready (LFR) line (refer to Service Sheet 10) the state of the HI and LO lines from the Over and Under Modulation Comparators (refer to Service Sheet 6), and the state of the HP-IB Interrupt Request (IBI) line (refer to Service Sheet 17). During normal program execution, the Microprocessor issues and decodes hexidecimal address 01FC to strobe the contents of U10 onto the data bus. If one of these five conditions is active when the Microprocessor strobes U10, it will execute the necessary instructions to service that condition.

+5V Supply Filtering

Capacitors C1, C3, C6 through C9, C11 through C15, and C17 through C19 are used to filter the +5V supply to the Microprocessor/Memory/HP-IB - A11 circuitry.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

Troubleshooting is done on the circuits of Service Sheet 14 when a defect seems to be related to the Microprocessor. The only troubleshooting information provided is signature analysis. If nothing definite is discovered in performing these checks, refer to Service Sheet 16 (ROM and RAM test) or consider the other possiblities listed on Service Sheet BD4.

Test Equipment

Signature Analyzer ....HP 5004A

Test 1. Address Check

Purpose. Verify ability of the Microprocessor to run through entire address range.

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'E' A11TP11
3) START to 'ADR 15' A11TP4
4) STOP to 'ADR 15' A11TP4

Set the signature analyzer's controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Generator as follows:

1) The TEST/NRM switch P/O A11S1 to TEST.
2) The ROM/NRM switch P/O A11S1 to ROM.

Probe. Connect the probe to the node indicated in Table 1. Verify that each signature is correct and stable.

After the signatures are taken, reset the TEST/NRM switch to NRM and the ROM/NRM switch to NRM position.

SERVICE SHEET 14 (Cont'd)

Table 1. Microprocessor Address Signatures

Node	Correct Signature	Comments
+5V U13 #35	0001	Address Lines
A0 U13 #9	5555	
A1 U13 #10	CCCC	
A2 U13 #11	7F7F	
A3 U13 #12	5H21	
A4 U13 #13	0AFA	
A5 U13 #14	UPFH	
A6 U13 #15	52F8	
A7 U13 #16	HC89	
A8 U13 #17	2H70	
A9 U13 #18	HPPO	
A10 U13 #19	1293	
A11 U13 #20	HAP7	
A12 U13 #22	3C96	
A13 U13 #23	3827	
A14 U13 #24	755U	
*A15 U13 #25	0000	
+5V	0001	Buffered Address Lines
A0 J4 #2	5555	
A1 J4 #3	CCCC	
A2 J4 #4	7F7F	
A3 J4 #5	5H21	
A4 J4 #6	0AFA	
A5 J4 #7	UPFH	
A6 J4 #8	52F8	
A7 J4 #9	HC89	
A8 J4 #10	2H70	
A9 J4 #11	HPP0	
A10 J4 #12	1293	
A11 J4 #13	HAP7	
A12 J4 #14	3C96	
A13 J4 #15	3827	
A14 J4 #16	755U	
*A15 J2 #5	0000	

*Even though the signature equals zero, the probe tip should blink.

st 2. Data Bus Verification

pose. To test the Microprocessor and circuit rd digital logic.

up. Connect the signature analyzer as follows:

GND as close to circuitry being probed as possible (bad grounding can cause unstable signatures).

2) CLK to 'E' A11TP11
3) START to 'SA1' A11TP5
4) STOP to 'SA2' A11TP6

Set the signature analyzer controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN

Set up the Signal Generator as follows:

1) Disconnect the attenuator cable W17 from the power supply board to the attenuator.
2) Set the LOGIC/RAM switch P/O A11S1 to LOGIC.

NOTE

If the Signal Generator's address switch has been set to other than '07', the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON. Refer to Service Sheet 17 for location of the address switches.

Initialize. Briefly short A11TP3 'NMI' to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the 'RST/RUN' switch to 'RST' and then 'RUN'. Briefly touch the 'NMI' test point to ground.

Probe. Connect the probe to the node indicated in Table 2. Verify that each signature is correct and stable.

NOTE

If the signatures in the first portion of the following table are incorrect, the signatures for the second portion will also be incorrect.

SERVICE SHEET 14 (Cont'd)

Table 2. Microprocessor Data Bus Signatures

Node	Correct Signature	Comments
+5V	H6H5	Data Bus Signatures are subject to setting of HP-IB address switches.
*D0 U13 #33	75HI	
D1 U13 #32	2H55	
D2 U13 #31	197C	
D3 U13 #30	0926	
D4 U13 #29	4F62	
D5 U13 #28	52U5	
D6 U13 #27	088H	
D7 U13 #26	3001	
+5V	H6H5	Buffered Data Bus Signatures are subject to setting of HP-IB address switches.
*D0 J2 #16	4U4A	
D1 J2 #15	A132	
D2 J2 #14	1A47	
D3 J2 #13	4989	
D4 J2 #12	5586	
D5 J2 #11	307C	
D6 J2 #10	0F11	
D7 J2 #9	8130	

*This signature may vary from unit-to-unit due to differences in one-shot timing of A2U28B. If SA6 A11TP10 is connected to SA7 A2TP15, the signature should read the same as above.

Reset the LOGIC/RAM switch to the RAM position. Reconnect attenuator cable W17.

NOTE

If the HP-IB address switch was changed, reset the address switch (Service Sheet 17) to the original address. Set the front panel RESET-STBY-ON switch to RESET and back to ON.

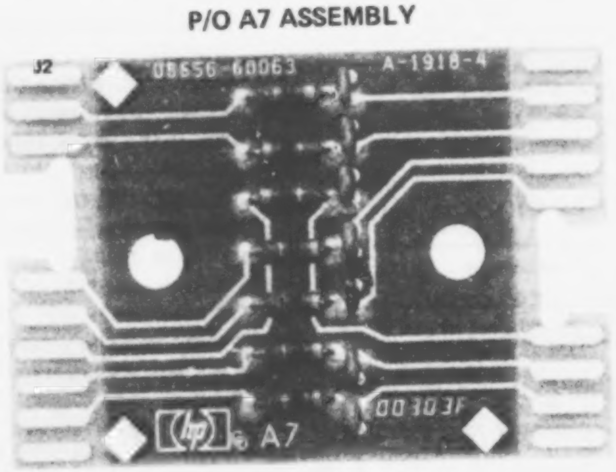


Figure 8-83. A7 Assembly Interrupt Input Component Locations

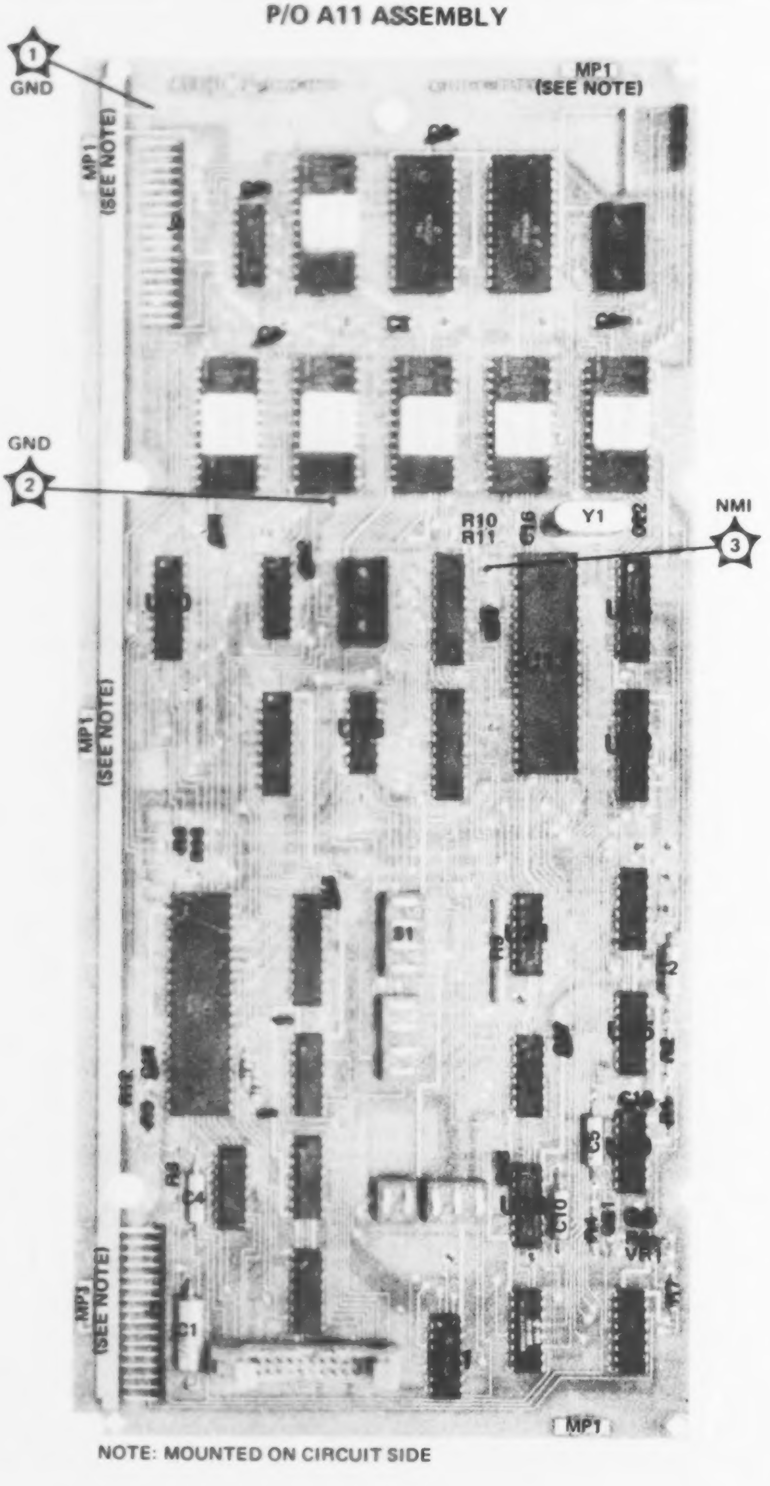

P/O A11 ASSEMBLY
1
GND
MP1
(SEE NOTE)
MP1
(SEE NOTE)
GND
2
R10
R11
C16
Y1
NMI
3
MP1
(SEE NOTE)
C1
C4
C5
C10
VR1
MP1
(SEE NOTE)
MP1
NOTE: MOUNTED ON CIRCUIT SIDE

Figure 8-84. Microprocessor, Interrupt Processing and Restart Component Locations

oi
ri
on
ne
n
h
I
V
a
el

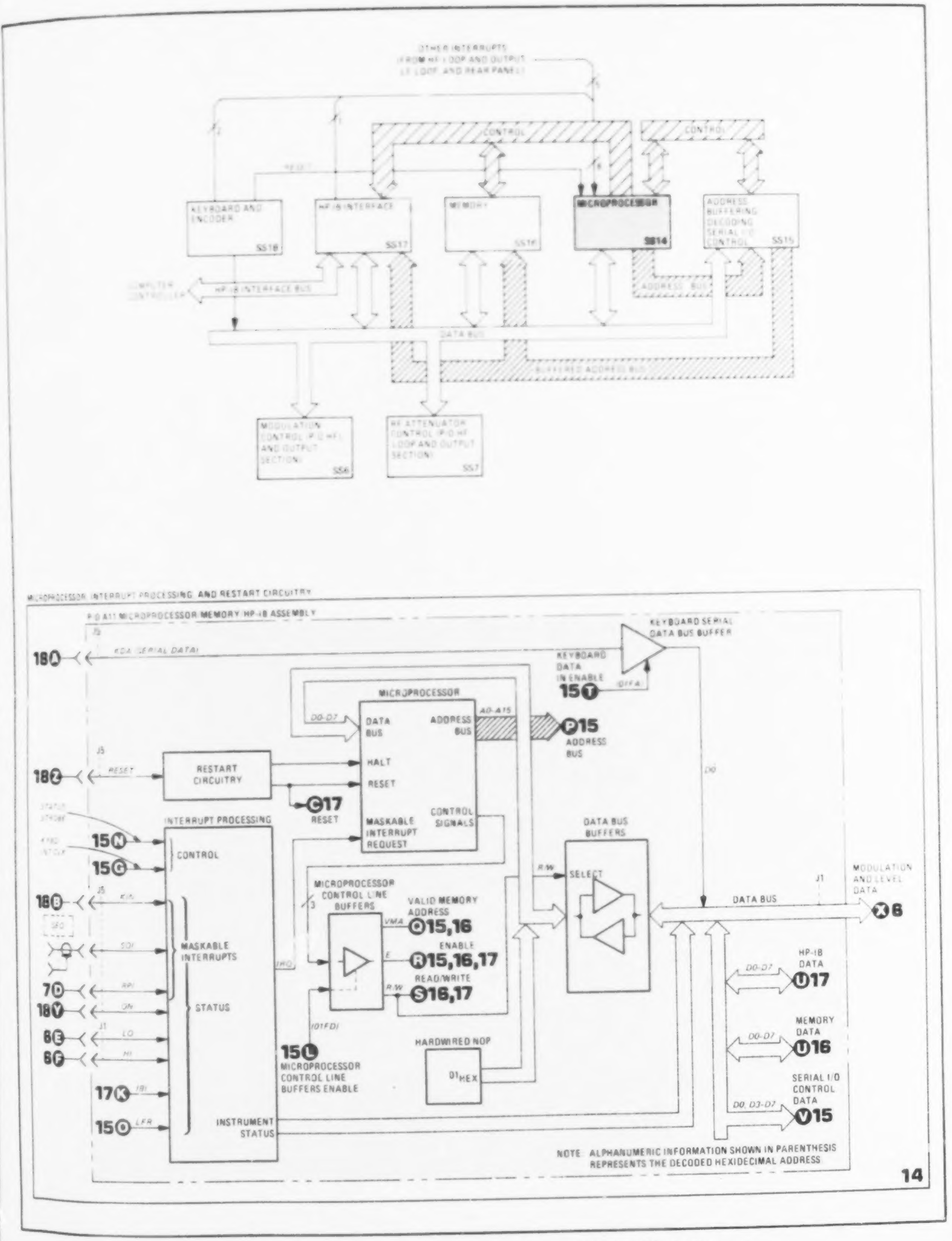
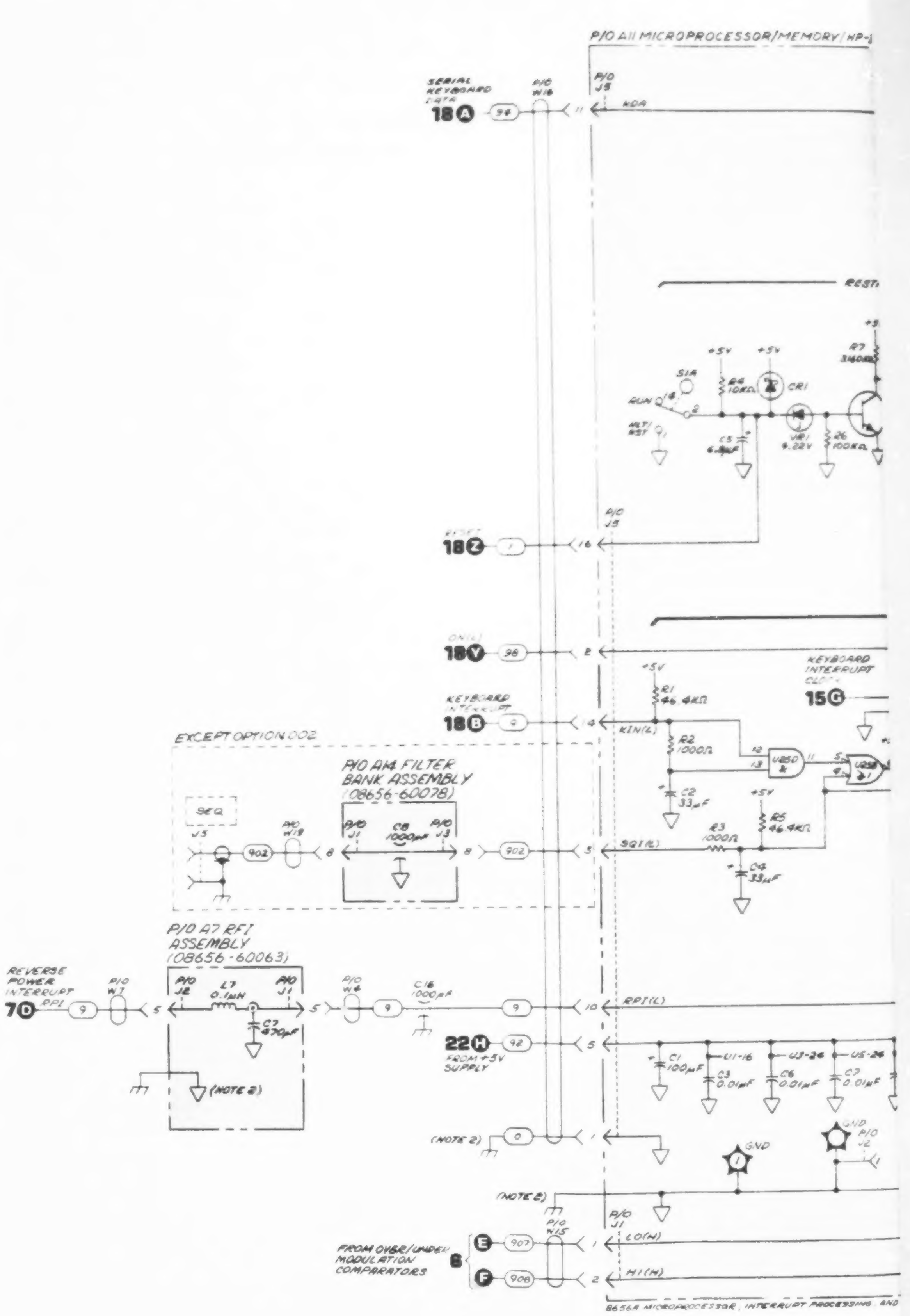
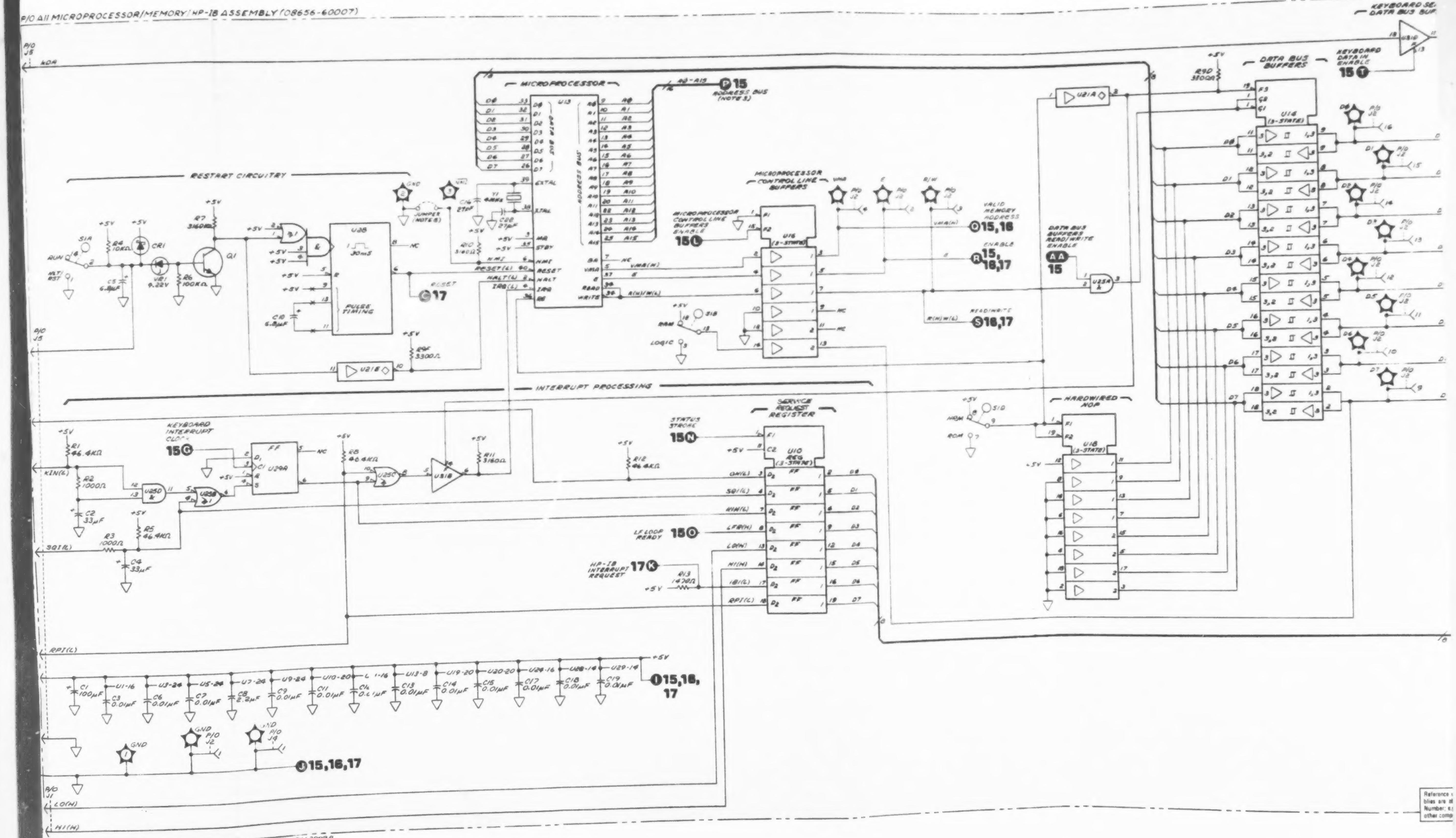

OTHER INTERRUPTS (FROM HF LOOP AND OUTPUT LF LOOP, AND REAR PANEL)
CONTROL
KEYBOARD AND ENCODER SS18
HP-IB INTERFACE SS17
MEMORY SS16
MICROPROCESSOR SS14
ADDRESS BUFFERING DECODING SERIAL I/O CONTROL SS15
COMPUTER CONTROLLER
HP-IB INTERFACE BUS
ADDRESS BUS
DATA BUS
BUFFERED ADDRESS BUS
MODULATION CONTROL (P/O HF LOOP AND OUTPUT SECTION) SS6
RF ATTENUATOR CONTROL (P/O HF LOOP AND OUTPUT SECTION) SS7
MICROPROCESSOR, INTERRUPT PROCESSING, AND RESTART CIRCUITRY
P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY
18A
KDA (SERIAL DATA)
KEYBOARD SERIAL DATA BUS BUFFER
KEYBOARD DATA IN ENABLE
15T
MICROPROCESSOR
DATA BUS
ADDRESS BUS
A0-A15
P15
ADDRESS BUS
HALT
RESET
18Z
RESTART CIRCUITRY
C17
RESET
MASKABLE INTERRUPT REQUEST
CONTROL SIGNALS
INTERRUPT PROCESSING
15N
15G
CONTROL
18B
MASKABLE INTERRUPTS
7D
18Y
STATUS
6E
6F
17K
15O
INSTRUMENT STATUS
MICROPROCESSOR CONTROL LINE BUFFERS
VALID MEMORY ADDRESS
O15,16
ENABLE
R15,16,17
READ/WRITE
S16,17
15L
MICROPROCESSOR CONTROL LINE BUFFERS ENABLE
HARDWIRED NOP
01HEX
DATA BUS BUFFERS
SELECT
DATA BUS
MODULATION AND LEVEL DATA
X6
HP-IB DATA
U17
MEMORY DATA
U16
SERIAL I/O CONTROL DATA
V15
NOTE: ALPHANUMERIC INFORMATION SHOWN IN PARENTHESIS REPRESENTS THE DECODED HEXIDECIMAL ADDRESS
14

Figure 8-85. Microprocessor, Interrupt Processing and Restart Block Diagrams


P/O A11 MICROPROCESSOR/MEMORY/HP-I
SERIAL KEYBOARD DATA
18A
KDA
RESET
18Z
ON(L)
18Y
KEYBOARD INTERRUPT
18B
KIN(L)
KEYBOARD INTERRUPT CLOCK
15G
EXCEPT OPTION 002
P/O A14 FILTER BANK ASSEMBLY (08656-60078)
SEQ
SQI(L)
P/O A7 RFI ASSEMBLY (08656-60063)
REVERSE POWER INTERRUPT
7D
RPI(L)
22H
FROM +5V SUPPLY
(NOTE 2)
FROM OVER/UNDER MODULATION COMPARATORS
6
E
F
LO(H)
HI(H)
8656A MICROPROCESSOR, INTERRUPT PROCESSING, AND


P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY (08656-60007)
KEYBOARD SE
DATA BUS BUF
MICROPROCESSOR
U13
A0-A15
P 15
ADDRESS BUS (NOTE 3)
RESTART CIRCUITRY
S1A
RUN
INT/RST
R4 10KΩ
C5 6.8μF
CR1
VR1 9.22V
R6 100KΩ
R7 3160Ω
Q1
U28
30mS
PULSE TIMING
C10 6.8μF
R9F 3300Ω
U21B
JUMPER (NOTE 6)
C16 27pF
Y1 4MHz
C20 27pF
R10 3160Ω
EXTAL
XTAL
NMI
RESET(L)
HALT(L)
IRQ(L)
MR
STBY
HALT
VMA
READ
WRITE
VMA(H)
R(H)/W(L)
RESET
G 17
MICROPROCESSOR CONTROL LINE BUFFERS
MICROPROCESSOR CONTROL LINE BUFFERS ENABLE
15 L
U15 (3-STATE)
VMA
E
R/W
VALID MEMORY ADDRESS
Q 15,16
ENABLE
R 15,16,17
READ/WRITE
R(H)W(L)
S 16,17
S1B
RAM
LOGIC
DATA BUS BUFFERS READ/WRITE ENABLE
AA 15
U21A
U25A
R40 3300Ω
DATA BUS BUFFERS
KEYBOARD DATA IN ENABLE
15 T
U14 (3-STATE)
U31B
P/O J2
D0
D1
D2
D3
D4
D5
D6
D7
INTERRUPT PROCESSING
KEYBOARD INTERRUPT CLOCK
15 G
FF
U29A
U25D
U25B
U25C
U31B
R1 46.4KΩ
R2 1000Ω
C2 33μF
R3 1000Ω
R5 46.4KΩ
C4 33μF
R8 46.4KΩ
R11 3160Ω
R12 46.4KΩ
KIN(L)
SQI(L)
RPI(L)
STATUS STROBE
15 N
SERVICE REQUEST REGISTER
U10 REG (3-STATE)
QH(L)
SQI(L)
KIN(L)
LFR(H)
LO(H)
HI(H)
IBI(L)
RPI(L)
LF LOOP READY
15 O
HP-IB INTERRUPT REQUEST
17 K
R13 1470Ω
HARDWIRED NOP
S1D
NOP
ROM
U18 (3-STATE)
C1 100μF
C3 0.01μF
C6 0.01μF
C7 0.01μF
C8 2.2μF
C9 0.01μF
C11 0.01μF
C12 0.01μF
C13 0.01μF
C14 0.01μF
C15 0.01μF
C17 0.01μF
C18 0.01μF
C19 0.01μF
U1-16
U3-24
U5-24
U7-24
U9-24
U10-20
U11-16
U13-8
U19-20
U20-20
U24-16
U28-16
U29-14
+5V
O 15,16,17
GND
P/O J2
P/O J4
J 15,16,17
P/O J1
LO(H)
HI(H)
P/O J5
KDA
Reference
blies are
Number;
other comp

8656A MICROPROCESSOR, INTERRUPT PROCESSING, AND RESTART CIRCUITRY: 2009A

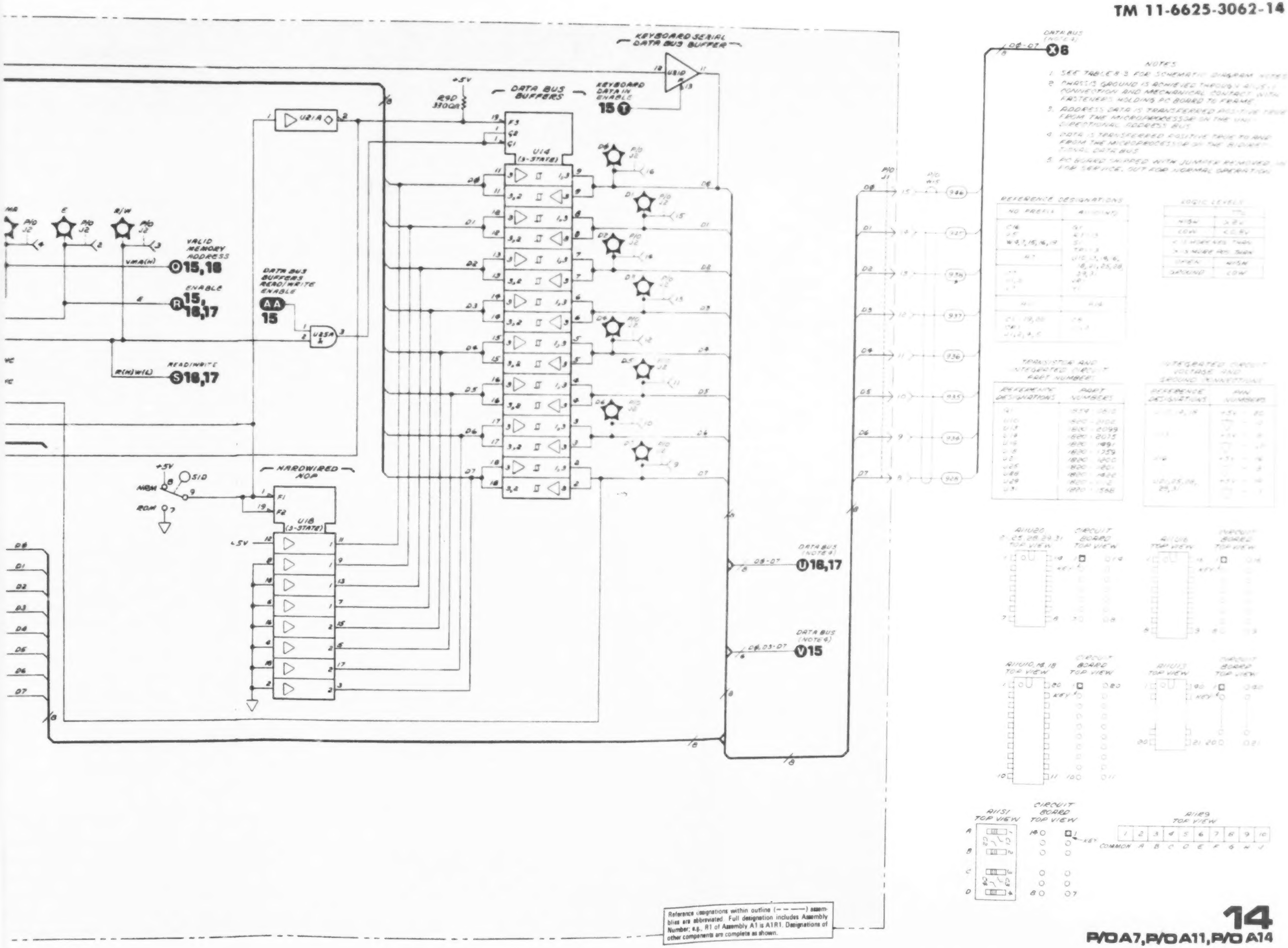

KEYBOARD SERIAL DATA BUS BUFFER
DATA BUS BUFFERS
KEYBOARD DATA IN ENABLE
15 T
U14 (3-STATE)
U21A
R9D 330ΩR
+5V
VALID MEMORY ADDRESS
O 15,16
ENABLE
R 15,16,17
READ/WRITE
S 16,17
DATA BUS BUFFERS READ/WRITE ENABLE
AA 15
U25A
HARDWIRED NOP
U18 (3-STATE)
NRM
ROM
SID
DATA BUS (NOTE 4)
D0-D7
U 16,17
D0,D3-D7
V 15
X 8
P/O J1
P/O J2
NOTES
1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES
2. CHASSIS GROUND IS ACHIEVED THROUGH A11J5-1 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. ADDRESS DATA IS TRANSFERRED POSITIVE TRUE FROM THE MICROPROCESSOR ON THE UNIDIRECTIONAL ADDRESS BUS
4. DATA IS TRANSFERRED POSITIVE TRUE TO AND FROM THE MICROPROCESSOR ON THE BIDIRECTIONAL DATA BUS
5. PC BOARD SHIPPED WITH JUMPER REMOVED. IN FOR SERVICE, OUT FOR NORMAL OPERATION
REFERENCE DESIGNATIONS
LOGIC LEVELS
TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS
INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS
CIRCUIT BOARD TOP VIEW
TOP VIEW
KEY
COMMON
Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.
14
P/O A7, P/O A11, P/O A14

Figure 8-86. Microprocessor, Interrupt Processing and Restart Schematic Diagram

SERVICE SHEET 15
P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

Control of the major functions of the Signal Generator are contained on the circuits of Service Sheet 15. Direct control is exerted on almost all of the analog functions of the instrument such as frequency, amplitude and modulation. Addresses from the Microprocessor are decoded and the accompanying data (either series or parallel) is manipulated to set various output modes, levels and frequencies. In addition, many purely digital functions such as control of keyboard, display and data bus are decoded here. The Address Bus Buffers U12 and U17 are always enabled during normal operation.

Address Decoders

U22 outputs the Data Bus Buffer Read/Write Enable signal, signature analyzer enable signals and enable signals for U1 and U24. A Valid Memory Address and a low on A14 are required to decode A7, A8 and A9.

U1 outputs strobes that control modulation and attenuation data. Series data contol strobes and Microprocessor related control signals are output by U24. Both U1 and U24 are enabled by the output from U22 and the enable E(H) clock. Address A3 determines which of U1 or U22 is active at a given time. Addresses A0, A1 and A2 are decoded to produce the individual control signals.

Serial I/O Control

The Serial I/O Control Clock/Strobe Enable Flip-Flop U29B provides an enable signal to the Serial I/O Control Clock/Strobe Generator U33. U33 controls the serial data flow from the keyboard, to the display and to the phase lock loops. Encoded data and strobes are received from the data bus by the Serial I/O Control Register U32. U32 passes the encoded information to the serial data lines and to U33.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

Troubleshooting is done on the circuits of Service Sheet 15 when a defect seems to be related to the Display, Keyboard, or control of the other major sections of the instrument. Examples are the High Frequency Loop, the Output Section and the Low Frequency Loop. If the signatures shown in the tables are correct but the problem is related to another major section of this instrument, refer to:

1) Service Sheet BD2 for Output or High Frequency Loop problems
2) Service Sheet BD3 for Low Frequency Loop problems.

SERVICE SHEET 15 (Cont'd)

If the signatures are incorrect, the circuits of Service Sheets 14, 16, 17 or 18 (the Microprocessor, ROM and RAM, the Keyboard or the HP-IB Interface) may be defective. As a last resort, return to Service Sheet BD4 or possibly Service Sheet BD1 and consider the other possiblities shown.

Test Equipment

Signature Analyzer ....HP 5004A

Purpose. To verify transmission of encoded addresses and data from the Microprocessor through the decoders, strobe generators and registers.

Setup. Connect the signature analyzer as follows:

1) GND as close to the circuitry being probed as possible. Bad grounding can cause unstable signatures.
2) CLK to 'E' A11TP11
3) START to 'SA1' A11TP5
4) STOP to 'SA2' A11TP6

Set the signature analyzer's controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN

Set up the Signal Generator as follows:

1) Disconnect the attenuator cable W17 from the power supply board to the attenuator.
2) Set the LOGIC/RAM switch P/O A11S1 to the LOGIC position.

NOTE

If the Signal Generator's address switch has been set to other than '07', the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON. Refer to Service Sheet 17 for location of the address switches.

Initialize. Briefly short A11TP3 'NMI' to ground.

NOTE

With careless probing, it is possible to get the Microprocessor into a program sequence other than that intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the 'RST/RUN' switch to 'RST' and then 'RUN'. Briefly touch the 'NMI' test point to ground.

Probe. Connect the probe as indicated in Table 1. Verify that the signature is correct and stable as shown.

SERVICE SHEET 15 (Cont'd)

Table 1. Interface Signatures

Node	Correct Signature	Comments
+5V	H6H5	
U22 #7	UA17	
*U22 #12	8690	SA CLK(RF)
U24 #7	330C	SER CLK EN
U24 #9	6H08	SER CLK EN
U29 #9	42H7	SER LATCH
U33 #11	6468	
U33 #12	6F77	
+5V	H6H5	
U33 #14	C45F	
U33 #15	2841	
U32 #2	5401	
U32 #5	UC8P	
U32 #7	9PPA	
U32 #10	75UP	
*U32 #15	7064	SA Strobe/Stop
*U31 #8	FP00	
*U31 #9	FP00	
+5V	H6H5	
U1 #15	58AP	U5 strobe
U1 #14	57F4	U9 strobe
U1 #13	97CC	U13 strobe
U1 #12	A5FP	U16 strobe
U1 #11	P1H1	U19 strobe

*This node is only used to control the signature analyzer during the display and RF interface test.

Reset the LOG/RAM switch to the RAM position. Reconnect attenuator cable W17.

NOTE

If the HP-IB address switch was changed, reset the address switch (service sheet 17) to the original address. Set the front panel RESET-STBY-ON switch to RESET and back to ON.

◀ Microprocessor, Interrupt Processing and Restart
P/O A7, P/O A11, P/O A14
SERVICE SHEET 14

P/O A11 ASSEMBLY

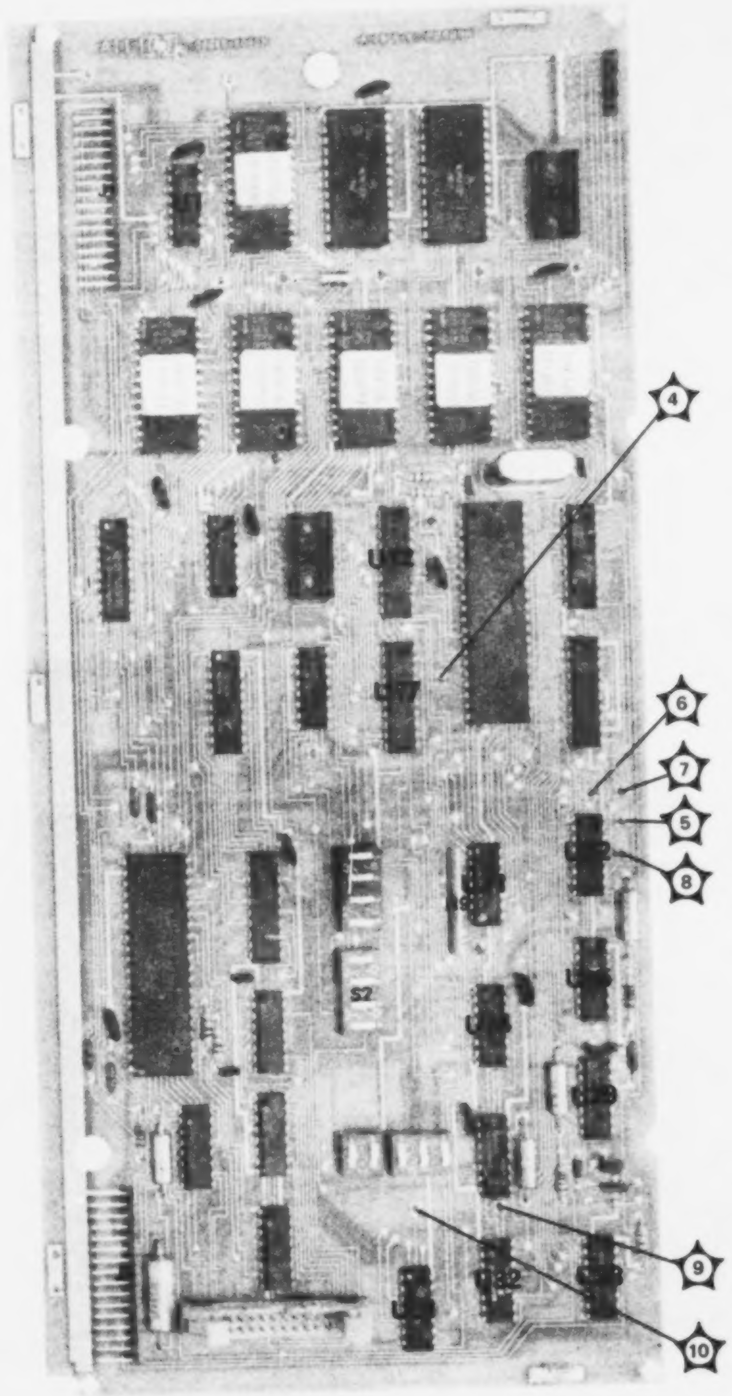

U12
U17
S2
U32
4
6
7
5
8
9
10

Figure 8-87. Address Buffering and Decoding, Serial I/O and Control Component Locations

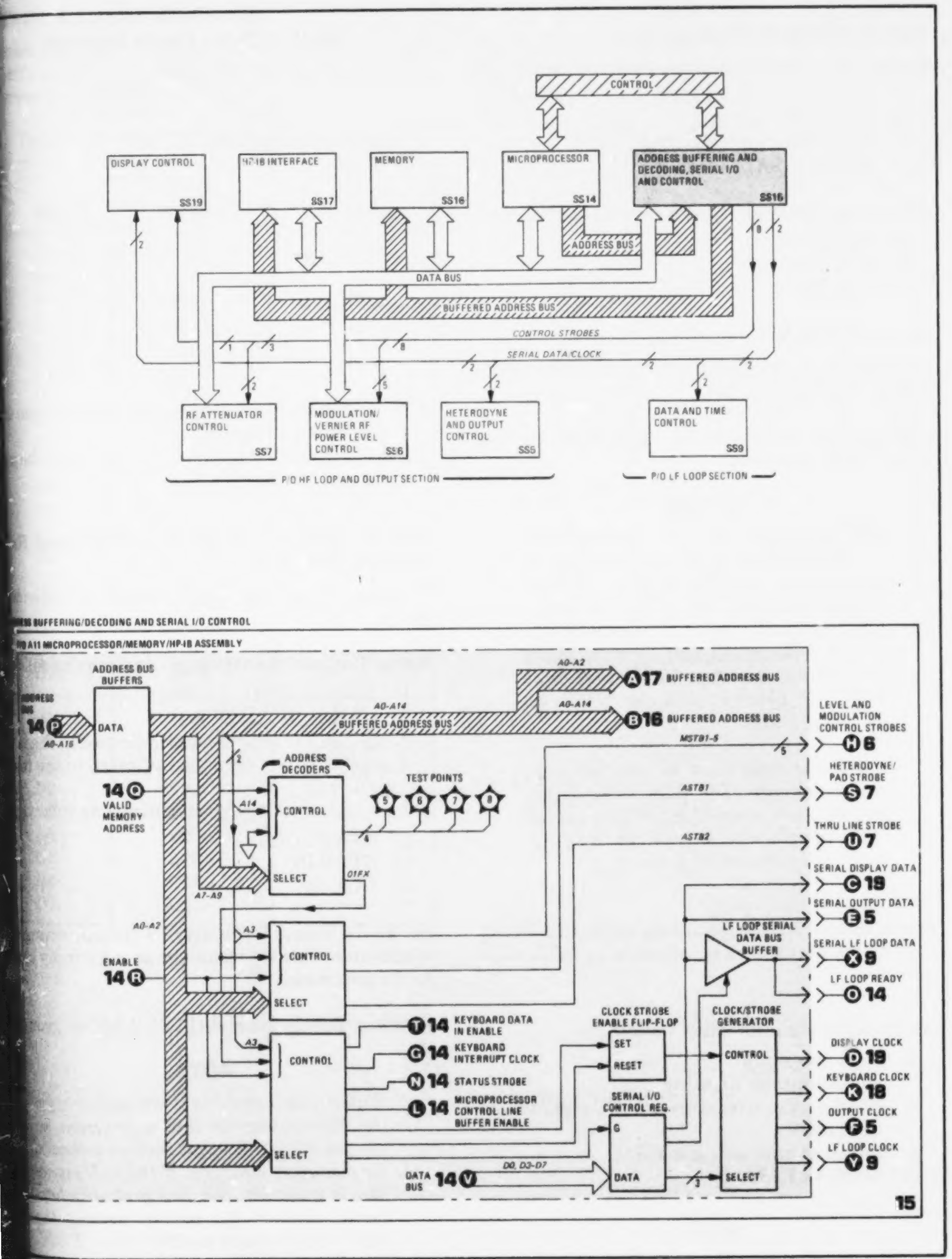
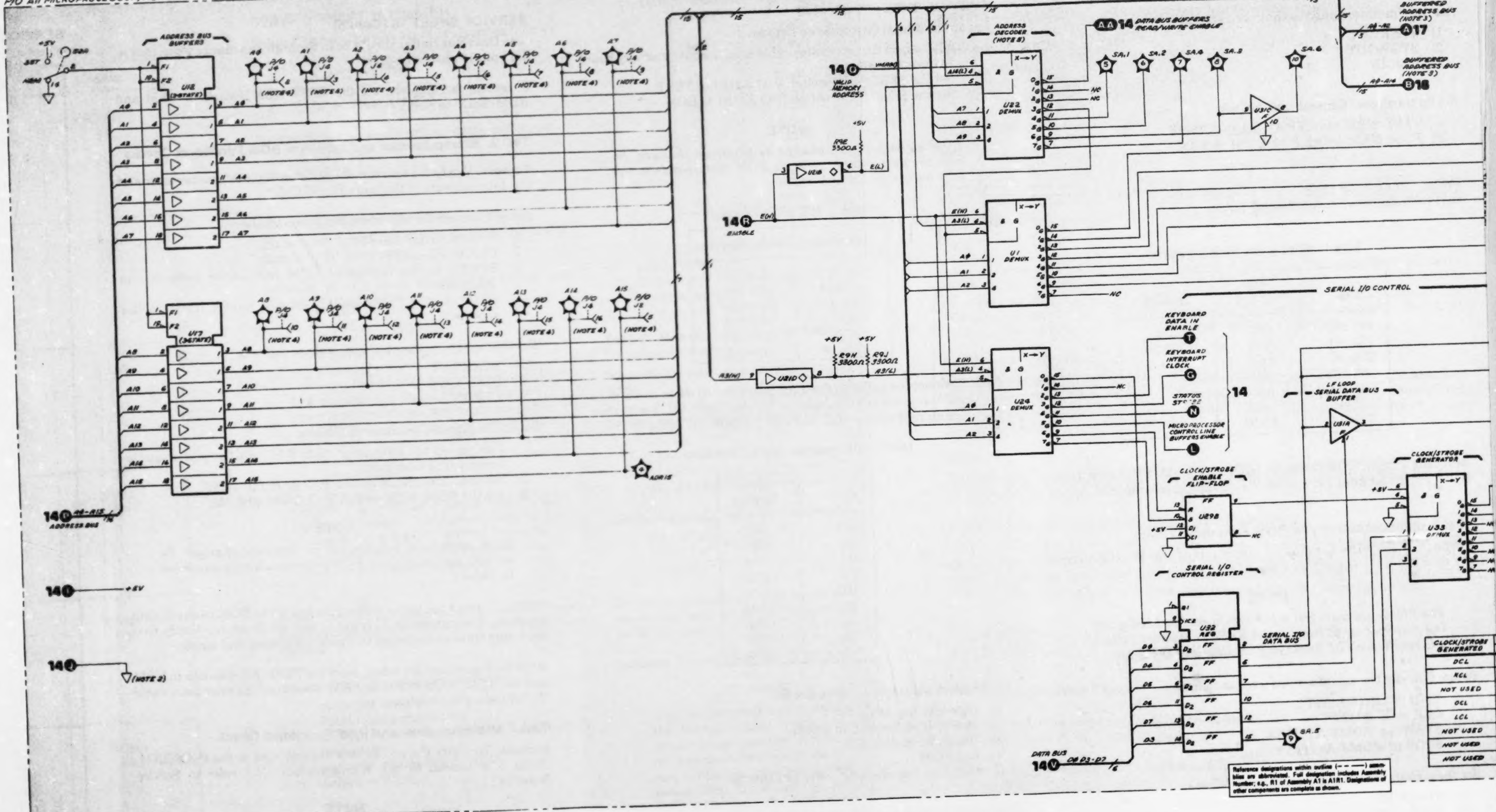

CONTROL
DISPLAY CONTROL SS19
HP-IB INTERFACE SS17
MEMORY SS16
MICROPROCESSOR SS14
ADDRESS BUFFERING AND DECODING, SERIAL I/O AND CONTROL SS15
ADDRESS BUS
DATA BUS
BUFFERED ADDRESS BUS
CONTROL STROBES
SERIAL DATA/CLOCK
RF ATTENUATOR CONTROL SS7
MODULATION/ VERNIER RF POWER LEVEL CONTROL SS6
HETERODYNE AND OUTPUT CONTROL SS5
DATA AND TIME CONTROL SS9
P/O HF LOOP AND OUTPUT SECTION
P/O LF LOOP SECTION
BUFFERING/DECODING AND SERIAL I/O CONTROL
A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY
ADDRESS BUS BUFFERS
ADDRESS BUS 14 P
A0-A15
DATA
A0-A14
BUFFERED ADDRESS BUS
A0-A2
A17 BUFFERED ADDRESS BUS
B16 BUFFERED ADDRESS BUS
14 Q VALID MEMORY ADDRESS
ADDRESS DECODERS
CONTROL
SELECT
A14
A7-A9
01FX
TEST POINTS
5 6 7 8
MSTB1-5
LEVEL AND MODULATION CONTROL STROBES
H 6
ASTB1
HETERODYNE/ PAD STROBE
S 7
ASTB2
THRU LINE STROBE
U 7
SERIAL DISPLAY DATA
C 19
SERIAL OUTPUT DATA
E 5
LF LOOP SERIAL DATA BUS BUFFER
SERIAL LF LOOP DATA
X 9
LF LOOP READY
O 14
A3
ENABLE 14 R
T 14 KEYBOARD DATA IN ENABLE
G 14 KEYBOARD INTERRUPT CLOCK
N 14 STATUS STROBE
L 14 MICROPROCESSOR CONTROL LINE BUFFER ENABLE
CLOCK STROBE ENABLE FLIP-FLOP
SET
RESET
CLOCK/STROBE GENERATOR
SERIAL I/O CONTROL REG.
G
DATA BUS 14 V
D0, D3-D7
DATA
DISPLAY CLOCK
D 19
KEYBOARD CLOCK
K 18
OUTPUT CLOCK
F 5
LF LOOP CLOCK
Y 9
15

Figure 8-88. Address Buffering and Decoding, Serial I/O and Control Block Diagrams

P/O A11 MICROA
+5V
3S7
MEM
14
14 P A0-A15 ADDRESS BUS
14 Q
14 R
MEGA ADDRESS BU

P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY (08656-60007)†


ADDRESS BUS BUFFERS
U18 (3STATE)
U17 (3STATE)
+5V
SET
NORM
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
P/O J4
P/O J5
(NOTE 4)
ADRIS
14 A0-A15 ADDRESS BUS
14 +5V
14 (NOTE 2)
14 VALID MEMORY ADDRESS
VMA
+5V
R9E 3300Ω
U21B
E(L)
14 R ENABLE
E(H)
R9H 3300Ω
R9J 3300Ω
A3(H)
U21D
A3(L)
ADDRESS DECODER (NOTE 5)
U22 DEMUX
U1 DEMUX
U24 DEMUX
X→Y
NC
AA 14 DATA BUS BUFFERS READ/WRITE ENABLE
SA.1
SA.2
SA.4
SA.3
SA.6
U31C
BUFFERED ADDRESS BUS (NOTE 5)
A0-A10
A17
BUFFERED ADDRESS BUS (NOTE 5)
A0-A14
B16
SERIAL I/O CONTROL
KEYBOARD DATA IN ENABLE
KEYBOARD INTERRUPT CLOCK
STATUS STROBE
MICROPROCESSOR CONTROL LINE BUFFERS ENABLE
14
LF LOOP SERIAL DATA BUS BUFFER
U31A
CLOCK/STROBE ENABLE FLIP-FLOP
U29B
FF
CLOCK/STROBE GENERATOR
U33 DEMUX
SERIAL I/O CONTROL REGISTER
U32 REG
SERIAL I/O DATA BUS
SA.5
DATA BUS
14 V D0 D3-D7

CLOCK/STROBE GENERATED
DCL
KCL
NOT USED
OCL
LCL
NOT USED
NOT USED
NOT USED

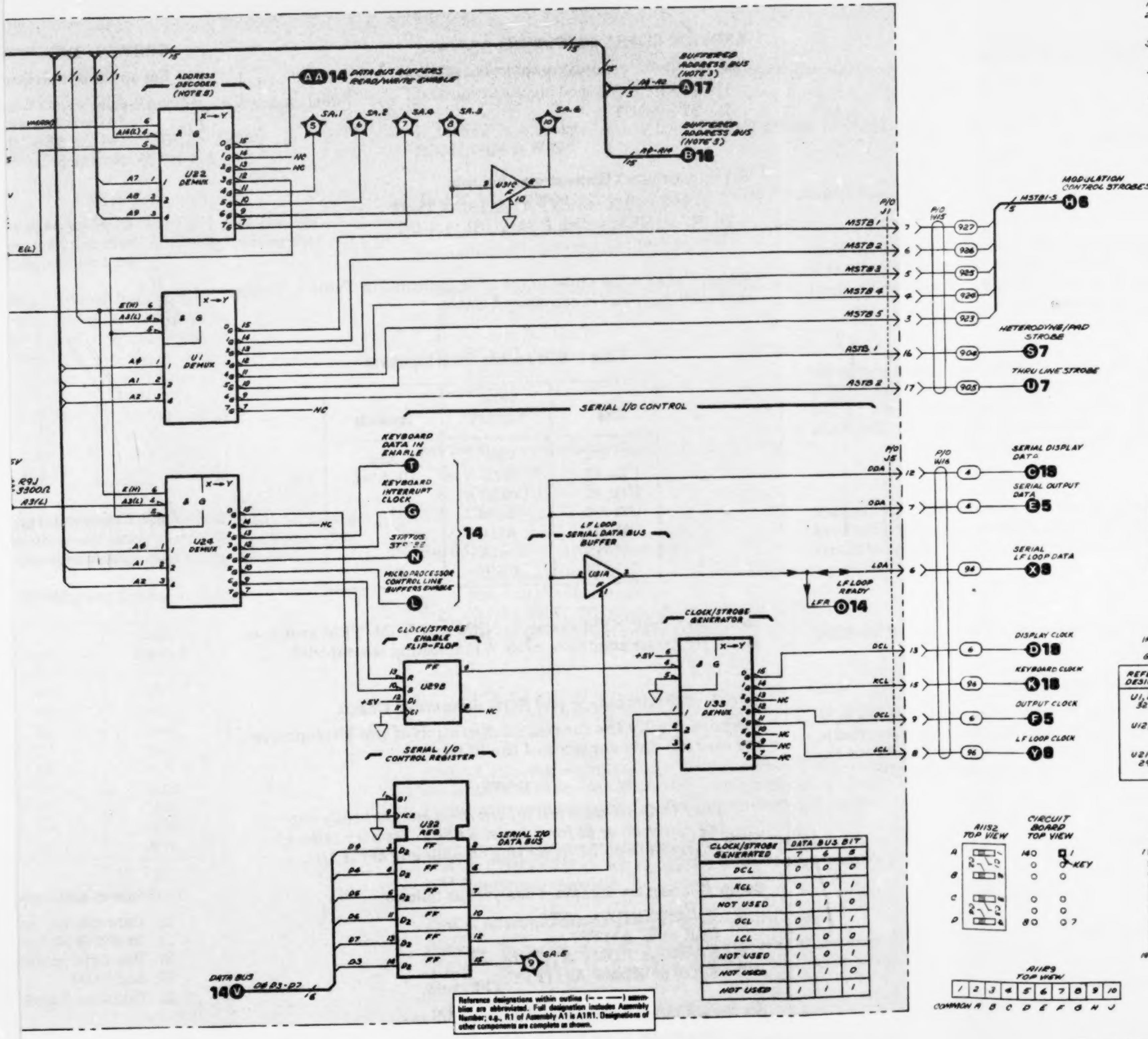
Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

8656A ADDRESS BUFFERING/DECODING AND SERIAL I/O CONTROL: 2022A

NOTES

1. SEE TABLE 8-8 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A11J5-1 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. ADDRESS DATA IS TRANSFERRED POSITIVE TRUE FROM THE MICROPROCESSOR ON THE UNIDIRECTIONAL BUFFERED ADDRESS BUS.
4. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKETS J2 OR J4.

† INDICATES CIRCUIT CHANGES. SEE SECTION VII.


ADDRESS DECODER (NOTE 5)
U22 DEMUX
U1 DEMUX
U24 DEMUX
X→Y
A7
A8
A9
A0
A1
A2
E(H)
E(L)
A3(L)
A11(L)
R9J 3300Ω
NC
AA 14 DATA BUS BUFFERS READ/WRITE ENABLE
SA.1
SA.2
SA.4
SA.3
SA.6
U31C
BUFFERED ADDRESS BUS (NOTE 3)
A0-A10
A17
A0-A14
B18
P/O J1
P/O W15
MSTB 1
MSTB 2
MSTB 3
MSTB 4
MSTB 5
ASTB 1
ASTB 2
927
926
925
924
923
904
905
MSTB1-5
MODULATION CONTROL STROBES
H6
HETERODYNE/PAD STROBE
S7
THRU LINE STROBE
U7
SERIAL I/O CONTROL
KEYBOARD DATA IN ENABLE
KEYBOARD INTERRUPT CLOCK
STATUS STROBE
MICROPROCESSOR CONTROL LINE BUFFERS ENABLE
14
LF LOOP SERIAL DATA BUS BUFFER
U31A
LF LOOP READY
LFR
O14
CLOCK/STROBE ENABLE FLIP-FLOP
U29B
FF
+5V
CLOCK/STROBE GENERATOR
U33 DEMUX
SERIAL I/O CONTROL REGISTER
U32 REG
SERIAL I/O DATA BUS
SA.5
DATA BUS
14V
D0 D3-D7
P/O J5
P/O W16
DDA
ODA
LDA
DCL
KCL
OCL
LCL
SERIAL DISPLAY DATA
C18
SERIAL OUTPUT DATA
E5
SERIAL LF LOOP DATA
X8
DISPLAY CLOCK
D18
KEYBOARD CLOCK
K18
OUTPUT CLOCK
F5
LF LOOP CLOCK
Y8

CLOCK/STROBE GENERATED	DATA BUS BIT 7	DATA BUS BIT 6	DATA BUS BIT 5
DCL	0	0	0
KCL	0	0	1
NOT USED	0	1	0
OCL	0	1	1
LCL	1	0	0
NOT USED	1	0	1
NOT USED	1	1	0
NOT USED	1	1	1

Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

REFERENCE DESIGNATIONS

NO PREFIX	A11
W15,16	J1,2,4,5 R9 S2 TP4-10 U1,12,17,21, 22,24,25, 29,31-33

LOGIC LEVELS

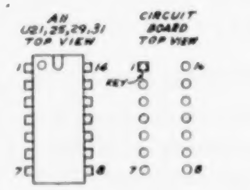
	TTL
HIGH	> 2V
LOW	< 0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

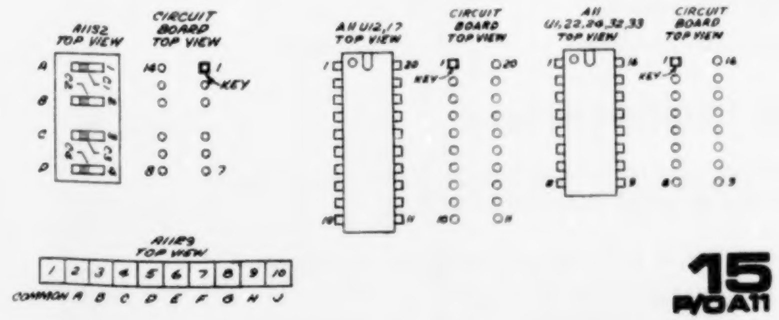
INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1,24	1820-1240
U12,17	1820-1759
U21	1820-1200
U22,33	1820-1216
U25	1820-1201
U29	1820-1112
U31	1820-1568
U32	1820-2056

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1,22,24, 32,33	+5V -16 ▽ -8
U12,17	+5V -20 ▽ -10
U21,25, 29,31	+5V -14 ▽ -7


A11 U21,25,29,31 TOP VIEW
CIRCUIT BOARD TOP VIEW
1
14
7
8
KEY


A11S2 TOP VIEW
CIRCUIT BOARD TOP VIEW
A
B
C
D
14
8
1
7
KEY
A11 U12,17 TOP VIEW
CIRCUIT BOARD TOP VIEW
1
20
10
11
A11 U1,22,24,32,33 TOP VIEW
CIRCUIT BOARD TOP VIEW
1
16
8
9
A11P3 TOP VIEW
1 2 3 4 5 6 7 8 9 10
COMMON A B C D E F G H J

15
P/O A11

Figure 8-89. Address Buffering and Decoding. Serial I/O and Control Schematic Diagram

SERVICE SHEET 16
P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The memory circuits, except for the Microprocessor's internal RAM (Read/Write Memory) are part of the circuits shown on Service Sheet 16. The individual RAM is selected by direct addressing. The ROM (Read Only Memory) is selected by direct addressing and by means of the ROM Select Decoder U11.

RAM

Valid Memory Address VMA and the enable (clock) E are the inputs that enable the RAM, U3 and U4. Address A14 must be low while A7 and A8 determine which RAM is selected. The Read/Write mode is selected by the control signal placed on pin 16. The memory location in each RAM is selected by addresses A0 through A6. The RAM input/output is connected directly to the data bus D0 through D7.

ROM Select Decoder

The Valid Memory Address VMA and enable (clock) E enable a ROM or the interface bus select IB SEL via the ROM Select Decoder U11. Address A14 (at the Buffered Address Bus) must be high while A11, A12 and A13 are decoded to select one of the six ROM or the interface bus select IB SEL(L).

ROM

Addresses A0 through A10 select the ROM memory location. The outputs of the ROM are connected to the Data Bus D0 through D7.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

Troubleshooting is done to the circuits of Service Sheet 16 when a defect seems to be related to the ROM or RAM circuits. The only troubleshooting information provided is signature analysis. If nothing definite is discovered in performing these checks, refer to Service Sheet 14 or consider the other possibilities listed on Service Sheet BD4.

Test Equipment

Signature Analyzer ....HP 5004A

Test 1. ROM Address Select

Purpose. Verify the ability of the Microprocessor to select the correct ROM/RAM address.

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'E' A11TP11
3) START to 'ADR 15' A11TP4
4) STOP to 'ADR 15' A11TP4

SERVICE SHEET 16 (Cont'd)

Set the signature analyzer controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Generator as follows:

1) TEST/NRM switch P/O A11S1 to TEST.
2) ROM/NRM switch P/O A11S1 to ROM.

Probe. Connect the probe to the node indicated in Table 1. Verify that each signature is correct and stable.

Table 1. ROM Address Select Signatures

Node	Correct Signature	Comments
U21 #12	755P	A14
U11 #7	826U	Chip Sel
U11 #9	603C	
U11 #10	54F5	
U11 #11	A711	
U11 #12	AA6A	
U11 #13	A3UH	

Reset the TEST/NRM switch to NRM and ROM/NRM switch to NRM; reconnect attenuator cable W17 if testing is completed.

Test 2. Microprocessor and ROM Functional Check

Purpose. Verify the functional operation of the Microprocessor and the data contents of the ROM.

NOTE

The ROM checksum test is performed automatically during power up or at front panel RESET. Memory failure will result in all LEDs staying on until any key is hit.

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'E' A11TP7
3) START to 'ROM1' A11TP13
4) STOP to 'ROM6' A11TP18

Set the signature analyzer's controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN

SERVICE SHEET 16 (Cont'd)

Set up the Signal Generator as follows:

1) Disconnect the attenuator cable from the power supply board to the attenuator.
2) Set the TEST/NRM switch P/O A11S1 to TEST.
3) Set the ROM/NRM switch P/O A11S1 to ROM.

NOTE

ROM signatures will change as firmware changes. Be sure the part number on each ROM corresponds to the part number in Table 2.

Table 2. ROM HP Part Number

ROM Number	HP Part Number
ROM 1	1818-1365
ROM 2	1818-1358
ROM 3	1818-1359
ROM 4	1818-1360
ROM 5	1818-1361
ROM 6	1818-1362

Probe. Connect the probe to the data bus of the ROM to check data contents. Use connector J2 (refer to Service Sheet 14). Verify that each signature is correct and stable as indicated in Table 3.

Table 3. ROM Generated Data Bus Signatures

Node	Correct Signature
+5V	1857
D0	F5F2
D1	1758
D2	2719
D3	F177
D4	7AA2
D5	CA47
D6	U7U2
D7	5F72

An incorrect signature could be due to:

1) improper test setup
2) improper addressing to ROM
3) Bus fight on data bus
4) bad ROM
5) firmware has changed (refer to Table 2).

Recheck the test setup. The D0 to D7 should be set to 1000 0000. If incorrect, be sure the ROM/NRM switch P/O A11S1 is set to ROM (NOP).

SERVICE SHEET 16 (Cont'd)

The Data Bus Buffer should be in the high impedance state, that is, U14-pin 19 should be high.

If testing is complete, set the TEST/NRM switch to NRM and ROM/NRM to NRM.

Test 3. Microprocessor and Individual ROM Functional Checks

Purpose. Verify the functional operation of the Microprocessor and the data contents of the individual ROM.

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'E' A11TP7
3) START to the individual ROM test points (refer to the schematic)
4) STOP to the individual ROM test points (refer to the schematic).

Set the signature analyzer's controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Generator as follows:

1) Disconnect the attenuator cable W17 from the power supply board to the attenuator.
2) Set the TEST/NRM switch P/O A11S1 to TEST.
3) Set the ROM/NRM switch P/O A11S1 to ROM.

NOTE

ROM signatures will change as firmware changes. Be sure the part number on ROM corresponds to part number in Table 2.

Probe. Connect the probe to the data bus of the ROM to check data contents. Use connector J2 (refer to Service Sheet 14). Verify that each signature as indicated in Table 4 is correct and stable.

After the signatures are taken, reset the TEST/NRM switch to NRM and the ROM/NRM switch to NRM. Reconnect the attenuator cable W17 if testing is complete.

Test 4. Microprocessor and RAM Functional Check

Purpose. To verify the ability to write and read to the three RAM. (RAM 3 is located in the Microprocessor U13; refer to Service Sheet 14.)

NOTE

An abbreviated RAM check is performed at power up or reset. Memory failute will result in all front panel LEDs staying lit until any key is pressed.

SERVICE SHEET 16 (Cont'd)

Table 4. Individual ROM Generated Data Bus Signatures

Node	Correct Signature	Comments
+5V	826P	
D0	HC6U	ROM1 U2
D1	F5FC	
D2	FAU1	
D3	C149	
D4	8P66	
D5	P3P4	
D6	17F4	
D7	8FP1	
+5V	826P	
D0	665U	ROM2 U9
D1	8C5H	
D2	2763	
D3	3CA7	
D4	38C1	
D5	9AC0	
D6	3487	
D7	84A2	
+5V	826P	
D0	PP18	ROM3 U8
D1	AH74	
D2	93H6	
D3	A87F	
D4	P428	
D5	5580	
D6	CHFC	
D7	08H9	
+5V	826P	
D0	1C4C	ROM4 U7
D1	14U5	
D2	6389	
D3	7F04	
D4	F1A5	
D5	HAF5	
D6	1F62	
D7	C18U	
+5V	826P	
D0	46C1	ROM5 U6
D1	8831	
D2	U30C	
D3	8UCU	
D4	4221	
D5	3AUP	
D6	AA1P	
D7	2559	
+5V	826P	
D0	HP67	ROM6 U5
D1	FO46	
D2	323A	
D3	3U32	
D4	15FU	
D5	7FP8	
D6	9A4A	
D7	9F1A	

Address Buffering and Decoding
Serial I/O and Control
P/O A11
SERVICE SHEET 15

SERVICE SHEET 16 (Cont'd)

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'E' A11TP7
3) START to 'SA1' A11TP5
4) STOP to 'SA4' A11TP7

Set the signature analyzer's controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN

Set up the Signal Generator as follows:

Disconnect the attenuator cable from the power supply to the attenuator.

Initialize. Briefly short the Microprocessor test point 'NMI' to ground.

NOTES

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect this has probably happened. Restart the test by setting the 'RST/RUN' switch to 'RST'; then back to 'RUN'. Briefly touch the 'NMI' test point to ground.

RAM 2 is only used for storing front panel settings. The Signal Generator should work even if RAM 2 is faulty. Only the store and recall related functions will not operate properly.

Probe. Connect the probe to data lines at J2. Verify that the data transfers as indicated by Table 5 are correct.

An incorrect signature may indicate:

1) improper setup
2) RAM program aborting
3) ROM program is incorrect (+5V signature is incorrect).
4) incorrect addressing to RAM
5) defective RAM.

NOTE

Go to Service Sheet 14 to test the addressing.

Table 5. RAM Data Transfer Signatures

Node	Correct Signature
+5V	C888
D0	3U02
D1	489H
D2	1560
D3	9A3A
D4	58U6
D5	9038
D6	35C7
D7	98HF

1) If the ROM signatures are correct, then the program is correct.
2) If the +5V signature is correct, then the program is running.

Test 5. Microprocessor and Individual RAM Functional Check

Purpose. To test the data transfer of individual RAM.

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'E' A11TP7
3) START to test point as indicated in the table
4) STOP to test point as indicated in the table.

Set the signature analyzer controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN.

Set up the Signal Generator by disconnecting the attenuator cable W17 from the power supply board to the attenuator.

Initialize. Briefly short A11TP3 'NMI' to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the 'RST/RUN' switch to 'RST'; then 'RUN'. Briefly touch the 'NMI' test point to ground.

SERVICE SHEET 16 (Cont'd)

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'E' A11TP7
3) START to 'SA1' A11TP5
4) STOP to 'SA4' A11TP7

Set the signature analyzer's controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN

Set up the Signal Generator as follows:

Disconnect the attenuator cable from the power supply to the attenuator.

Initialize. Briefly short the Microprocessor test point 'NMI' to ground.

NOTES

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect this has probably happened. Restart the test by setting the 'RST/RUN' switch to 'RST'; then back to 'RUN'. Briefly touch the 'NMI' test point to ground.

RAM 2 is only used for storing front panel settings. The Signal Generator should work even if RAM 2 is faulty. Only the store and recall related functions will not operate properly.

Probe. Connect the probe to data lines at J2. Verify that the data transfers as indicated by Table 5 are correct.

An incorrect signature may indicate:

1) improper setup
2) RAM program aborting
3) ROM program is incorrect (+5V signature is incorrect).
4) incorrect addressing to RAM
5) defective RAM.

NOTE

Go to Service Sheet 14 to test the addressing.

Table 5. RAM Data Transfer Signatures

Node	Correct Signature
+5V	C888
D0	3U02
D1	489H
D2	1560
D3	9A3A
D4	58U6
D5	9038
D6	35C7
D7	98HF

1) If the ROM signatures are correct, then the program is correct.
2) If the +5V signature is correct, then the program is running.

Test 5. Microprocessor and Individual RAM Functional Check

Purpose. To test the data transfer of individual RAM.

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'E' A11TP7
3) START to test point as indicated in the table
4) STOP to test point as indicated in the table.

Set the signature analyzer controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN.

Set up the Signal Generator by disconnecting the attenuator cable W17 from the power supply board to the attenuator.

Initialize. Briefly short A11TP3 'NMI' to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the 'RST/RUN' switch to 'RST'; then 'RUN'. Briefly touch the 'NMI' test point to ground.

SERVICE SHEET 16 (Cont'd)

Probe. Connect the probe to the data lines at J2. Verify that the individual RAMdata transfers are correct as indicated in Table 6.

Table 6. Individual RAM Data Transfer Signatures

Node	Correct Signature	Comments
+5V	CU45	RAM1 (U2)
D0	30H4	
D1	C372	STRT- SA.2
D2	5P69	STP - SA.3
D3	A585	
D4	5846	
D5	875F	
D6	CCFC	
D7	HPFU	
+5V	A2FP	RAM2 (U3)
D0	4542	
D1	CU9P	STRT- SA.3
D2	1U1H	STP - SA.4
D3	F6P0	
D4	273C	
D5	AAU1	
D6	P5FA	
D7	669F	
+5V	1217	RAM3(U13
D0	66F4	internal)
D1	356C	STRT- SA.1
D2	6F15	STP - SA.2
D3	0H43	
D4	4PC8	
D5	C2F6	
D6	17HU	
D7	C316	

Reconnect the attenuator cable W17. Reset the Signal Generator by setting the front panel RESET-STBY-ON switch to RESET and back to ON.

P/O A11 ASSEMBLY

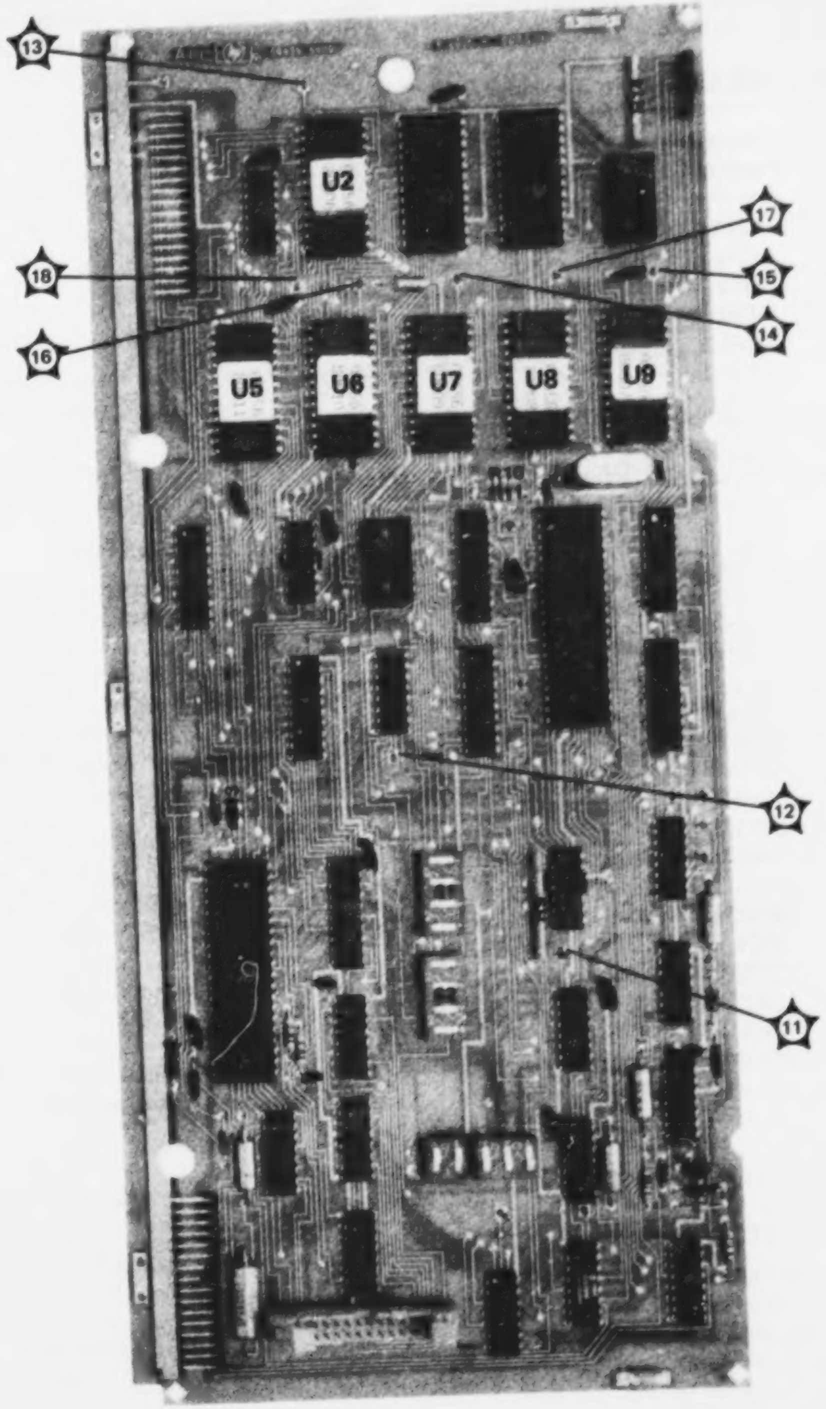

13
U2
17
18
15
16
14
U5
U6
U7
U8
U9
12
11

Figure 8-90. Memory Component Locations

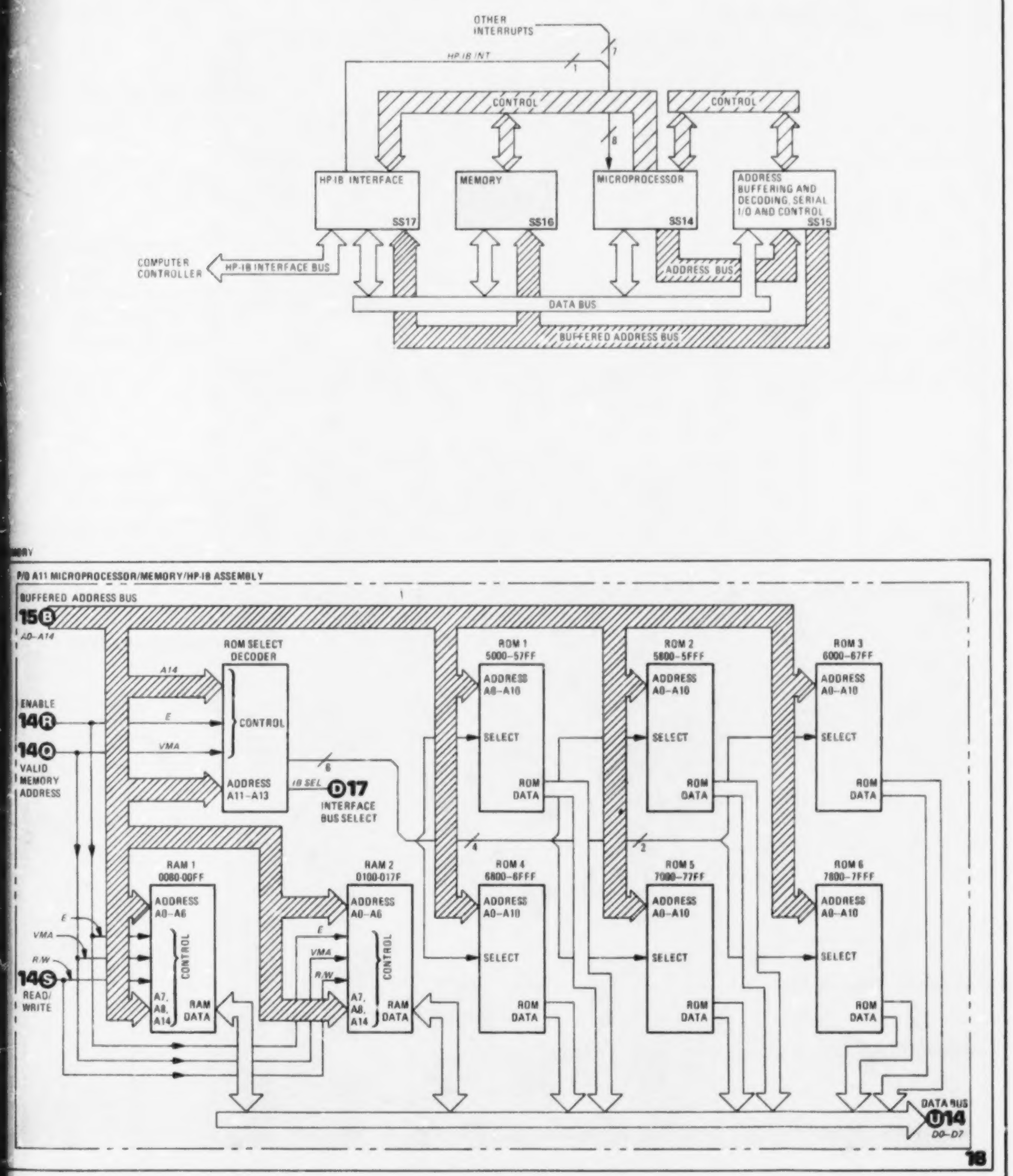
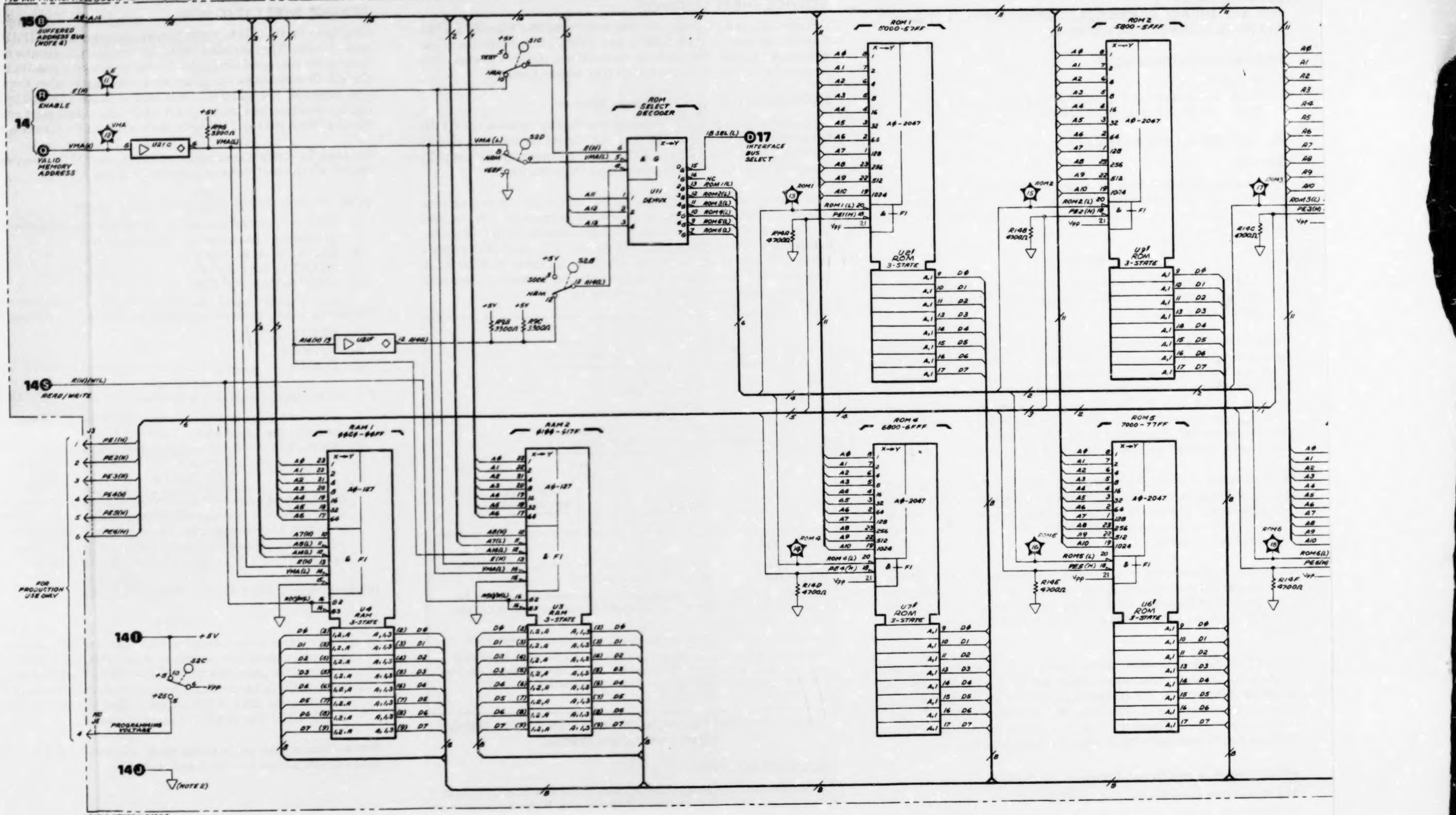

OTHER INTERRUPTS
HP-IB INT
CONTROL
CONTROL
HP-IB INTERFACE
SS17
MEMORY
SS16
MICROPROCESSOR
SS14
ADDRESS BUFFERING AND DECODING, SERIAL I/O AND CONTROL
SS15
COMPUTER CONTROLLER
HP-IB INTERFACE BUS
ADDRESS BUS
DATA BUS
BUFFERED ADDRESS BUS
ORY
P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY
BUFFERED ADDRESS BUS
15B
A0–A14
ENABLE
14R
14Q
VALID MEMORY ADDRESS
14S
READ/WRITE
ROM SELECT DECODER
A14
E
VMA
CONTROL
ADDRESS A11–A13
IB SEL
D17
INTERFACE BUS SELECT
ROM 1 5000–57FF
ROM 2 5800–5FFF
ROM 3 6000–67FF
ROM 4 6800–6FFF
ROM 5 7000–77FF
ROM 6 7800–7FFF
ADDRESS A0–A10
SELECT
ROM DATA
RAM 1 0080-00FF
RAM 2 0100-017F
ADDRESS A0–A6
A7, A8, A14
CONTROL
RAM DATA
E
VMA
R/W
DATA BUS
U14
D0–D7
18

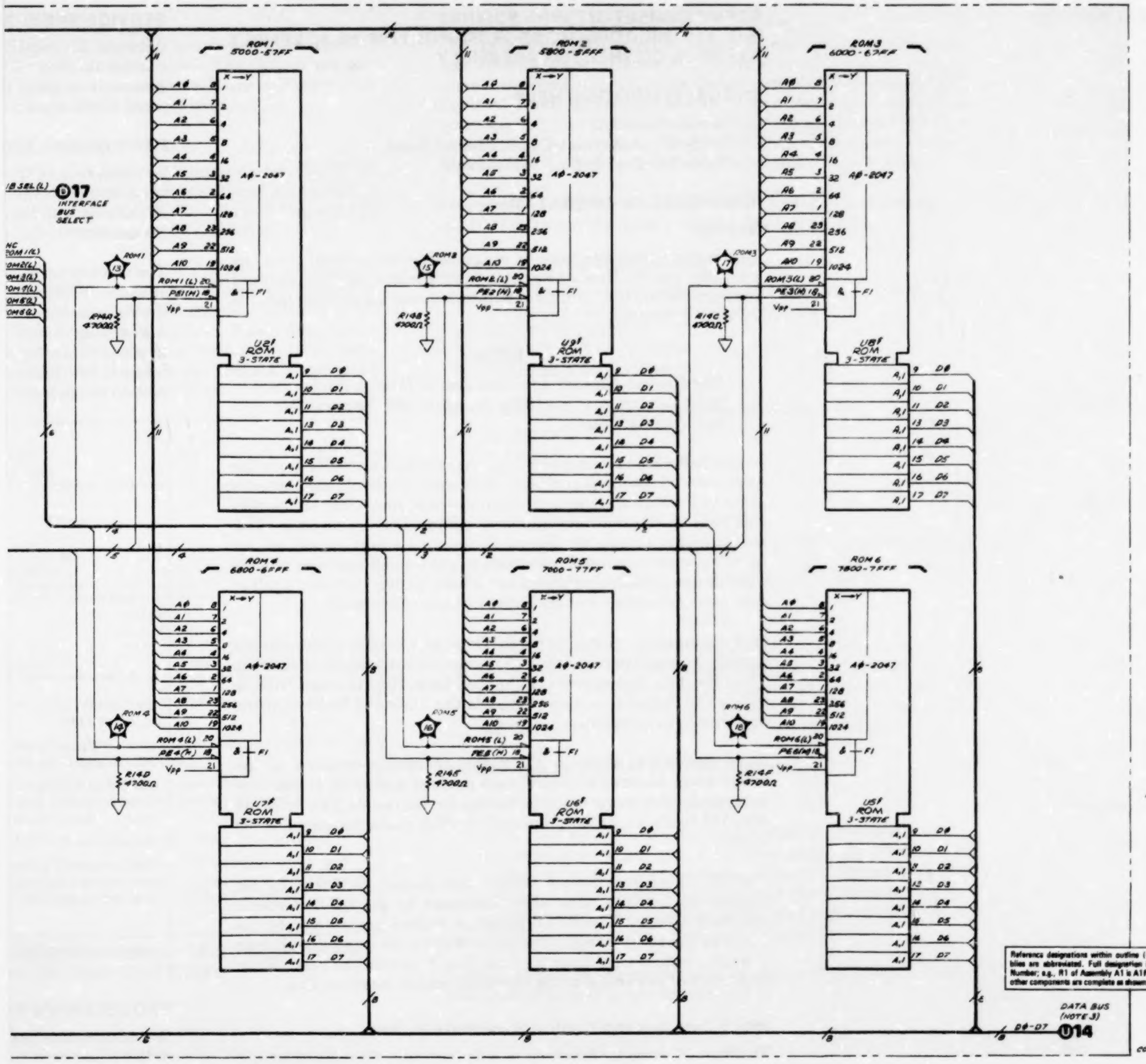
Figure 8-91. Memory Block Diagrams

P/O A11 MICROPR
15B
BUFFERED ADDRESS BU (NOTE 4)
14
R
ENABLE
Q
VMA
VALID MEMORY ADDRESS
14S
R/W
READ/WRIT
1
2
3
4
5
6
FOR PRODUCTION USE ONLY
4

P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY (08656-60007)


15 B
A0-A15
BUFFERED ADDRESS BUS (NOTE 4)
14
R
ENABLE
E(H)
Q
VALID MEMORY ADDRESS
VMA(H)
VMA
U21C
R96 3300Ω
+5V
VMA(L)
S1C
TEST
NRM
S2D
VERF
ROM SELECT DECODER
U11 DEMUX
A11
A12
A13
IB SEL(L)
D17
INTERFACE BUS SELECT
NC
ROM1(L)
ROM2(L)
ROM3(L)
ROM4(L)
ROM5(L)
ROM6(L)
S2B
500E
A14(L)
R9B 3300Ω
R9C 3300Ω
U21F
A14(H)
14 S
READ/WRITE
R(H)/W(L)
J3
PE1(H)
PE2(H)
PE3(H)
PE4(H)
PE5(H)
PE6(H)
FOR PRODUCTION USE ONLY
RAM 1
RAM 2
U4 RAM 3-STATE
U3 RAM 3-STATE
A0-127
S2C
+5V
+25
-VPP
W1 J5
PROGRAMMING VOLTAGE
14 I
14 J
(NOTE 2)
ROM 1 5000-57FF
ROM 2 5800-5FFF
ROM 4 6800-6FFF
ROM 5 7000-77FF
ROM 6
ROM 3
A0-2047
U21 ROM 3-STATE
U9 ROM 3-STATE
U7 ROM 3-STATE
U6 ROM 3-STATE
R14A 4700Ω
R14B 4700Ω
R14C 4700Ω
R14D 4700Ω
R14E 4700Ω
R14F 4700Ω
VPP
D0
D1
D2
D3
D4
D5
D6
D7

8656A MEMORY: 2082A


ROM1 5000-57FF
ROM2 5800-5FFF
ROM3 6000-67FF
ROM4 6800-6FFF
ROM5 7000-77FF
ROM6 7800-7FFF
U2 ROM 3-STATE
U9 ROM 3-STATE
U8 ROM 3-STATE
U7 ROM 3-STATE
U6 ROM 3-STATE
U5 ROM 3-STATE
A0-2047
X→Y
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
ROM1(L)
PE1(H)
ROM2(L)
PE2(H)
ROM3(L)
PE3(H)
ROM4(L)
PE4(H)
ROM5(L)
PE5(H)
ROM6(L)
PE6(H)
Vpp
& F1
R14A 4700Ω
R14B 4700Ω
R14C 4700Ω
R14D 4700Ω
R14E 4700Ω
R14F 4700Ω
IBSEL(L)
17 INTERFACE BUS SELECT
NC
ROM1(L)
ROM2(L)
ROM3(L)
ROM4(L)
ROM5(L)
ROM6(L)
D0
D1
D2
D3
D4
D5
D6
D7
DATA BUS (NOTE 3)
D0-D7
14

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A11J5-1 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. DATA IS TRANSFERRED POSITIVE TRUE FROM ROM OR RAM MEMORY TO THE MICROPROCESSOR ON THE DATA BUS (D0-D7).
4. ADDRESS DATA IS TRANSFERRED POSITVE TRUE FROM THE MICROPROCESSOR ON THE BUFFERED ADDRESS BUS (A0-A14).

INDICATES CIRCUIT CHANGE. SEE SECTION VII.

REFERENCE DESIGNATIONS

A11
J3, 5 R9, 14 S1, 2 TP11-18 U2-9, 11, 21

LOGIC LEVELS

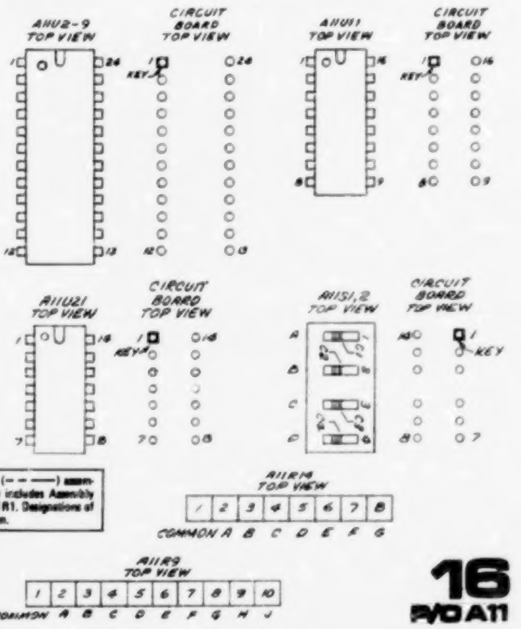
	TTL
HIGH	> 2V
LOW	< 0.8V
< IS MORE NEG. THAN	
> IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U2	1818-1368
U3, 4	1818-0701
U5	1818-1362
U6	1818-1361
U7	1818-1360
U8	1818-1359
U9	1818-1358
U11	1820-1240
U21	1820-1200

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2, 5-9	+5V - 24 ▽ - 12
U3, 4	+5V - 24 ▽ - 1
U11	+5V - 16 ▽ - 8
U21	+5V - 14 ▽ - 7


A11U2-9 TOP VIEW
CIRCUIT BOARD TOP VIEW
A11U11 TOP VIEW
CIRCUIT BOARD TOP VIEW
A11U21 TOP VIEW
CIRCUIT BOARD TOP VIEW
A11S1,2 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY
A11R14 TOP VIEW
1 2 3 4 5 6 7 8
COMMON A B C D E F G
A11R9 TOP VIEW
1 2 3 4 5 6 7 8 9 10
COMMON A B C D E F G H J

16
A11

Figure 8-92. Memory Schematic Diagram

SERVICE SHEET 17
P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY
A13 HP-IB CONNECTOR ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

This Signal Generator may be connected to an external computer controller via the Hewlett-Packard Interface Bus (HP-IB). Encoded data and control information is passed between the two instruments on the interface bus.

NOTE

The Hewlett-Packard Interface Bus is Hewlett-Packard's implementation of the IEEE Standard 488 "General Purpose Interface Bus".

Inputs to the Signal Generator from the external controller are in the form of encoded control and data information. Control information is input to the Signal Generator via five control lines (four are used in this instrument) and three handshake lines. The control lines allow the controller to gain the Signal Generator's attention and impart other appropriate control information. The handshake lines provide asynchronous control information for data transfer between a talker (computer controller) and the listener (Signal Generator).

In the handshake mode, the Signal Generator first indicates when it is ready to listen (receive data). The controller responds by indicating when the data that appears on the data lines, DI01 through DI08, is valid. The Signal Generator then lets the controller know that the data has been accepted.

Data that is transferred to the Signal Generator contains all the information required to control each mode of operation. It also contains the level or frequency information for each mode. Examples are 50% AM depth, an RF amplitude of -10 dBm and a frequency of 100 MHz.

The HP-IB Address Switch Buffer U20 places the internally set address on the data lines when addressed by the HP-IB General Interface Adapter. The HP-IB Interface Buffers are enabled by the interface bus select IB SEL. The Read/Write mode determines if data is written onto or read from the Data Bus. Note that the Read/Write lines are tied in parallel to the Hewlett-Packard Interface Bus.

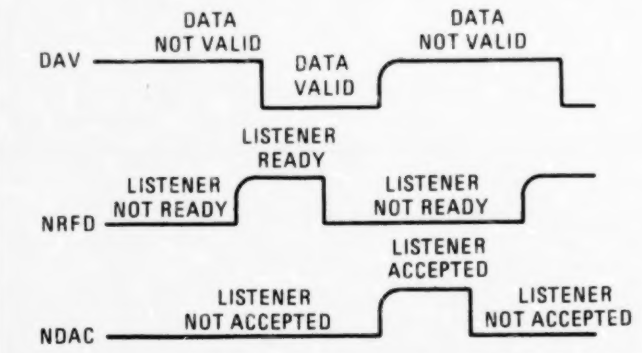
HP-IB Data Bus and Control/Handshake Buffers

The Signal Generator functions as a listener only, therefore there are no input connections to the Data Bus Buffers from the Data Bus. Also, there are no connections to and from the service request line SRQ (U19-pin 23 and U27-pin 15). The only outgoing signals are the handshake control lines NRFD and NDAC. The buffers are permanently enabled by hardwire connections. Refer to Figure 1 for more information about the HP-IB Handshake Control.

HP-IB General Purpose Interface Adapter

The interface adapter U19 provides interfacing between the HP-IB connections to the controller and the Signal Generator's digital circuits. The address select ASE and HP-IB Interrupt Request IBI are generated as a result of inputs from the controller.

The Microprocessor, under the control of the HP-IB subroutines stored in ROM, outputs control and address signals to U19 to control the data input from the controller. IB SEL selects the HP-IB mode. Addressing is input to U19 on A0, A1 and A2. Read/Write determines if data is written onto the data lines D0 through D7 or if the internal address is read by U19. The internal address is compared with that input to the Signal Generator by U19.



Start with the talker waiting for the listener to release NRFD (not ready for data) indicating it is ready.

When the listener is ready, NRFD goes high (false). The talker then places valid data on DI01 through DI08 and sets DAV (data valid) low (true).

NRFD then goes low (true) and the talker waits for the listener to indicate it has accepted the data (or ignored it) by releasing the NDAC (not data accepted) to a high (false, i.e., data is accepted).

The talker sets DAV high (false) and again waits for the listener to release NRFD.

(NOTE that if ATN is true, all instruments on the bus must handshake regardless of whether they are talkers, listeners, or bystanders. Being in remote or local has nothing to do with handshaking. If ATN is false, they only handshake if addressed).

Figure 1. Simplified HP-IB Handshake between a Talker (Computer Controller) and One Listener (Signal Generator)

TROUBLESHOOTING

Troubleshooting is done on the circuits of Service Sheet 17 when a defect seems to be related to the HP-IB circuits. If the signatures are all correct, the instrument interface circuits from U19 to the Microprocessor are probably functional. Refer to the HP-IB Functional Checks in Section III to verify proper operation of the HP-IB interface circuits. This includes data, control and handshake connections to the computer controller. Do not overlook the possibility that the HP-IB address switches are set to an address other than what was expected. The address switch setting may be checked by pressing the front panel switch HP-IB ADRS. As a last resort return to Service Sheet BD4 and consider the other possibilities shown.

Purpose. To verify transmission of data from the Microprocessor to the HP-IB General Purpose Interface Adapter A11U19.

Setup. Connect the signature analyzer as follows:

1) GND as close as possible to the circuitry being probed. (Bad grounding can cause unstable signatures.)
2) CLK to 'E' A11TP11
3) START to 'SA1' A11TP5
4) STOP to 'SA2' A11TP6

Set the signature analyzer's controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN

Set up the Signal Generator as follows:

1) Disconnect the attenuator cable W17 from the power supply board to the attenuator.
2) Set the LOGIC/RAM switch P/O A11S1 to LOGIC.

NOTE

If the Signal Generator's address switch has been set to other than '07', the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON.

Initialize. Briefly short A11TP3 'NMI' to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the the test by setting the 'RST/RUN' switch to 'RST and then 'RUN'. Briefly touch the 'NMI' test point to ground.

Probe. Connect the probe to the node indicated in Table 1. Verify that each signature is correct and stable.

n of the HP-IB inter-
handshake connec-
k the possibility that
ess other than what
be checked by press-
last resort return to
ibilities shown.

he Microprocessor to
A11U19.

ws:

being probed. (Bad
s.)

s:

m the power supply

to LOGIC.

has been set to
this test will be
vitches to A1=1,
the front panel
back to ON.

d.

he Microproces-
n that portion
5V signature is
start the the test
and then 'RUN'.
nd.

ed in Table 1. Verify

SERVICE SHEET 17 (Cont'd)

Table 1. Interface Signatures

Node	Correct Signature
+5V	H6H5
U15 #19	39A7
U19 #4	6514
U19 #7	69F8
U19 #8	0444
U19 #9	36A9
U19 #10	FF2C
U19 #11	U939
U19 #12	P71U
U19 #13	FH9F
U19 #14	652F

Reconnect attenuator cable W17. Reset the LOGIC/RAM switch to the RAM position.

NOTE

If the HP-IB address switch was changed, reset the address switch to the original address. Set the front panel RESET-STBY-ON switch to RESET and back to ON.

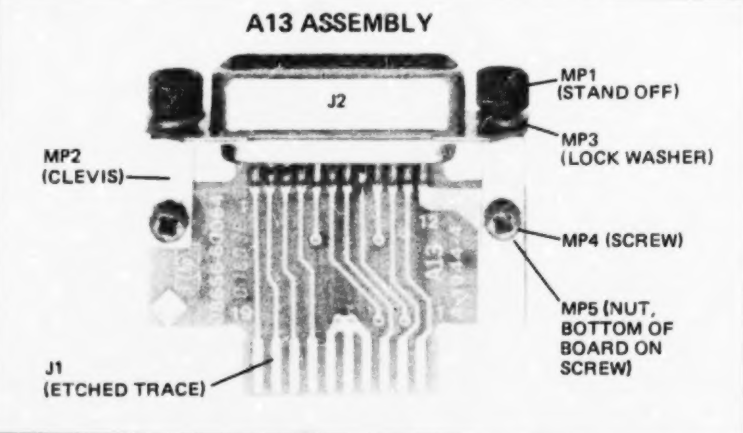

A13 ASSEMBLY
J2
MP1 (STAND OFF)
MP3 (LOCK WASHER)
MP2 (CLEVIS)
MP4 (SCREW)
MP5 (NUT, BOTTOM OF BOARD ON SCREW)
J1 (ETCHED TRACE)

Figure 8-93. HP-IB Connector Component Locations

Memory P/O A11 SERVICE SHEET 16

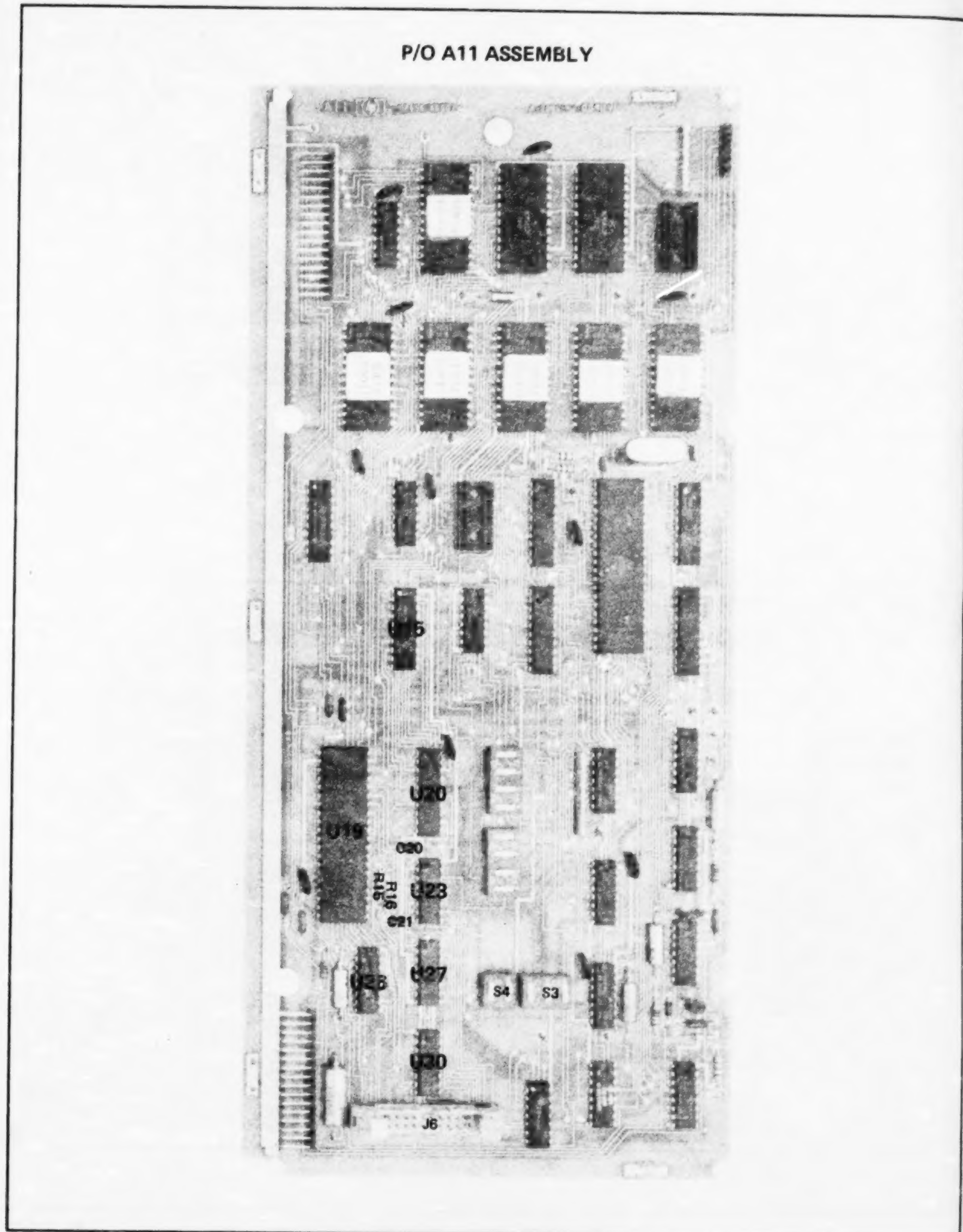

P/O A11 ASSEMBLY
U15
U20
U19
C20
R16
R15
U23
C21
U26
U27
S4
S3
U30
J6

Figure 8-94. HP-IB Interface Component Locations

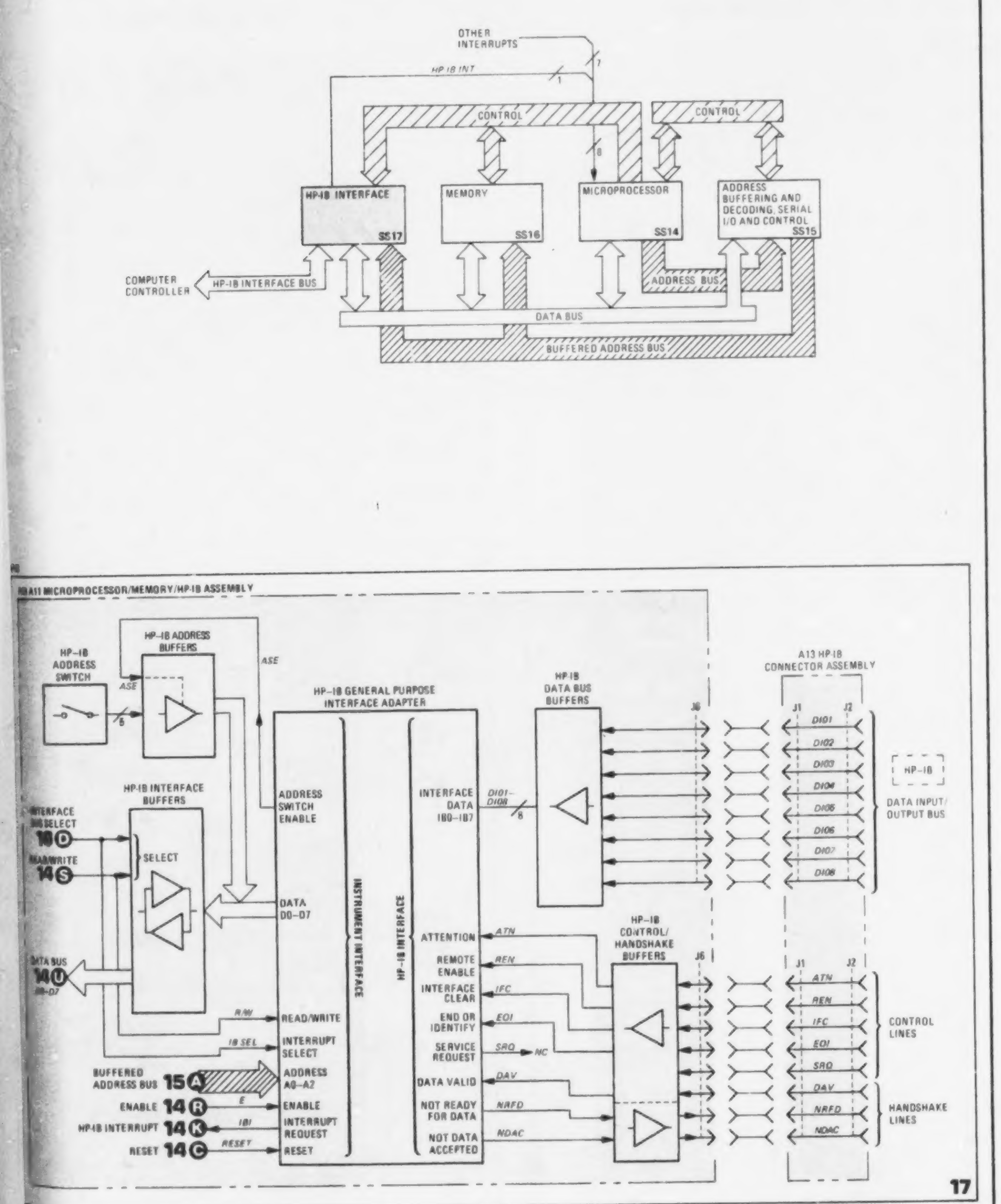
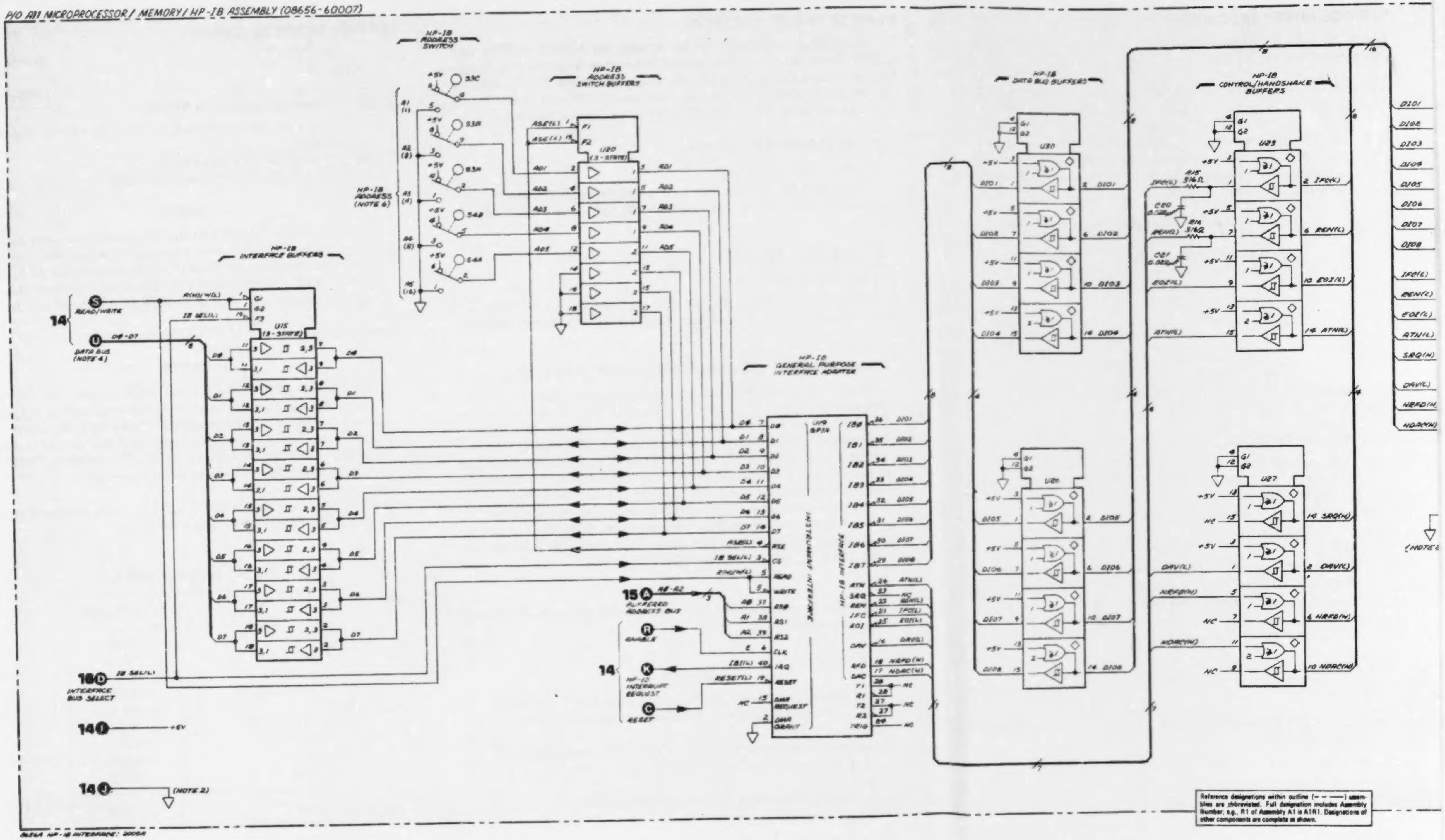

OTHER INTERRUPTS
HP-IB INT
1
1
CONTROL
8
CONTROL
HP-IB INTERFACE SS17
MEMORY SS16
MICROPROCESSOR SS14
ADDRESS BUFFERING AND DECODING, SERIAL I/O AND CONTROL SS15
COMPUTER CONTROLLER
HP-IB INTERFACE BUS
ADDRESS BUS
DATA BUS
BUFFERED ADDRESS BUS
P/O A11 MICROPROCESSOR/MEMORY/HP-IB ASSEMBLY
HP-IB ADDRESS SWITCH
HP-IB ADDRESS BUFFERS
ASE
5
ASE
HP-IB GENERAL PURPOSE INTERFACE ADAPTER
HP-IB INTERFACE BUFFERS
INTERFACE BUS SELECT 18 D
READ/WRITE 14 S
SELECT
DATA BUS 14 U IB0-D7
R/W
IB SEL
BUFFERED ADDRESS BUS 15 A
ENABLE 14 R
HP-IB INTERRUPT 14 K
RESET 14 C
E
IBI
RESET
ADDRESS SWITCH ENABLE
DATA D0-D7
READ/WRITE
INTERRUPT SELECT
ADDRESS A0-A2
ENABLE
INTERRUPT REQUEST
RESET
INSTRUMENT INTERFACE
HP-IB INTERFACE
INTERFACE DATA IB0-IB7
ATTENTION
REMOTE ENABLE
INTERFACE CLEAR
END OR IDENTIFY
SERVICE REQUEST
DATA VALID
NOT READY FOR DATA
NOT DATA ACCEPTED
DIO1-DIO8
8
ATN
REN
IFC
EOI
SRQ
NC
DAV
NRFD
NDAC
HP-IB DATA BUS BUFFERS
HP-IB CONTROL/HANDSHAKE BUFFERS
J6
J6
A13 HP-IB CONNECTOR ASSEMBLY
J1
J2
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
HP-IB
DATA INPUT/OUTPUT BUS
J1
J2
ATN
REN
IFC
EOI
SRQ
DAV
NRFD
NDAC
CONTROL LINES
HANDSHAKE LINES
17

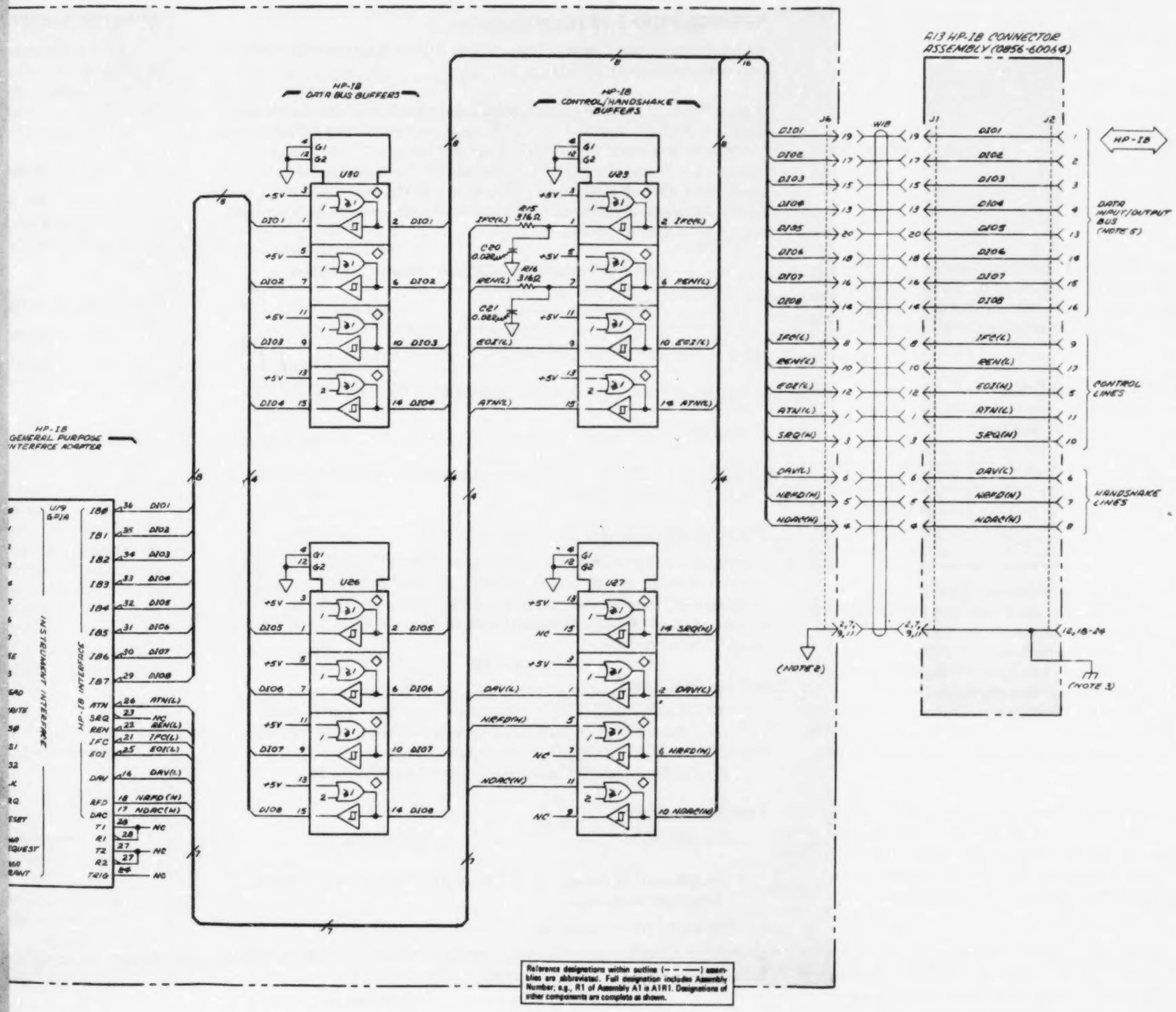
Figure 8-95. HP-IB Interface Block Diagrams

P/O A11 MICROPROC
14
S
U
18 D
14 U
14


P/O A11 MICROPROCESSOR / MEMORY / HP-IB ASSEMBLY (08656-60007)
HP-IB ADDRESS SWITCH
HP-IB ADDRESS SWITCH BUFFERS
U20 (3-STATE)
HP-IB INTERFACE BUFFERS
U15 (3-STATE)
HP-IB GENERAL PURPOSE INTERFACE ADAPTER
U19 GP14
INSTRUMENT INTERFACE
HP-IB INTERFACE
HP-IB DATA BUS BUFFERS
U30
U26
HP-IB CONTROL/HANDSHAKE BUFFERS
U23
U27
HP-IB ADDRESS (NOTE 6)
14
READ/WRITE
DATA BUS (NOTE 4)
D0-D7
16 INTERFACE BUS SELECT
IB SEL(L)
14 +5V
14 (NOTE 2)
15 BUFFERED ADDRESS BUS
A0-A2
ENABLE
14 HP-IB INTERRUPT REQUEST
RESET
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
IFC(L)
REN(L)
EOI(L)
ATN(L)
SRQ(H)
DAV(L)
NRFD(H)
NDAC(H)
R15 316Ω
R16 316Ω
C20 0.022μF
C21 0.022μF
(NOTE

Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

8656A HP-IB INTERFACE: 2005A


HP-IB DATA BUS BUFFERS
HP-IB CONTROL/HANDSHAKE BUFFERS
HP-IB GENERAL PURPOSE INTERFACE ADAPTER
U19 GPIA
INSTRUMENT INTERFACE
HP-IB INTERFACE
U30
U23
U26
U27
R15 316Ω
R16 316Ω
C20 0.022µF
C21 0.022µF
+5V
G1
G2
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
IFC(L)
REN(L)
EOI(L)
ATN(L)
SRQ(H)
DAV(L)
NRFD(H)
NDAC(H)
NC
J6
W18
J1
J2
A13 HP-IB CONNECTOR ASSEMBLY (0856-60064)
HP-IB
DATA INPUT/OUTPUT BUS (NOTE 5)
CONTROL LINES
HANDSHAKE LINES
EOI(H)
(NOTE 2)
(NOTE 3)
12,18-24

Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. A11 CHASSIS GROUND IS ACHIEVED THROUGH A11 J5-1 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. A13 CHASSIS GROUND IS ACHIEVED THROUGH A13 J2-12 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
4. DATA TRANSFERRED ON THE DATA BUS (D0 TO D7) IS POSITIVE TRUE.
5. DATA TRANSFERRED ON THE DATA INPUT/OUTPUT BUS (DIO1-DIO8) IS NEGATIVE TRUE.
6. HP-IB ADDRESSES GREATER THAN 30 ARE INVALID.

REFERENCE DESIGNATIONS

NO PREFIX	A13
W18	J1, 2
A11	
C20, 21 J4 R15, 16 S3, 4 U15, 19, 20, 23, 26, 27, 30	

LOGIC LEVELS

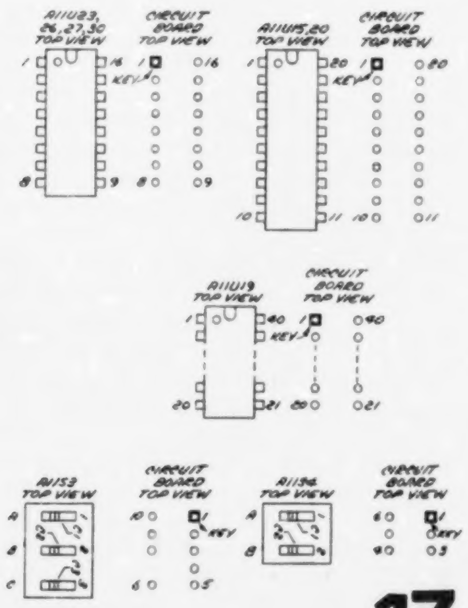
	TTL
HIGH	>2V
LOW	<0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PIN NUMBERS
A11	
U15, 20	+5V - 20 ▽ - 10
U19	+5V - 20 ▽ - 1
U23, 26 27, 30	+5V - 16 ▽ - 8

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PART NUMBERS
A11	
U15	1820-2075
U19	1820-2219
U20	1820-1759
U23, 26, 27, 30	1820-1689


A11U23, 26, 27, 30 TOP VIEW
CIRCUIT BOARD TOP VIEW
A11U15, 20 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY
A11U19 TOP VIEW
CIRCUIT BOARD TOP VIEW
A11S3 TOP VIEW
A11S4 TOP VIEW
A
B
C

17
P/O A11, A13

Figure 8-96. HP-IB Interface Schematic Diagram

SERVICE SHEET 18
A1 KEYBOARD ASSEMBLY
P/O A2 DISPLAY ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

Keyboard Encoding (A1 and A2)

The Keyboard Assembly (A1) is composed of forty-eight pushbuttons or keys. They are hard-wired in an eight row by six column matrix. With none of the keys pressed, the eight row lines will be pulled high (+5V) through a 1 kΩ resistor and the six column lines will be pulled low (0V) through a 10 kΩ resistor. The resultant keyboard data is shown in Table 1.

Table 1. Keyboard Data (KDA) With No Keys Pressed

Column Data								Row Data							
15*	14*	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
* Bits 14 and 15 are tied low.															

Whenever a key is pressed, a row line is connected to a column line through the dividing network of the 1 kΩ and 10 kΩ resistors which are located on the Display Assembly (A2). As long as the key remains pressed, the column line will remain high and the keyboard interrupt will remain issued to the Microprocessor by the Keyboard Interrupt Generator U19. U19 is hard-wired to function as a 6-input NOR gate because its three control lines (pins 11, 12, and 15) are tied low. Also, its output (pin 1) is always enabled because its enable line (pin 2) is tied high. Therefore, whenever a key is pressed, the control line associated with it will be pulled high as previously mentioned. This high will be sensed by U19 which in turn transfers a low to interrupt the Microprocessor (refer to Service Sheet 14).

When the Microprocessor is interrupted, it enters its keyboard read subroutine. A 5 μs keyboard strobe (KSTB1) is decoded (refer to Service Sheet 19) to strobe the column data into the Key Column Data Latch/Shift Register U18. The column data will consist of seven low bits (the two most-significant bits are hard-wired low) and one high bit. The high bit will be in the bit position that is associated with the column position in which the key was pressed.

Once the column data is latched, the Microprocessor issues a Read Key Row Data (RKRD) signal (refer to Service Sheet 21). This signal is inverted by U22G and applied to the six inputs of the Key Row Data Read Pull-Down U20 to force all six column lines low so that the row data can be read. When the column lines are all forced low, the row line associated with the pressed key will also be forced low. Forcing the column lines low will also disable the keyboard interrupt. Next, another 5 μs keyboard strobe (KSTB2) is decoded (refer to Service Sheet 19) to strobe the row data into the Key Row Data Latch/Shift Register U3. The row data will consist of seven high bits and one low bit. The low bit will be in the bit position that is associated with the row position in which the key was pressed. Once the row data is latched, the Microprocessor will clear RKRD.

A parallel-to-serial conversion takes place as the 16 bits of keyboard data are shifted from U3 and U18. As each row bit is shifted out of U3 (pin 9), a column bit is shifted out of U18 (pin 9) into U3 (pin 10). Sixteen keyboard clocks (KCL) later, all 16 bits of keyboard data will have been shifted to the Microprocessor. If the FREQUENCY key had been pressed, the resultant keyboard data sent to the Microprocessor would be as shown in Table 2.

Table 2. Keyboard Data (KDA) With Frequency Key Pressed

Column Data								Row Data							
15*	14*	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	1	0	1	1	1	1	1	1
* Bits 14 and 15 are tied low.															

Capacitors C1 through C10 are used to filter the +5V supply to the Display Assembly circuitry.

TROUBLESHOOTING

Troubleshooting is done on the circuits of Service Sheet 18 when a malfunction seems to have occurred on the keyboard or display. Perform the Troubleshooting Using Signature Analysis on Service Sheets 14, 15, and 16 before attempting to troubleshoot these circuits using this procedure.

NOTE

This troubleshooting information is to be used instead of Troubleshooting Using Signature Analysis for Signal Generators with serial number prefixes 2009A, 2014A and 2018A. If preferred, this information may be used for all Signal Generators regardless of serial number prefix.

Test Equipment

Oscilloscope ....HP 1222A

√1 Keyboard Interrupt and Serial Keyboard Data Output to Microprocessor

1. Press any front panel key.
2. Verify that a negative going pulse of about 5 volts occurs at A2TP10 each time a key is pressed.
3. Verify that at least one pulse train about 16-bits long occurs at A2TP9.

√2 Control Inputs from Microprocessor

1. Press any front panel key.
2. Verify that a series of keyboard clock pulses appear on A2TP7.

3. Verify that keyboard strobes appear on A2TP5, A2TP6 ar A2TP8. Note that the signal on A2TP5 comes from the Amplitu Annunciator Latch A2U42 (shown on Service Sheet 21). The strob for A2U42 as well as the strobes seen on A2TP6 and A2TP8 com from the strobe decoders A2U25 (shown on Service Sheet 19).

√3 Key Column Data Lines

1. Press a front panel key.
2. Verify that the column data line which includes the pressed ke is a positive-going pulse. The other column data lines should remai low.

√4 Key Row Data Lines

1. Press a front panel key.
2. Verify that the row data line that includes the pressed key is negative-going pulse. The other row data lines should remain high

TROUBLESHOOTING USING SIGNATURE ANALYSIS

Troubleshooting is done on the circuits of Service Sheet 18 when a defect seems to be related to the keyboard. If nothing definite is discovered in performing the signature analysis on this service sheet, consider the other possibilities shown on Service Sheet BD4. Remember that the serial data from the keyboard encoding circuits does pass through the data bus buffers on the way to the Microprocessor (refer to Service Sheet 14). Also, several of the strobes, clocks and control signals are decoded on the circuits of Service Sheet 15. The Load Keyboard Data Strobes are decoded on the circuits of Service Sheet 19. The Read Key Row Data Strobe is latched into A2U42 and is shown on Service Sheet 21.

Purpose. Verify transmission of encoded addresses from Keyboard to Microprocessor.

NOTES

The signatures shown on this service sheet are not valid for instruments with serial prefixes 2018A and below.

Refer to the paragraph entitled REPAIR in this section for front panel keyboard disassembly instructions.

Setup. Connect the signature analyzer as follows:

1) GND to 'GND' A11TP2
2) CLK to 'SA4' A11TP7
3) START to 'SA5' A11TP9
4) STOP to 'SA5' A11TP9

Set the signature anayzer's controls as follows:

1) START-IN

18 (Cont'd)

yboard strobes appear on A2TP5, A2TP6 and he signal on A2TP5 comes from the Amplitude A2U42 (shown on Service Sheet 21). The strobes as the strobes seen on A2TP6 and A2TP8 come oders A2U25 (shown on Service Sheet 19).

n Data Lines

nel key.

column data line which includes the pressed key ulse. The other column data lines should remain

ta Lines

nel key.

row data line that includes the pressed key is a e. The other row data lines should remain high.

'ING USING SIGNATURE ANALYSIS

done on the circuits of Service Sheet 18 when a related to the keyboard. If nothing definite is rming the signature analysis on this service other possibilities shown on Service Sheet BD4. serial data from the keyboard encoding circuits he data bus buffers on the way to the Micropro- ice Sheet 14). Also, several of the strobes, clocks are decoded on the circuits of Service Sheet 15. d Data Strobes are decoded on the circuits of 'he Read Key Row Data Strobe is latched into n on Service Sheet 21.

nsmission of encoded addresses from Keyboard

NOTES

shown on this service sheet are not valid s with serial prefixes 2018A and below.

agraph entitled REPAIR in this section for board disassembly instructions.

signature analyzer as follows:

' A11TP2
A11TP7
5' A11TP9
' A11TP9

ayzer's controls as follows:

SERVICE SHEET 18 (Cont'd)

2) STOP-OUT
3) CLK-IN

Set up the Signal Generator as follows:

1) Set the LOGIC/RAM switch P/O A11S1 to the LOGIC position.
2) Short A2TP14 'T02' to ground.
3) Connect 'SA6' A11TP10 to 'SA7' A2TP1.

NOTE

If the Signal Generator's address switch has been set to other than '07', the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET/STBY/ON switch to RESET and back to ON.

Initialize. Briefly short A11TP3 'NMI' to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting 'RST/RUN' switch to 'RST' and then 'RUN'. Briefly touch the 'NMI' test point to ground.

Probe. Connect the probe to 'KDA' A2TP9. Verify that each signature as indicated in Table 3 is correct and stable.

Table 3. Keyboard Signatures

Key	Correct Signature
+5V	F84P
NO KEY	3FUA
LOCAL	1F38
HP-IB ADRS	89P3
EXT	0802
INT 400 Hz	4P01
INT 1 kHz	560H
OFF	363U
AM	35UF
AM UP	C9UA
AM DOWN	A2CA
FM	68U5
FM UP	2PU6
FM DOWN	F24H
FREQUENCY	550C
COARSE TUNE	H90H
FINE TUNE	56F8

SERVICE SHEET 18 (Cont'd)

Table 3. Keyboard Signatures (Cont'd)

Key	Correct Signature
FREQ UP	36UA
FREQ DOWN	P914
AMPTD	A91A
AMP UP	PU19
AMP DOWN	U715
INCR SET	9727
7	94P4
4	18P2
1	28UC
0	03A2
8	2AF5
5	6FF6
2	74FA
NO KEY	3FUA
.	14U8
9	173C
6	9C3H
3	AC24
-	807H
MHz	2H7A
KHz	6C79
NO KEY	3FUA
%	7375
–	1347
dBm	1084
dBf	9F82
dB	AF9C
EMF	87F2
V	2205
NO KEY	3FUA
mV	6406
μV	7F0A
SEQ	1UUC
STORE	93UH
RECALL	A3P4
DISPLAY	88CH

Remove the jumpers between A2TP '02' and ground and between A2TP1 'SA7' and A11TP10 'SA6'.

Reset the LOGIC/RAM switch P/O A11S1 to the RAM position.

NOTE

If the HP-IB address switch was changed, reset the address switch (Service Sheet 17) to the original address. Set the front panel RESET-STBY-ON switch to RESET and back to ON.

HP-IB Interface
P/O A11, A13
SERVICE SHEET 17

Fig

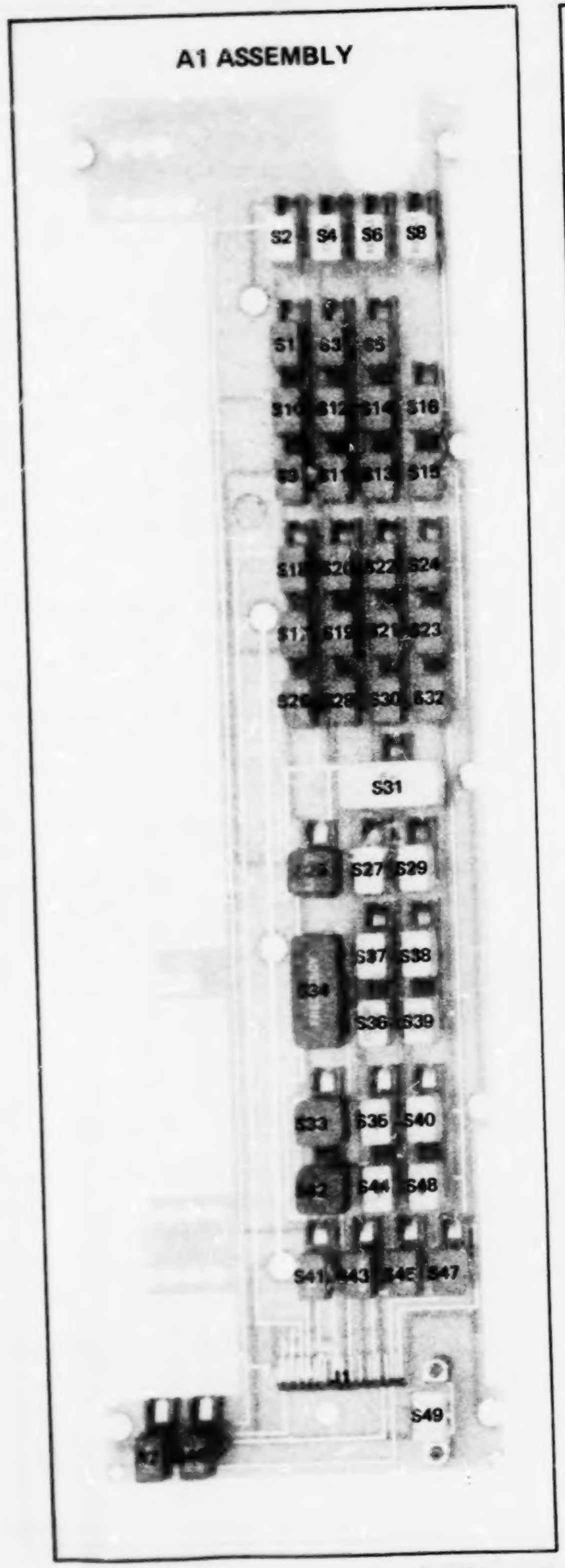

A1 ASSEMBLY
S2
S4
S6
S8
S1
S3
S5
S10
S12
S14
S16
S9
S11
S13
S15
S18
S20
S22
S24
S17
S19
S21
S23
S26
S28
S30
S32
S31
S25
S27
S29
S34
S37
S38
S36
S39
S33
S35
S40
S42
S44
S48
S41
S43
S46
S47
J1
S49

Figure 8-97. Keyboard Component Locations

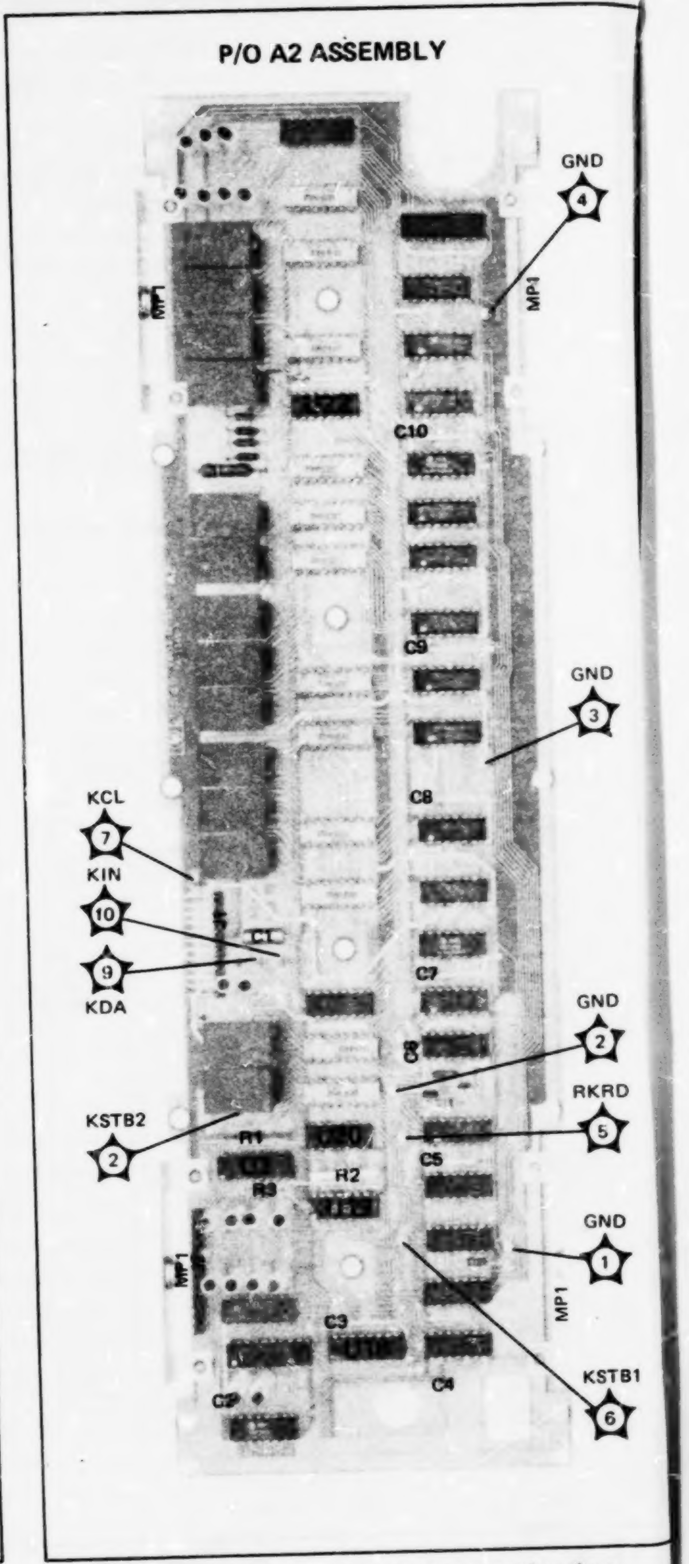
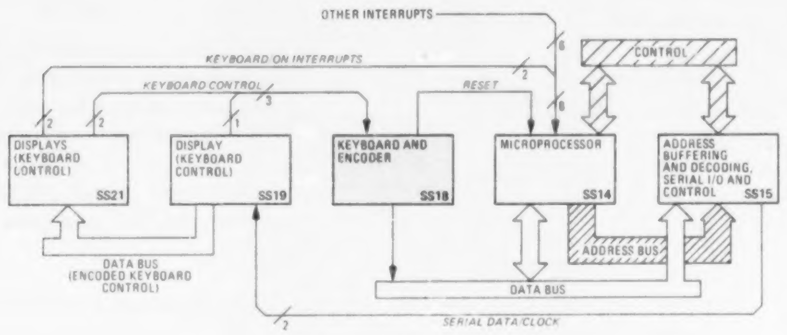

P/O A2 ASSEMBLY
GND
4
MP1
C10
C9
GND
3
C8
KCL
7
KIN
10
C1
9
KDA
C7
GND
2
C6
RKRD
5
KSTB2
2
R1
R3
R2
C5
GND
1
MP1
MP1
C3
C4
C2
KSTB1
6

Figure 8-98. Keyboard Encoder Component Locations


OTHER INTERRUPTS
KEYBOARD ON INTERRUPTS
KEYBOARD CONTROL
RESET
CONTROL
DISPLAYS (KEYBOARD CONTROL) SS21
DISPLAY (KEYBOARD CONTROL) SS19
KEYBOARD AND ENCODER SS18
MICROPROCESSOR SS14
ADDRESS BUFFERING AND DECODING, SERIAL I/O AND CONTROL SS15
DATA BUS (ENCODED KEYBOARD CONTROL)
ADDRESS BUS
DATA BUS
SERIAL DATA/CLOCK
2
3
1
8
6

YBOARD AND ENCODING

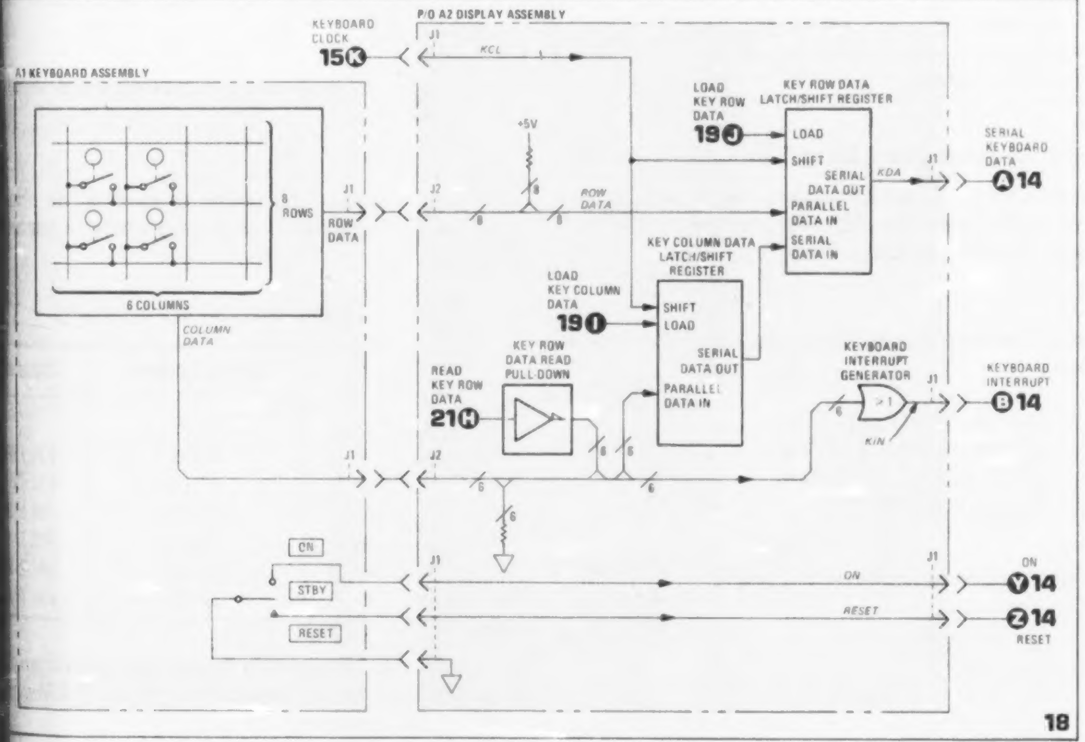
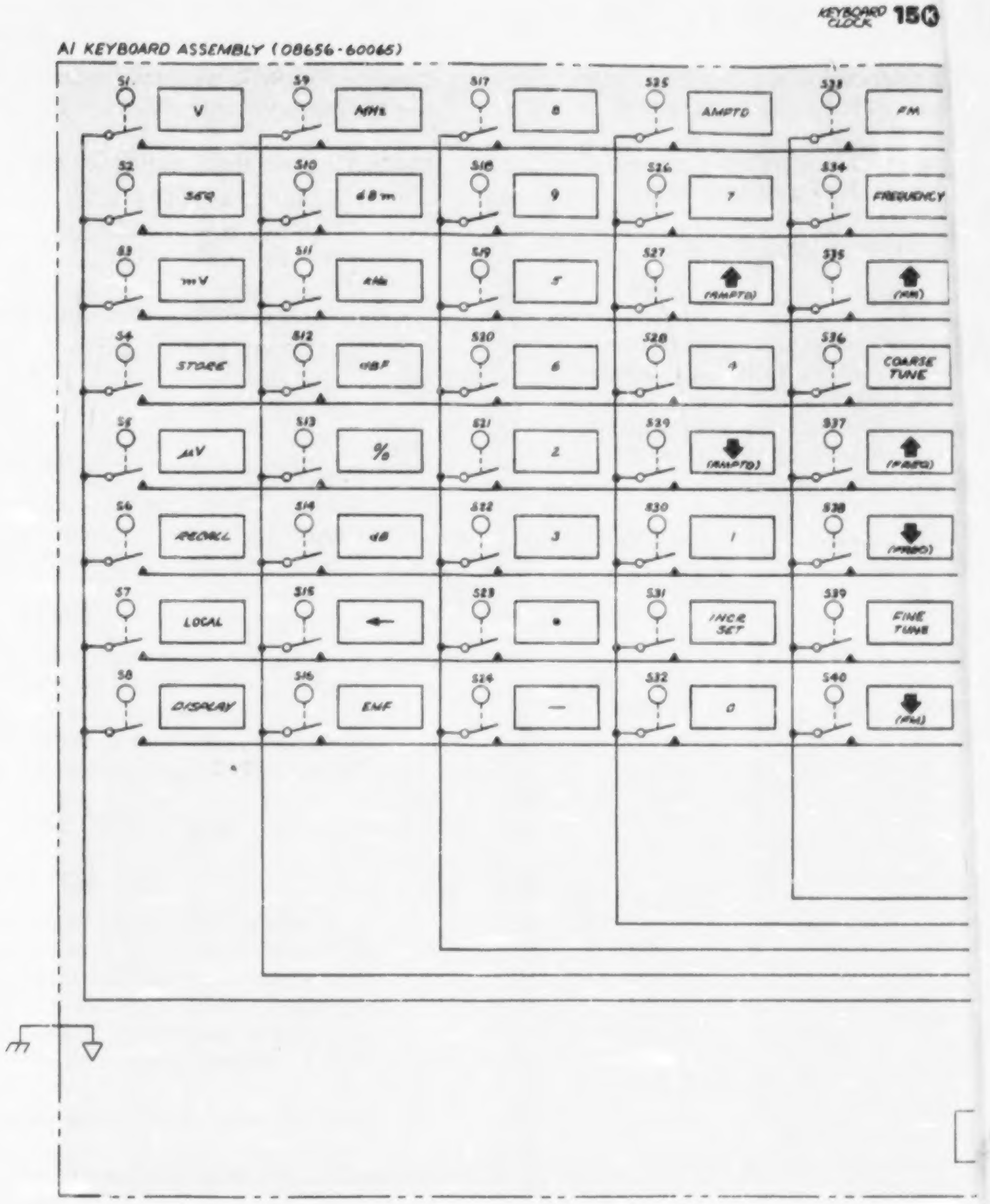
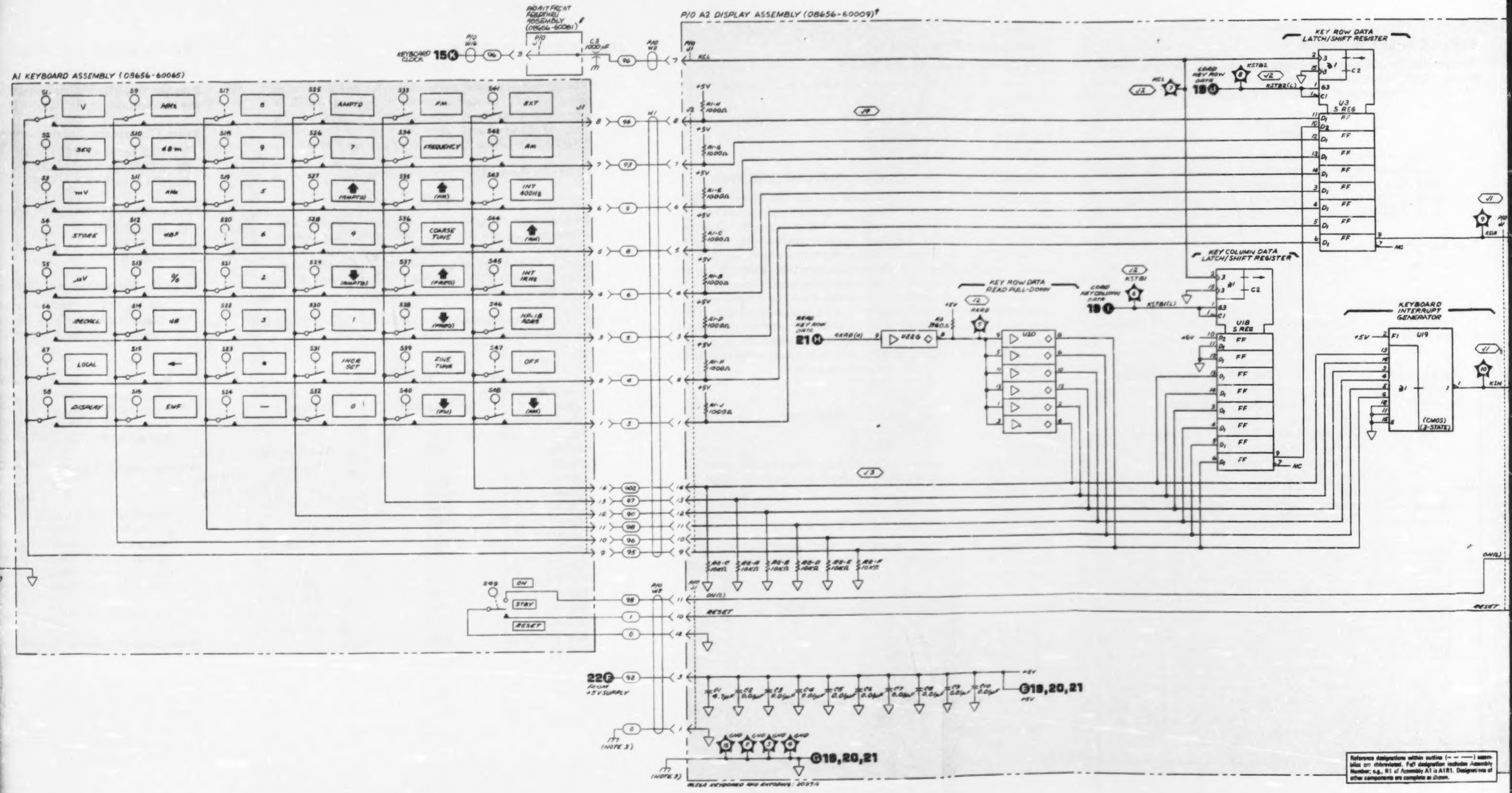
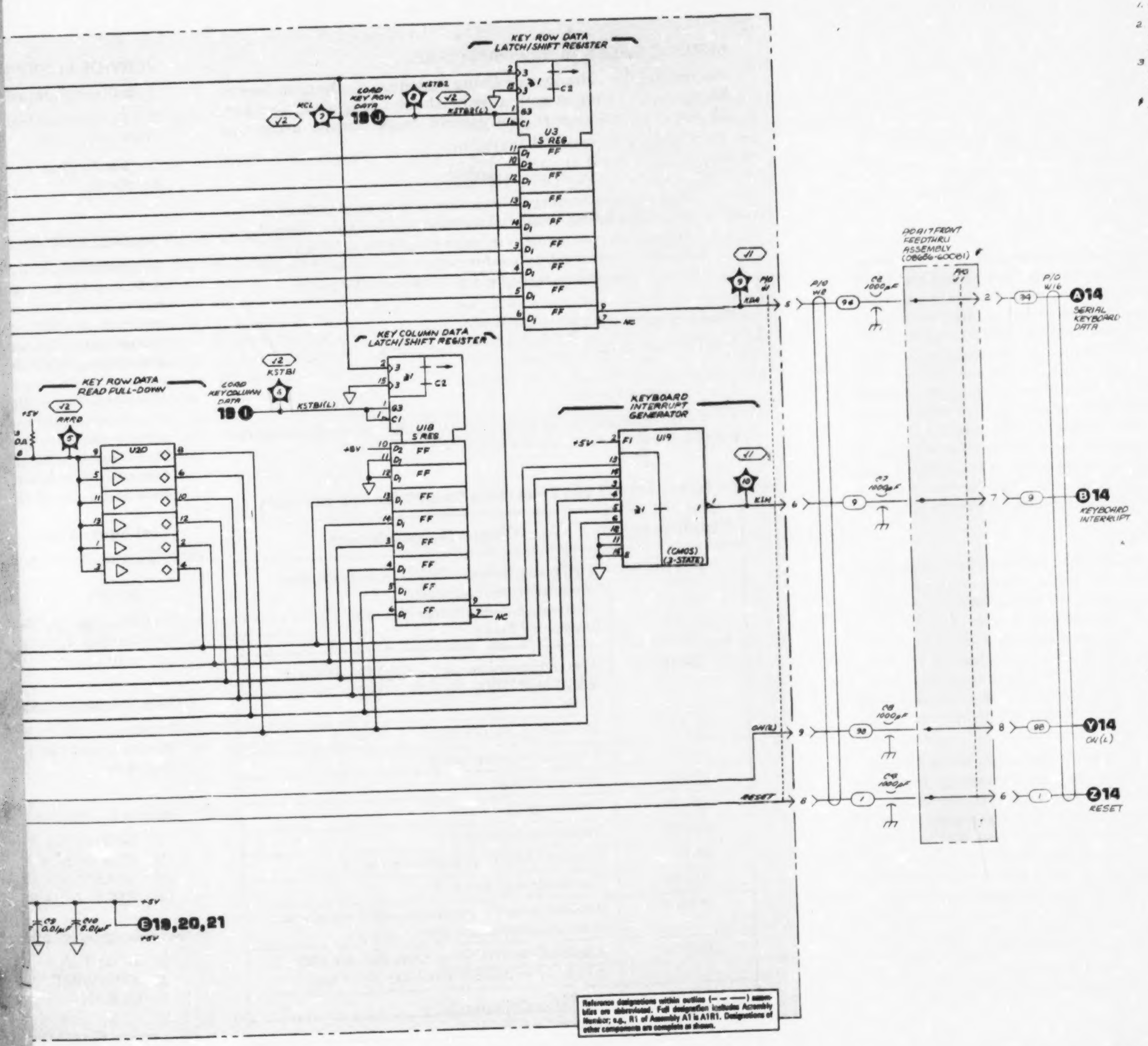

KEYBOARD CLOCK
15K
P/O A2 DISPLAY ASSEMBLY
A1 KEYBOARD ASSEMBLY
KCL
J1
J2
+5V
8 ROWS
ROW DATA
6 COLUMNS
COLUMN DATA
LOAD KEY ROW DATA
19J
KEY ROW DATA LATCH/SHIFT REGISTER
LOAD
SHIFT
SERIAL DATA OUT
PARALLEL DATA IN
SERIAL DATA IN
KDA
SERIAL KEYBOARD DATA
A14
KEY COLUMN DATA LATCH/SHIFT REGISTER
LOAD KEY COLUMN DATA
19I
SHIFT
LOAD
SERIAL DATA OUT
PARALLEL DATA IN
READ KEY ROW DATA
21H
KEY ROW DATA READ PULL-DOWN
KEYBOARD INTERRUPT GENERATOR
>1
KIN
KEYBOARD INTERRUPT
B14
ON
STBY
RESET
ON
Y14
RESET
Z14
RESET
8
6
18

Figure 8-99. Keyboard and Encoder Block Diagrams


KEYBOARD CLOCK
15K
A1 KEYBOARD ASSEMBLY (08656-60065)
S1
V
S9
MHz
S17
8
S25
AMPTD
S33
FM
S2
SEQ
S10
dBm
S18
9
S26
7
S34
FREQUENCY
S3
mV
S11
kHz
S19
5
S27
(AMPTD)
S35
(FM)
S4
STORE
S12
dBf
S20
6
S28
4
S36
COARSE TUNE
S5
μV
S13
%
S21
2
S29
(AMPTD)
S37
(FREQ)
S6
RECALL
S14
dB
S22
3
S30
1
S38
(FREQ)
S7
LOCAL
S15
←
S23
•
S31
INCR SET
S39
FINE TUNE
S8
DISPLAY
S16
EMF
S24
—
S32
0
S40
(FM)


A1 KEYBOARD ASSEMBLY (08656-60065)
P/O A2 DISPLAY ASSEMBLY (08656-60009)
P/O A17 FRONT FEEDTHRU ASSEMBLY (08656-60081)
KEYBOARD CLOCK
15K
C3 1000 pF
P/O W16
P/O W8
P/O J1
KCL
J1
J2
W1
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21
S22
S23
S24
S25
S26
S27
S28
S29
S30
S31
S32
S33
S34
S35
S36
S37
S38
S39
S40
S41
S42
S43
S44
S45
S46
S47
S48
S49
V
SEQ
mV
STORE
μV
RECALL
LOCAL
DISPLAY
MHz
dBm
kHz
dBf
%
dB
←
EMF
8
9
5
6
2
3
•
—
AMPTD
7
(AMPTD)
4
(AMPTD)
1
INCR SET
0
FM
FREQUENCY
(FM)
COARSE TUNE
(FREQ)
(FREQ)
FINE TUNE
(FM)
EXT
AM
INT 400Hz
(AM)
INT 1kHz
HP-IB ADRS
OFF
(AM)
ON
STBY
RESET
ON(L)
+5V
A1-H 1000Ω
A1-G 1000Ω
A1-E 1000Ω
A1-C 1000Ω
A1-B 1000Ω
A1-D 1000Ω
A1-F 1000Ω
A1-J 1000Ω
A6-C 10kΩ
A6-A 10kΩ
A6-B 10kΩ
A6-D 10kΩ
A6-E 10kΩ
A6-F 10kΩ
KEY ROW DATA LATCH/SHIFT REGISTER
U3 S REG
C2
KSTB2
LOAD KEY ROW DATA
19J
KSTB2(L)
D1
FF
KCR
KEY COLUMN DATA LATCH/SHIFT REGISTER
U18 S REG
LOAD KEY COLUMN DATA
19I
KSTB1
KSTB1(L)
KEY ROW DATA READ PULL-DOWN
U20
READ KEY ROW DATA
21H
RKRD(H)
U22G
R5 3160Ω
RKRD
KEYBOARD INTERRUPT GENERATOR
U19
(CMOS) (3-STATE)
KIN
NC
22E
FROM +5V SUPPLY
C1 4.7μF
C2 0.01μF
C3 0.01μF
C4 0.01μF
C5 0.01μF
C6 0.01μF
C7 0.01μF
C8 0.01μF
C9 0.01μF
C10 0.01μF
E19,20,21
GND
G19,20,21
(NOTE 3)

Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.


KEY ROW DATA LATCH/SHIFT REGISTER
U3 S REG
FF
D1
D2
C2
G3
C1
NC
MCL
LOAD KEY ROW DATA
KSTB2
KSTB2(L)
19 J
√2
KEY COLUMN DATA LATCH/SHIFT REGISTER
U18 S REG
LOAD KEY COLUMN DATA
KSTB1
KSTB1(L)
19 I
+5V
KEY ROW DATA READ PULL-DOWN
RRRD
U20
KEYBOARD INTERRUPT GENERATOR
U19
F1
(CMOS)
(3-STATE)
√1
KDA
KIN
P/O W1
P/O W8
C8 1000pF
C7 1000pF
C8 1000pF
C9 1000pF
A2 A17 FRONT FEEDTHRU ASSEMBLY (08686-60081)
P/O J1
P/O W16
A14 SERIAL KEYBOARD DATA
B14 KEYBOARD INTERRUPT
Y14 ON(L)
Z14 RESET
ON(L)
RESET
C9 0.01μF
C10 0.01μF
E19,20,21
+5V

Reference designations within outline (– – ––) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. A1 CHASSIS GROUND IS ACHIEVED THROUGH A1J1-16 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. A2 CHASSIS GROUND IS ACHIEVED THROUGH A2J1-1 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.

# INDICATES CIRCUIT CHANGE. SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A2
C2-4, 7,8 W1, 8, 16	C1-10 J1,2 R1-3 TP1-10 U3, 18-20, 22
A1	A17
J1 S1-49	J1

LOGIC LEVELS

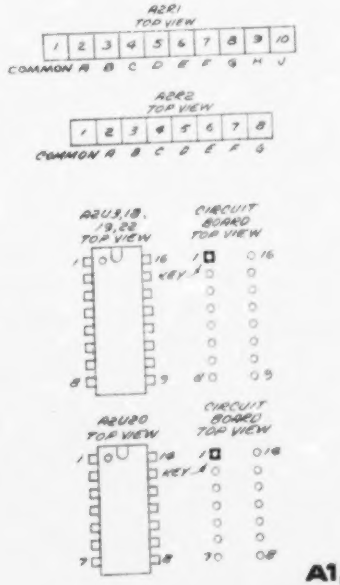
	TTL	CMOS
HIGH	>2V	>3.5V
LOW	<0.8V	<1.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
A2	
U3,18	1820-1560
U19	1820-1316
U20	1820-0618
U22	1820-2186

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U3,18	+5V - 16 ▽ - 8
U19	+5V - 16 ▽ - 7-10
U20	+5V - 14 ▽ - 7
U22	+5V - 16 ▽ - 1


A2R1
TOP VIEW
1 2 3 4 5 6 7 8 9 10
COMMON A B C D E F G H J
A2R2
TOP VIEW
1 2 3 4 5 6 7 8
COMMON A B C D E F G
A2U3,18, 19,22 TOP VIEW
1
16
8
9
KEY
CIRCUIT BOARD TOP VIEW
A2U20 TOP VIEW
14
7
8

18
A1,P/O A2

Figure 8-100. Keyboard and Encoder Schematic Diagram

SERVICE SHEET 19
P/O A2 DISPLAY ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

Display Control

Sixteen bits of serial display data (DDA) are sent from the Microprocessor via the Serial I/O control circuits (refer to Service Sheet 15) to Data Shift Registers U24 and U23 respectively. Six of the eight bits stored in U24 are decoded to produce eleven display strobes (DSTB1 through DSTB11) and two keyboard strobes (KSTB1 and KSTB2). DSTB1 through DSTB3 are used to strobe modulation display data (refer to Service Sheet 21), DSTB4 through DSTB8 are used to strobe frequency display data (refer to Service Sheet 20), DSTB8 through DSTB11 are used to strobe amplitude display data (refer to Service Sheet 21), and the two keyboard strobes (KSTB1 and KSTB2) are used to strobe column and row data from the keyboard (refer to Service Sheet 18). Strobe decoding takes place in the Display and Keyboard Strobe Decoders U26 and U25. The decoder outputs remain high until all 16 bits of display data are shifted in and settled.

Display data is shifted into the two shift registers by the display clock (DCL). Each transition of the display clock triggers U28A which forms part of the Serial Data Entry Timing Control circuitry. This circuitry is used to ensure that the data has at least 72 μs to settle after the last clock pulse clocks the sixteenth data bit into U24. When U28A times out, it clocks U28B which goes high for 5 μs to cause the bits stored in U24 to be decoded. During the period that the strobe is active (low), the display data stored in U23 will be decoded and latched to drive the respective 7-segment display or LED annunciator (refer to Service Sheets 20 and 21).

Frequency display decimal point drive is developed when display data bits 2 through 7 are strobed into the Frequency Display Decimal Point Latches U30 by DSTB4. The Microprocessor ensures that only one of these bits is active (low) at any given time (except during the power-up subroutine). When one of these bits is active (low), the associated decimal point control line (U6 through U11-Pin 9) will be pulled high through the associated network resistor (R6A, R7A, R8A, R9A, R10A, and R11A) to light the respective decimal point (refer to Service Sheet 20). When the bits are inactive (high), the stored output will be inverted by the associated Frequency Display Decimal Point Driver U21B through U21G. This will cause the associated decimal point control line (U6 through U11-Pin 9) to be pulled low to inhibit the respective decimal point from being lit.

TROUBLESHOOTING

Troubleshooting is done on the circuits of Service Sheet 19 when a malfunction seems to have occurred in the keyboard or display.

SERVICE SHEET 19 (Cont'd)

Perform the Troubleshooting Using Signature Analysis on Service Sheets 14, 15, and 16 as well as the Troubleshooting on Service Sheet 18 before attempting to troubleshoot these circuits using this procedure.

NOTE

This troubleshooting information is to be used instead of Troubleshooting Using Signature Analysis for Signal Generators with serial number prefixes 2009A, 2014A and 2018A. If preferred, this information may be used for all Signal Generators regardless of serial number prefix.

Test Equipment

Oscilloscope ....HP 1222A

⟨√1⟩ Display Clock

1. Verify that the display changes and/or the correct strobe occurs with each keystroke as shown in Table 1.

Table 1. Active Display Strobe versus Change in Displayed Information

Display Strobe	Change in Displayed Information
DSTB1	HP-IB annunciators REMOTE or ADDRESS Modulation decimal point Modulation annunciators % or kHz Frequency digit 8.
DSTB2	Modulation annunciators: EXT AM, INT AM, EXT FM, INT FM, HI EXT, LO EXT, 400 Hz or 1 kHz.
DSTB3	Modulation digits 1 or 2
DSTB4	Frequency decimal point
DSTB5	Frequency digit 1 or 2
DSTB6	Frequency digit 3 or 4
DSTB7	Frequency digit 5 or 6
DSTB8	Frequency digit 7 or amplitude digit 2
DSTB9	Amplitude digit 3 or 4
DSTB10	Amplitude digit 1, amplitude digit decimal point or the amplitude sign (plus or minus).
DSTB11	Amplitude annunciators: dBm, dBf, dB, EMF, V, mV, or μV or RKRD* (Read Key Row Data).
KSTB1	any key*
KSTB2	any key*

*DSTB11 (due to RKRD), KSTB1 and KSTB2 are strobed each time a key is pressed.

SERVICE SHEET 1

⟨√2⟩ Serial Data E

1. Verify that U28I clock pulse ends.

2. Verify that a c keystroke.

TROUBLESHOOTI

Troubleshooting is c defect seems to be r operation. The trou although looking at lem is due to a keybo about a possible defe correct, take anothe this service sheet. De try contained on Ser service sheet are inc and other control si Sheet 15 before arriv BD4 and consider th

Test Equipment

Signature Analyzer

The signatures for Signal Gene and below.

Test 1. Display Dat

Purpose. To verify t Microprocessor to t Registers.

Setup. Connect the s
1) GND to 'GND'
2) CLK to 'SA4'
3) START to 'SA
4) STOP to 'SA5'

Set the signature an
1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Ge
1) Set the LOGIC
2) Connect a jum
3) Connect a jum

SERVICE SHEET 19 (Cont'd)

√2 Serial Data Entry and Timing

1. Verify that U28B-Pin 5 goes high for 5 μs but 72 μs after the last clock pulse ends.

2. Verify that a clock pulse train occurs at A2TP11 for each keystroke.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

Troubleshooting is done on the circuits of Service Sheet 19 when a defect seems to be related to the front panel displays or keyboard operation. The troubleshooting provided is signature analysis although looking at the various displays or realizing that the problem is due to a keyboard malfunction may provide more information about a possible defect. If all the signatures on this service sheet are correct, take another look at the symptoms which brought you to this service sheet. Determine if the problem may be related to circuitry contained on Service Sheets 18, 20 or 21. If any signatures on this service sheet are incorrect, recall that the data and strobes, clocks and other control signals are passed through circuitry of Service Sheet 15 before arriving here. As a last resort, return to Service Sheet BD4 and consider the other possibilities shown.

Test Equipment

Signature Analyzer ....HP 5004A

NOTE

The signatures shown on this service sheet are not valid for Signal Generators with serial numbers prefixed 2018A and below.

Test 1. Display Data Transmission Check

Purpose. To verify transmission of encoded display data from the Microprocessor to the Display Address and Display Data Shift Registers.

Setup. Connect the signature analyzer as follows:

1) GND to 'GND'
2) CLK to 'SA4' A11TP7
3) START to 'SA5' A11TP5
4) STOP to 'SA5' A11TP9

Set the signature analyzer's controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Generator as follows:

1) Set the LOGIC/RAM switch P/O A11S1 to LOGIC.
2) Connect a jumper from A2TP14 T02 to ground.
3) Connect a jumper between A11TP10 SA6 and A2TP1 SA7.

SERVICE SHEET 19 (Cont'd)

NOTE

If the Signal Generator's address switch has been set to other than '07', the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON.

Initialize. Briefly short A11TP3 'NMI' to ground.

NOTE

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

Probe. Connect the probe to each node shown in Table 1. Verify that each signature is correct and stable.

Table 1. Display Data Signatures

Node	Correct Signature	Comments
+5V	F84P	
•U24 #8	F84P	DISP CLK
U24 #1	6UPP	DISP DATA
U24 #3	8A0H	
U24 #4	HCH1	
U24 #5	F06F	
U24 #6	F672	
U24 #10	05C8	
U24 #11	2235	
U24 #12	6UH4	
U24 #13	37PA	
U23 #3	2UAU	
U23 #4	7241	
U23 #5	P6U4	
U23 #6	A161	
U23 #10	890U	
U23 #11	FH78	
U23 #12	C382	
U23 #13	7758	

•Probe should blink.

If troubleshooting is completed, remove the jumpers and reset the LOGIC/RAM switch to RAM. Also, if the HP-IB address switch was changed, reset the address switch (Service Sheet 17) to the original address. Then set the front panel RESET-STBY-ON switch to RESET and back to ON.

SERVICE SHEET 19 (Cont'd)

Test 2. Display Strobe Data Transmission and Decoder Check

Purpose. To verify transmission of encoded display strobe data from the Microprocessor through the Display Strobe Decoders.

Setup. Connect the signature analyzer as follows:

1) CLK to 'E' A11TP11
2) START to 'SA1' A11TP5
3) STOP to 'SA2' A11TP6

Set the signature analyzer's controls as follows:

1) START-OUT
2) STOP-IN
3) CLK-IN

Set up the Signal Generator as follows:

1) Set the LOGIC/RAM switch P/O A11S1 to LOGIC.
2) Connect a jumper between A2TP14 T02 and ground.
3) Connect a jumper between A11TP10 SA6 and A2TP1 SA7.

NOTE

If the Signal Generator's address switch has been set to other than '07', the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON.

Initialize. Briefly short A11TP3 NMI to ground.

NOTES

With careless grounding of the test point, it is possible to get the Microprocessor into a program routine other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

All LEDs should be cycling on and off rapidly.

Probe. Connect the probe to each node shown in Table 2. Verify that each signature is correct and stable.

If troubleshooting is completed and the signatures are taken, remove the jumpers installed between test points and/or ground. Reset the LOGIC/RAM switch to the RAM position. Also, if the HP-IB switch was changed, reset the address switch (refer to Service Sheet 17) to the original address. Set the front panel RESET-STBY-ON switch to RESET and back to ON.

SERVICE SHEET 19 (Cont'd)

Table 2. Display and Keyboard Strobe Signatures

Node	Correct Signature*	Comments
+5V	H6H5	
U26 #7	C524	
U26 #9	FU10	
U26 #10	66UF	
U26 #11	1F0A	
U26 #12	5A73	
U26 #13	P3HA	
U26 #14	A128	
U26 #4	FP00	
U26 #6	H6H5	no blink
+5V	H6H5	
U25 #9	H161	
U25 #10	CP72	
U25 #11	93AH	
U25 #12	PH45	
U25 #13	FF4P	
U25 #14	8H64	
U25 #4	FP00	
U25 #6	H6H5	no blink

*Probe tip should blink.

Test 3. Decimal Point Data Transmission Check

Purpose. To verify transmission of encoded decimal point data from the Microprocessor to the Frequency Display Decimal Point Latch.

Setup. Connect the signature analyzer controls as follows:

1) GND to 'GND' A11TP2
2) START to SA5 A11TP9
3) STOP to SA5 A11TP9
4) CLK to SA4 A11TP7

Set the signature analyzer's controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Generator as follows:

1) Set the LOGIC/RAM switch to the LOGIC position.
2) Connect a jumper between A2TP14 'T02' and ground.
3) Connect a jumper between A11TP10 'SA6 and A2TP15 'SA7'.

NOTE

If the Signal Generator's address switch has been set to other than '07', the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON.

Initialize. Briefly short A11TP3 NMI to ground.

NOTES

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

All LEDs should be cycling on and off rapidly.

Probe. Connect the probe to each node shown i Table 3. Verify that each signature is correct an stable.

Table 3. Decimal Point Signatures

Node	Correct Signature	Comments
+5V	F84P	
U30 #2	F9H9	FR DP 3
U30 #5	8C19	FR DP 2
U30 #7	54PH	FR DP 1
U30 #10	7903	FR DP 4
U30 #12	A44F	FR DP 5
U30 #15	5FC5	FR DP 6

Remove the jumpers between test points and a tes point and ground. Reset the LOGIC/RAM switch t the RAM position.

If the HP-IB switch was changed, reset the addres switch to the original address. Then set the fro panel RESET-STBY-ON switch to RESET an back to ON.

P/O A2 ASSEMBLY

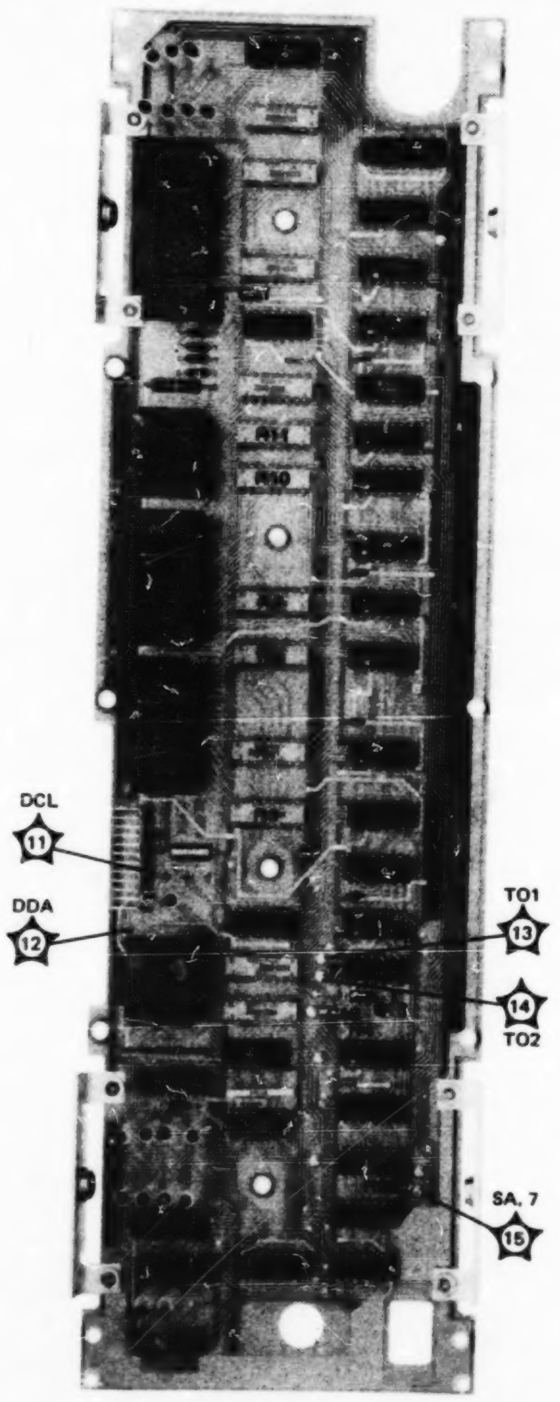


Figure 8-101. Display Control Component Locations

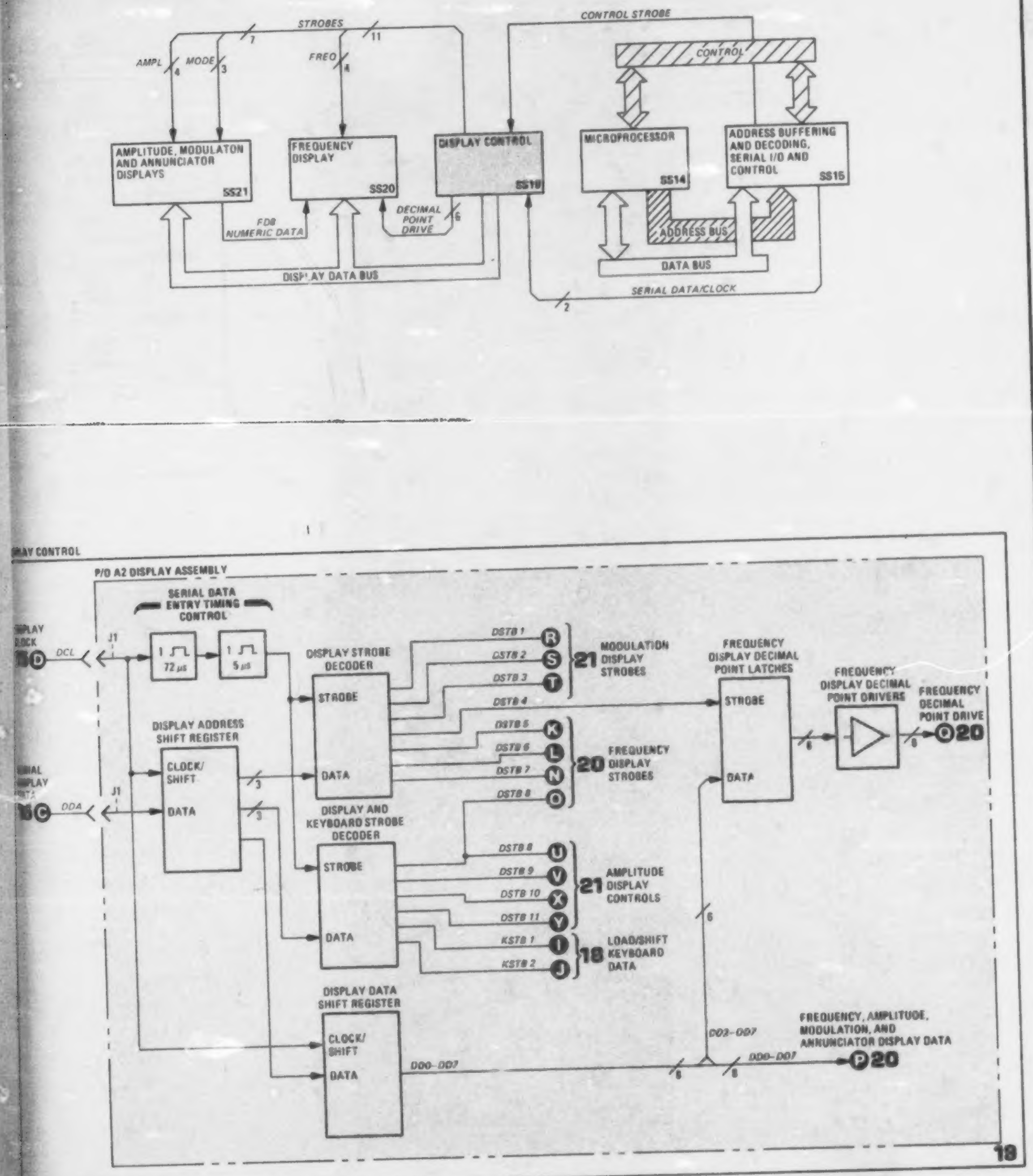
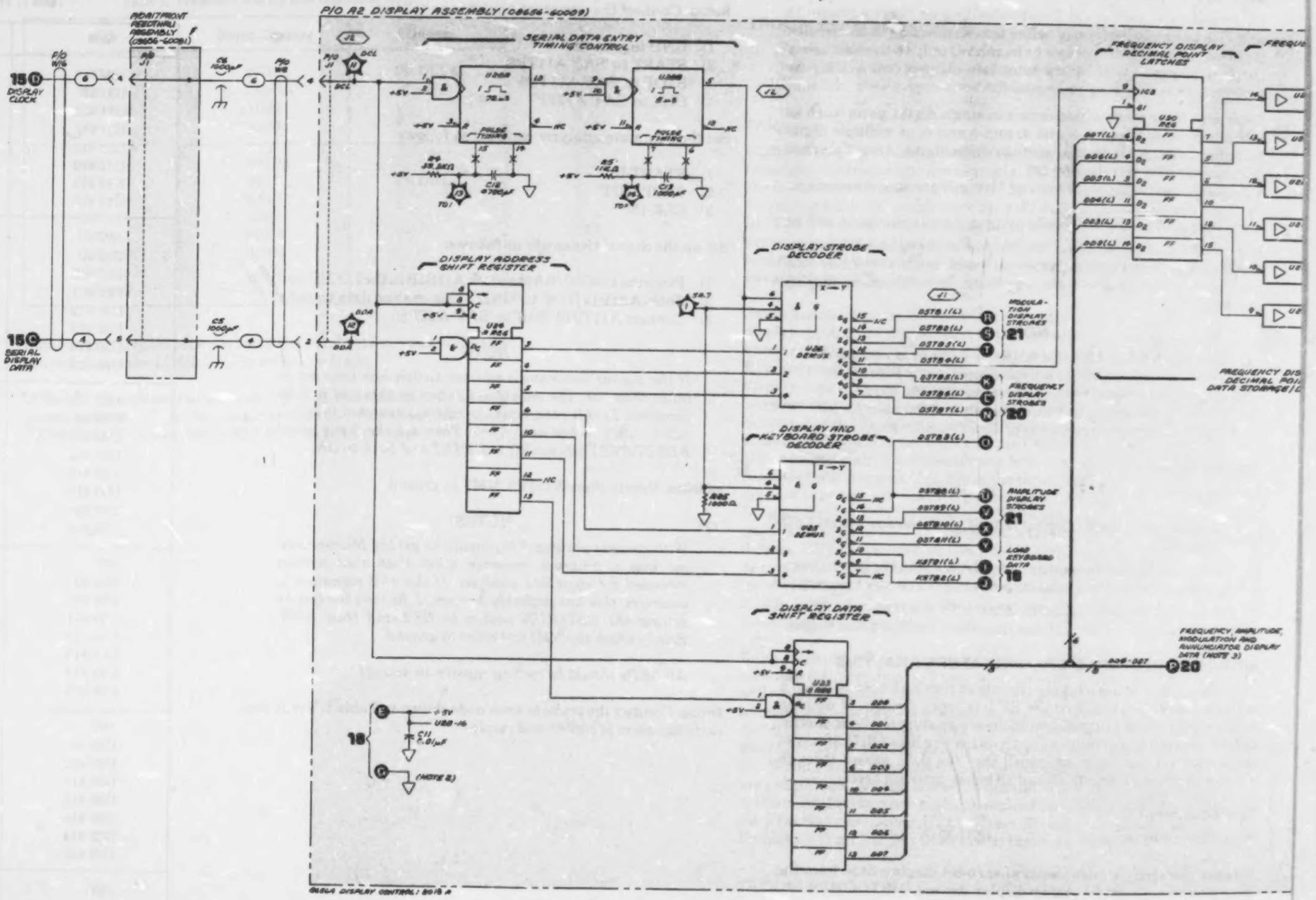
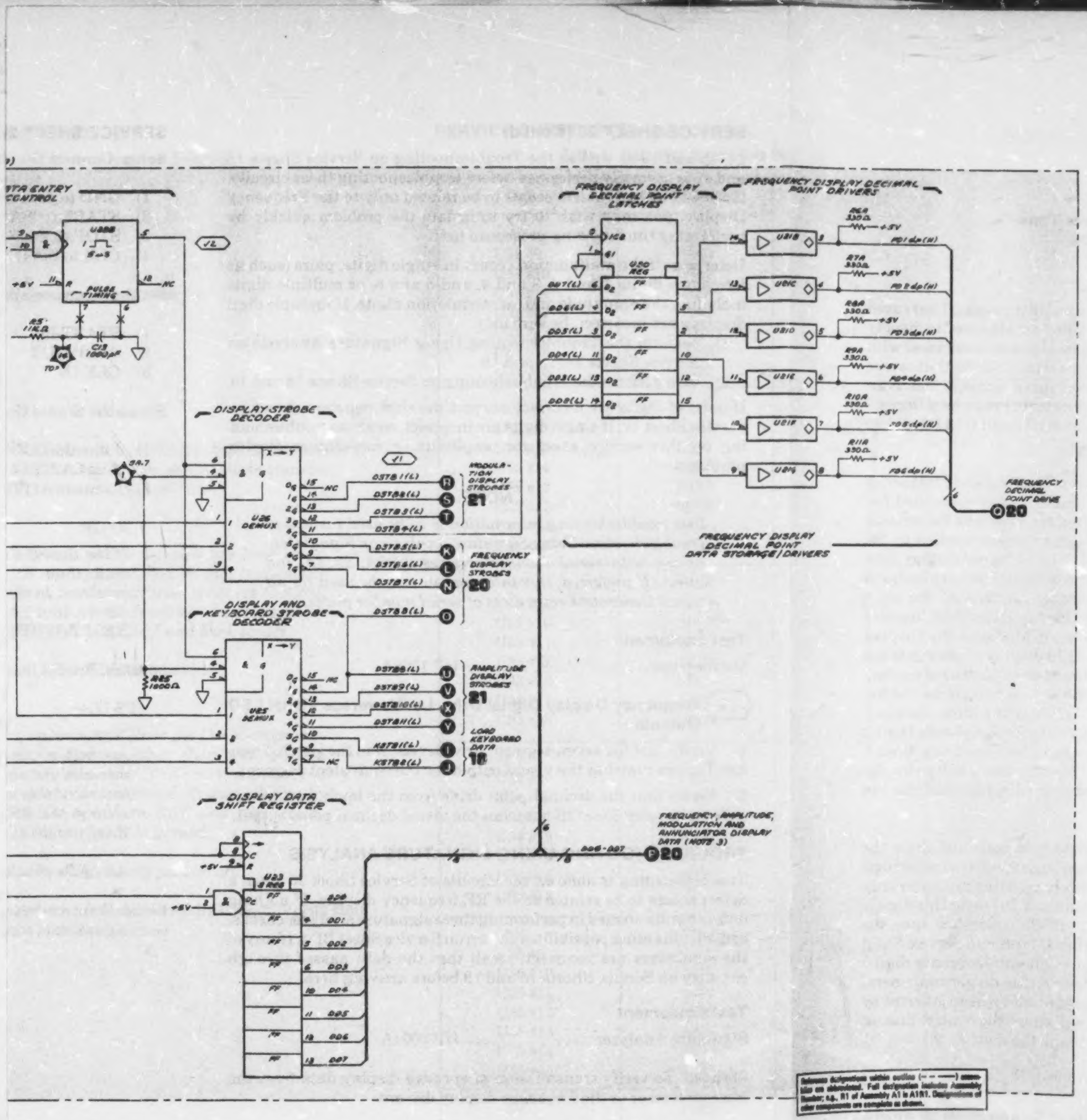

STROBES
7
11
AMPL
4
MODE
3
FREQ
4
CONTROL STROBE
CONTROL
AMPLITUDE, MODULATON AND ANNUNCIATOR DISPLAYS
SS21
FREQUENCY DISPLAY
SS20
DISPLAY CONTROL
SS18
MICROPROCESSOR
SS14
ADDRESS BUFFERING AND DECODING, SERIAL I/O AND CONTROL
SS15
FDB NUMERIC DATA
DECIMAL POINT DRIVE
6
ADDRESS BUS
DATA BUS
DISPLAY DATA BUS
SERIAL DATA/CLOCK
2
AY CONTROL
P/O A2 DISPLAY ASSEMBLY
SERIAL DATA ENTRY TIMING CONTROL
PLAY
OCK
D
DCL
J1
72 μs
5 μs
DISPLAY STROBE DECODER
STROBE
DATA
DISPLAY ADDRESS SHIFT REGISTER
CLOCK/ SHIFT
DATA
3
3
RIAL
PLAY
TA
C
DDA
J1
DISPLAY AND KEYBOARD STROBE DECODER
STROBE
DATA
DISPLAY DATA SHIFT REGISTER
CLOCK/ SHIFT
DATA
DD0-DD7
DSTB 1
R
DSTB 2
S
DSTB 3
T
21
MODULATION DISPLAY STROBES
DSTB 4
DSTB 5
K
DSTB 6
L
DSTB 7
N
DSTB 8
O
20
FREQUENCY DISPLAY STROBES
DSTB 8
U
DSTB 9
V
DSTB 10
X
DSTB 11
Y
21
AMPLITUDE DISPLAY CONTROLS
KSTB 1
I
KSTB 2
J
18
LOAD/SHIFT KEYBOARD DATA
FREQUENCY DISPLAY DECIMAL POINT LATCHES
STROBE
DATA
6
FREQUENCY DISPLAY DECIMAL POINT DRIVERS
6
FREQUENCY DECIMAL POINT DRIVE
O
20
6
DD2-DD7
6
8
DD0-DD7
FREQUENCY, AMPLITUDE, MODULATION, AND ANNUNCIATOR DISPLAY DATA
P
20
18

Figure 8-102. Display Control Block Diagrams


P/O A2 DISPLAY ASSEMBLY (08656-60009)
A2A1 FRONT FEEDTHRU ASSEMBLY (08656-60081)
P/O W16
P/O J1
P/O W8
P/O J1
J2
J2
15 D DISPLAY CLOCK
15 C SERIAL DISPLAY DATA
C6 1000pF
C5 1000pF
DCL
SDA
SERIAL DATA ENTRY TIMING CONTROL
U28A 78nS
U28B 6nS
PULSE TIMING
+5V
NC
R4 38.3KΩ
C12 4700pF
TD1
R5 11KΩ
C13 1000pF
DISPLAY ADDRESS SHIFT REGISTER
U26 8 REG
FF
DISPLAY STROBE DECODER
U36 DEMUX
X→Y
SA.7
J1
DSTB1(L)
DSTB2(L)
DSTB3(L)
DSTB4(L)
DSTB5(L)
DSTB6(L)
DSTB7(L)
DSTB8(L)
R
S
T
K
G
N
O
MODULATION DISPLAY STROBES 21
FREQUENCY DISPLAY STROBES 20
DISPLAY AND KEYBOARD STROBE DECODER
U35 DEMUX
R85 1000Ω
DSTB8(L)
DSTB9(L)
DSTB10(L)
DSTA11(L)
KSTB1(L)
KSTB2(L)
U
V
X
Y
I
J
AMPLITUDE DISPLAY STROBES 21
LOAD KEYBOARD DATA 18
FREQUENCY DISPLAY DECIMAL POINT LATCHES
U30 REG
DD7(L)
DD6(L)
DD5(L)
DD4(L)
DD3(L)
DD2(L)
FREQUENCY DISPLAY DECIMAL POINT DATA STORAGE
DISPLAY DATA SHIFT REGISTER
U33 8 REG
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD0-DD7
P 20
FREQUENCY, AMPLITUDE, MODULATION AND ANNUNCIATOR DISPLAY DATA (NOTE 3)
18
E
+5V
U28-16
C11 0.01μF
G
(NOTE 2)
8656A DISPLAY CONTROL: 8018 A


STA ENTRY CONTROL
U22B
PULSE TIMING
+5V
NC
R5 11kΩ
C13 1000pF
TP
√2
DISPLAY STROBE DECODER
9A.7
X→Y
U26 DEMUX
NC
√1
DSTB1(L)
DSTB2(L)
DSTB3(L)
DSTB4(L)
DSTB5(L)
DSTB6(L)
DSTB7(L)
DSTB8(L)
MODULATION DISPLAY STROBES
21
FREQUENCY DISPLAY STROBES
20
DISPLAY AND KEYBOARD STROBE DECODER
R25 1000Ω
U25 DEMUX
DSTB9(L)
DSTB10(L)
DSTB11(L)
KSTB1(L)
KSTB2(L)
AMPLITUDE DISPLAY STROBES
21
LOAD KEYBOARD DATA
18
DISPLAY DATA SHIFT REGISTER
U23 S REG
FF
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
FREQUENCY DISPLAY DECIMAL POINT LATCHES
U20 REG
DD7(L)
DD6(L)
DD5(L)
DD4(L)
DD3(L)
DD2(L)
FREQUENCY DISPLAY DECIMAL POINT DRIVERS
R6A 330Ω
R7A 330Ω
R8A 330Ω
R9A 330Ω
R10A 330Ω
R11A 330Ω
+5V
U21B
U21C
U21D
U21E
U21F
U21G
FD1dp(H)
FD2dp(H)
FD3dp(H)
FD4dp(H)
FD5dp(H)
FD6dp(H)
FREQUENCY DECIMAL POINT DRIVE
20
FREQUENCY DISPLAY DECIMAL POINT DATA STORAGE/DRIVERS
FREQUENCY, AMPLITUDE, MODULATION AND ANNUNCIATOR DISPLAY DATA (NOTE 3)
DD0-DD7
20

Reference designations within outline (— — ——) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A8J1-1 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. DISPLAY DATA BUS (DD0-DD7) IS POSITIVE TRUE FOR NUMERIC DATA, EXCEPT FOR FD6.

   DISPLAY DATA BUS (DD0-DD7) IS NEGATIVE TRUE FOR FD6 NUMERIC, DECIMAL POINT, SIGN AND ANNUNCIATOR DATA.

∮ INDICATES CIRCUIT CHANGE, SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A2
C5,6 W2,16	C11-13 J1 R4-11,25 TP11-15 U21,23-26, 28,30
A17	
J1	

LOGIC LEVELS

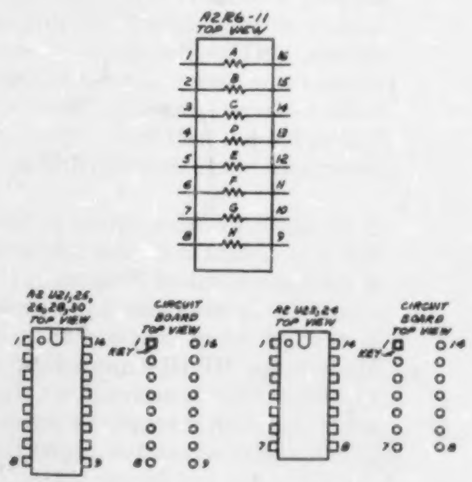
	TTL
HIGH	>2V
LOW	>0.8V
< IS MORE NEG. THAN > IS MORE POS. THAN	
OPEN	HIGH
GROUND	LOW

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
A2	
U21	1820-2186
U23,24	1820-1433
U25,26	1820-1216
U28	1820-1433
U30	1820-2056

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PART NUMBERS
A2	
U21	+5V - 16 ▽ - 1
U23,24	+5V - 14 ▽ - 7
U25, 26, 28, 30	+5V - 16 ▽ - 8


A2R6-11 TOP VIEW
A
B
C
D
E
F
G
H
A2 U21,25, 26,28,30 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY
A2 U23,24 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY

19
P/O A2

Figure 8-103. Display Control Schematic Diagram

SERVICE SHEET 20
P/O A2 DISPLAY ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Frequency Display

Eight 7-segment, common-cathode devices U6 through U13 are used to display the frequency in megahertz. They are also used to display the frequency increment value. The decimal points associated with frequency digits 1 through 6 are the only decimal points that can be lit. The frequency display decimal point drive circuitry has been previously discussed (refer to Service Sheet 19). Frequency Digits 7 and 8 have their decimal point control line (U12 and U13-Pin 9) tied low which inhibits them from being lit.

Seven Latch/Decoder/Drivers U31 through U37 decode frequency display data, store the decoded data, and drive the associated frequency display digit. The associated resistor networks R6 through R12 are used to limit the amount of drive current applied to the display digit. As previously mentioned 16 bits of serial display data are sent from the Microprocessor to the display circuitry (refer to Service Sheet 19). After a serial-to-parallel conversion, the eight most-significant bits are stored in the Display Data Shift Register U23 and the eight least-significant bits are stored in the Display Address Shift Register U24. Six of the eight display address bits are decoded to produce eleven display strobes and two keyboard strobes. Display strobes DSTB5 through DSTB8 are used to strobe the frequency display data (DD0 through DD7) into the latch/decoder/drivers. DSTB8 also strobes the display data for Amplitude Digit 2 at the same time it strobes the display data for Frequency Digit 7 (refer to Service Sheet 21). When a strobe is decoded, it will go low for 5 μs to latch a half byte (4 bits) of frequency display data into the associated latch/decoder/driver.

Each latch/decoder/driver is hard-wired to decode and drive the associated digit to display numerals 0 through 9, otherwise the digit will remain blanked. Frequency Digit 8 is hard-wired to display only a numeral 5, otherwise it will remain blanked. Drive for this digit is developed when display data bit 2 (DD2) is strobed into the Modulation/HP-IB Annunciator Latches U1 (refer to Service Sheet 21). When DD2 is active (low), the control lines of frequency digit 8 are pulled high through the series resistor R13 to display a numeral 5. When DD2 is inactive (high), the stored output will be inverted by the FD8 Numeral Driver U22A. This will cause the control lines of Frequency Digit 8 to be pulled low to blank the digit.

TROUBLESHOOTING

Troubleshooting is done on the circuits of Service Sheet 20 when a malfunction seems to be associated with the Frequency Display. The Troubleshooting Using Signature Analysis on Service Sheets 14, 15 and 16 as well as the Troubleshooting on Service Sheets 18 and 19 is normally performed before troubleshooting these circuits. However, if the problem seems to be related only to the Frequency Display, you may wish to try to isolate the problem quickly by performing the following procedure first.

Determine if the malfunction occurs in single digits, pairs (such as frequency digits 1 and 2, 3 and 4, and 5 and 6, or multiple digits including the amplitude and/or modulation digits. If multiple digit displays are incorrect, be sure to:

1) perform the Troubleshooting Using Signature Analysis on Service Sheets 14, 15 and 16
2) then perform the Troubleshooting on Service Sheets 18 and 19.

If pairs of digits are incorrect, suspect the shift registers shown on Service Sheet 19. If single digits are incorrect, continue troubleshooting on this service sheet for amplitude or modulation display problems.

NOTE

This troubleshooting information is to be used instead of Troubleshooting Using Signature Analysis on Signal Generators with serial number prefixes 2009A, 2014A and 2018A. If preferred, this information may be used for all Signal Generators regardless of serial number prefix.

Test Equipment

Oscilloscope .... HP 1222A

√1 Frequency Display Digital Drive Levels versus Visual LED Outputs

1. Verify that the seven-segment drive levels from the Latch/Decoder/Drivers matches the visual output for the equivalent segment.

2. Verify that the decimal point drive from the latch and drivers (refer to Service Sheet 19) matches the visual decimal point output.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

Troubleshooting is done on the circuits of Service Sheet 20 when a defect seems to be related to the RF frequency display. If nothing definite is discovered in performing these signature analyzer checks, consider the other possibilites shown on Service Sheet BD4. If any of the signatures are incorrect, recall that the data passes through circuitry on Service Sheets 15 and 19 before arriving here.

Test Equipment

Signature Analyzer .... HP 5004A

Purpose. To verify transmission of encoded display data from the Microprocessor to the frequency drivers.

NOTE

Signatures are not valid for Signal Generators with serial number prefixes of 2018A and below.

SERVICE SHEET 2

Setup. Connect the

1) GND to groun
2) START to 'SA
3) STOP to 'SA5'
4) CLK to 'SA4'

Set the signature an

1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Ge

1) Place the LOG
2) Short A2TP14
3) Connect A11T

If the Signal G
other than '07',
incorrect. In thi
A2=1, A3=1, A
RESET-STBY-

Initialize. Briefly shor

With careless pr
sor into a pro
intended for sig
incorrect, this h
setting the RS
Briefly touch th

All LEDs shoul

Probe. Connect the p
each signature is cor

E SHEET 20 (Cont'd)

onnect the signature analyzer as follows:

ID to ground
'ART to 'SA5' A11TP9
OP to 'SA5' A11TP9
.K to 'SA4' A11TP7

ignature analyzer controls as follows:

'ART-IN
OP-OUT
.K-IN

e Signal Generator as follows:

ace the LOGIC/RAM switch A11S1B in the LOGIC position.
ort A2TP14 'TO2' to 'GND'. This enables data transfer.
nnect A11TP10 'SA6' to 'SA7' A2TP15

NOTE

he Signal Generator's address switch has been set to er than '07', the signatures taken in this test will be rrect. In this case, reset the address switches to A1=1, =1, A3=1, A4=0 and A5=0. Then set the front panel SET-STBY-ON switch to RESET and back to ON.

Briefly short A11TP3 'NMI' to ground.

NOTES

h careless probing it is possible to get the Microprocessor into a program sequence other than that portion nded for signature analysis. If the +5V signature is rrect, this has probably happened. Restart the test by ing the RST/RUN switch to RST and then RUN. fly touch the NMI test point to ground.

LEDs should be cycling rapidly on and off.

onnect the probe to each node shown in Table 1. Verify that nature is correct and stable.

SERVICE SHEET 20 (Cont'd)

Table 1. Frequency Display Data Signatures

Node	Correct Signature	Comments
+5V	F84P	FR DIG 1
U31 #9	54A0	
U31 #10	0H80	
U31 #11	09FF	
U31 #12	1HAA	
U31 #13	01H8	
U31 #14	FU58	
U31 #15	3A9C	
+5V	F84P	FR DIG 2
U32 #9	H9PA	
U32 #10	1353	
U32 #11	UA1C	
U32 #12	PFF5	
U32 #13	25F6	
U32 #14	4AH1	
U32 #15	5554	
+5V	F84P	FR DIG 3
U33 #9	7059	
U33 #10	3P0P	
U33 #11	13PC	
U33 #12	C4P5	
U33 #13	6PC6	
U33 #14	133P	
U33 #15	CC02	
+5V	F84P	FR DIG 4
U34 #9	F3A2	
U34 #10	C22P	
U34 #11	P8U9	
U34 #12	U339	
U34 #13	U1H0	
U34 #14	9209	
U34 #15	2659	
+5V	F84P	FR DIG 5
U35 #9	UH23	
U35 #10	7880	
U35 #11	4135	
U35 #12	55PC	
U35 #13	A492	
U35 #14	AP11	
U35 #15	8F6F	
+5V	F84P	FR DIG 6
U36 #9	2C1A	
U36 #10	3168	
U36 #11	UUU9	

SERVICE SHEET 20 (Cont'd)

Table 1. Frequency Display Data Signatures (Cont'd)

Node	Correct Signature	Comments
U36 #12	26HP	FR DIG 6 (Cont'd)
U36 #13	PHP1	
U36 #14	1U22	
U36 #15	82C0	
+5V	F84P	FR DIG 7
U37 #9	9F11	
U37 #10	1F17	
U37 #11	8582	
U37 #12	PUHF	
U37 #13	HUU9	
U37 #14	A360	
U37 #15	6847	

Remove the jumpers between test points and between test point and ground. Reset the LOGIC/RAM switch to RAM.

If the HP-IB address switch was changed, reset the address switch (Service Sheet 17) to the original address. Set the front panel RESET-STBY-ON switch to RESET and back to ON.

y Data Signatures

re	Comments
	FR DIG 1
	FR DIG 2
	FR DIG 3
	FR DIG 4
	FR DIG 5
	FR DIG 6

SERVICE SHEET 20 (Cont'd)

Table 1. Frequency Display Data Signatures (Cont'd)

Node	Correct Signature	Comments
U36 #12 U36 #13 U36 #14 U36 #15	26HP PHP1 1U22 82C0	FR DIG 6 (Cont'd)
+5V U37 #9 U37 #10 U37 #11 U37 #12 U37 #13 U37 #14 U37 #15	F84P 9F11 1F17 8582 PUHF HUU9 A360 6847	FR DIG 7

Remove the jumpers between test points and between test point and ground. Reset the LOGIC/RAM switch to RAM.

If the HP-IB address switch was changed, reset the address switch (Service Sheet 17) to the original address. Set the front panel RESET-STBY-ON switch to RESET and back to ON.

Display Control
P/O A2
SERVICE SHEET 19

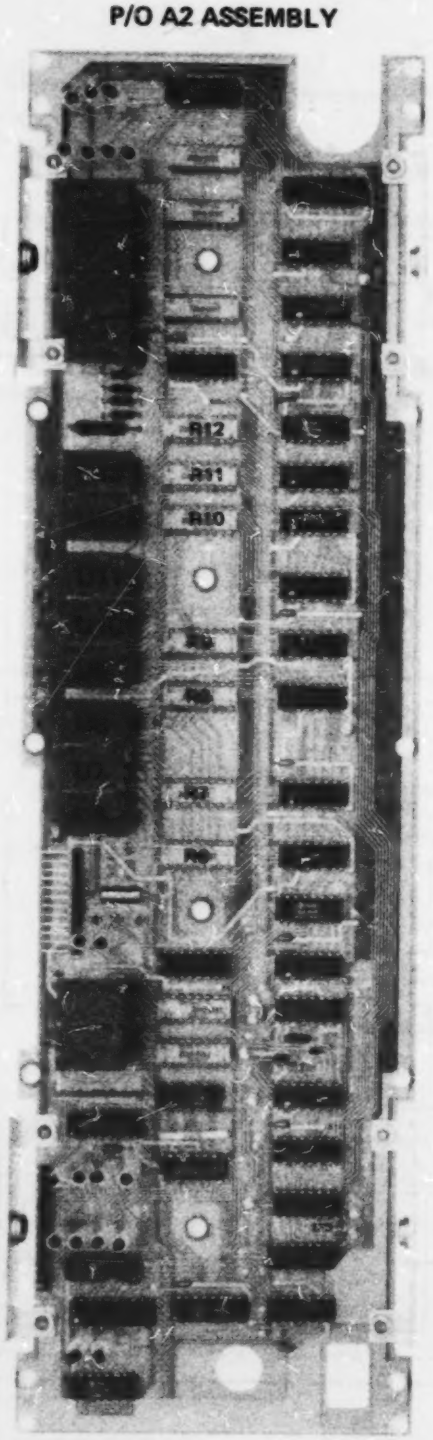


Figure 8-104. Frequency Displays Component Locations

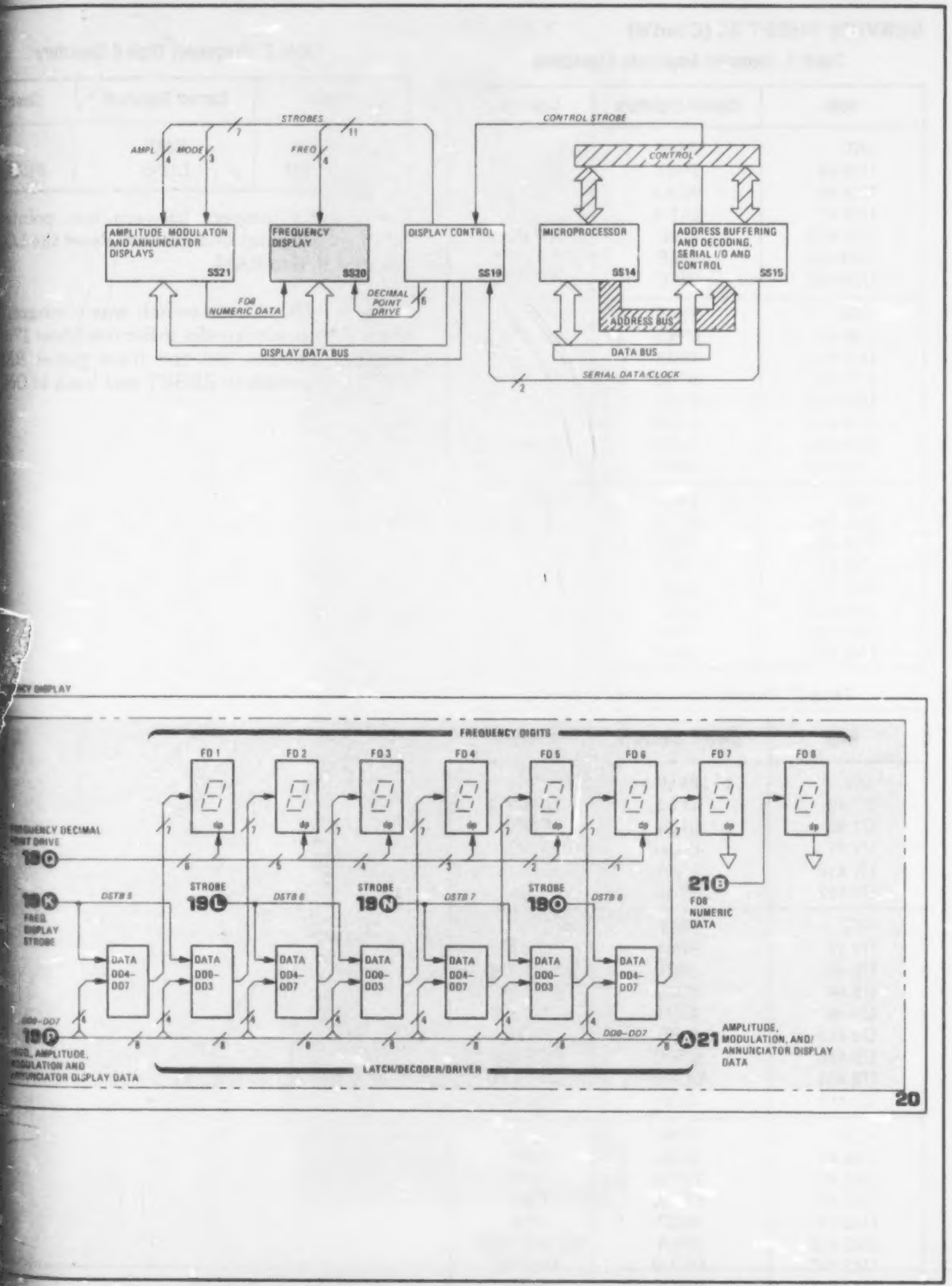
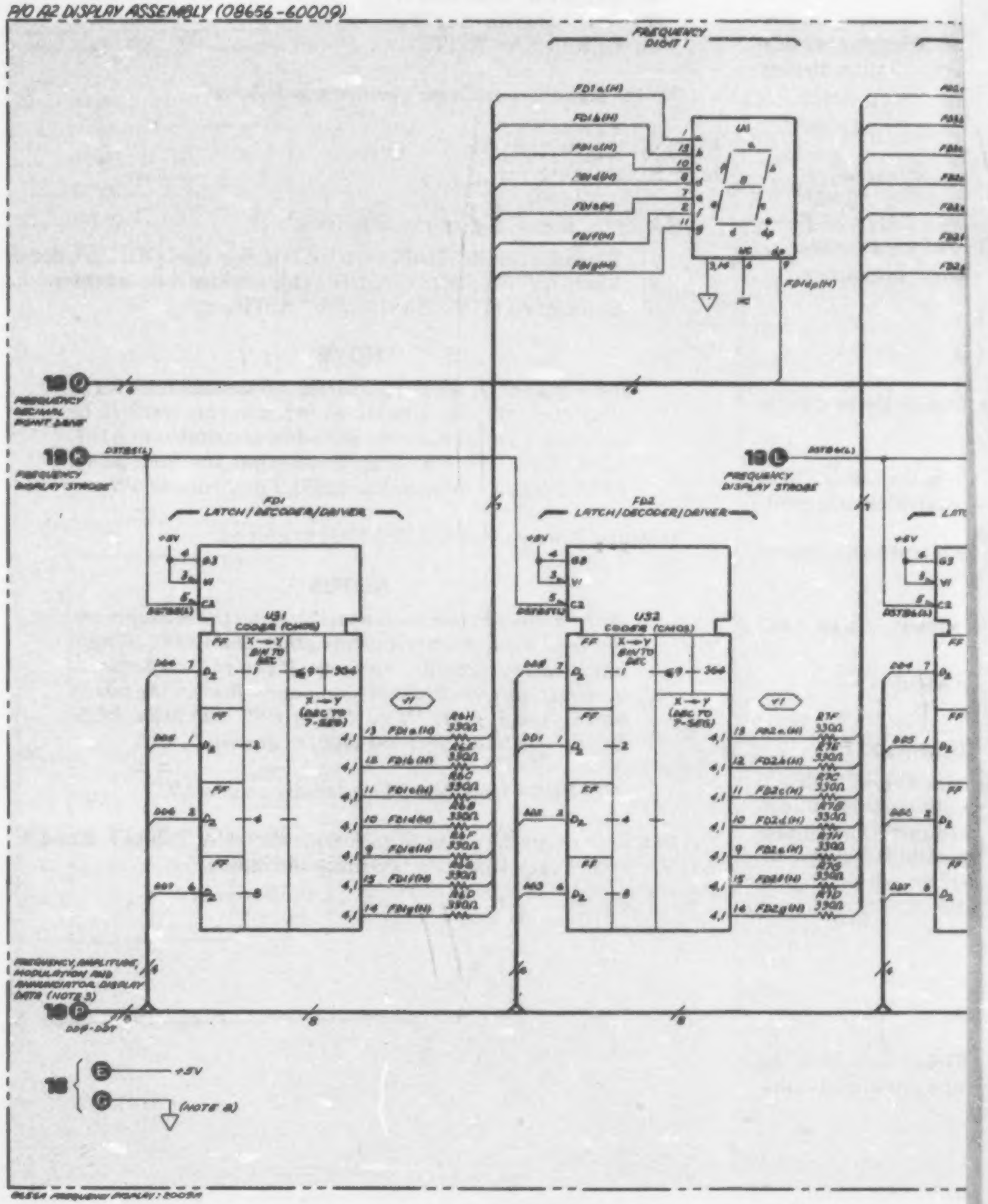
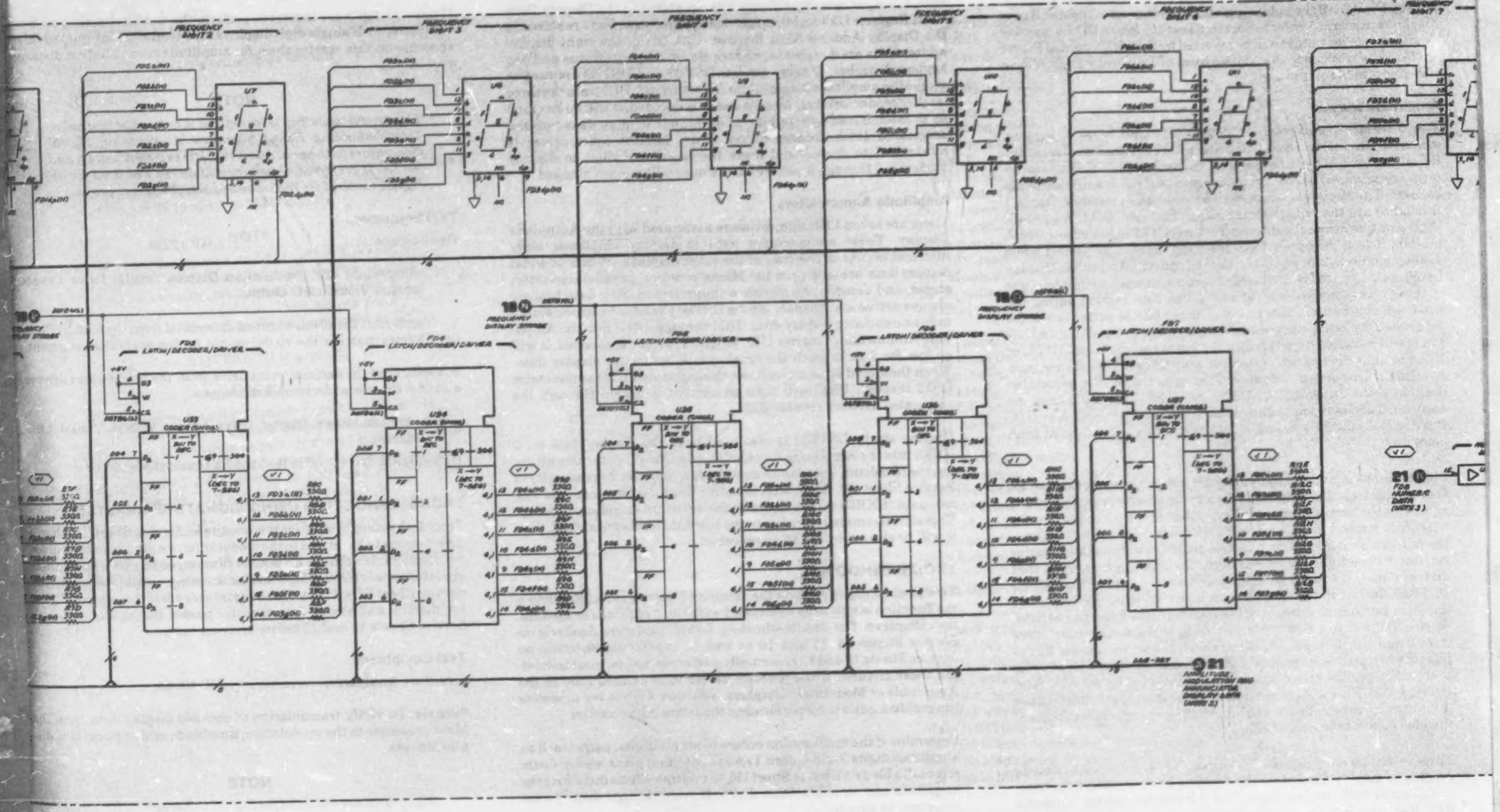
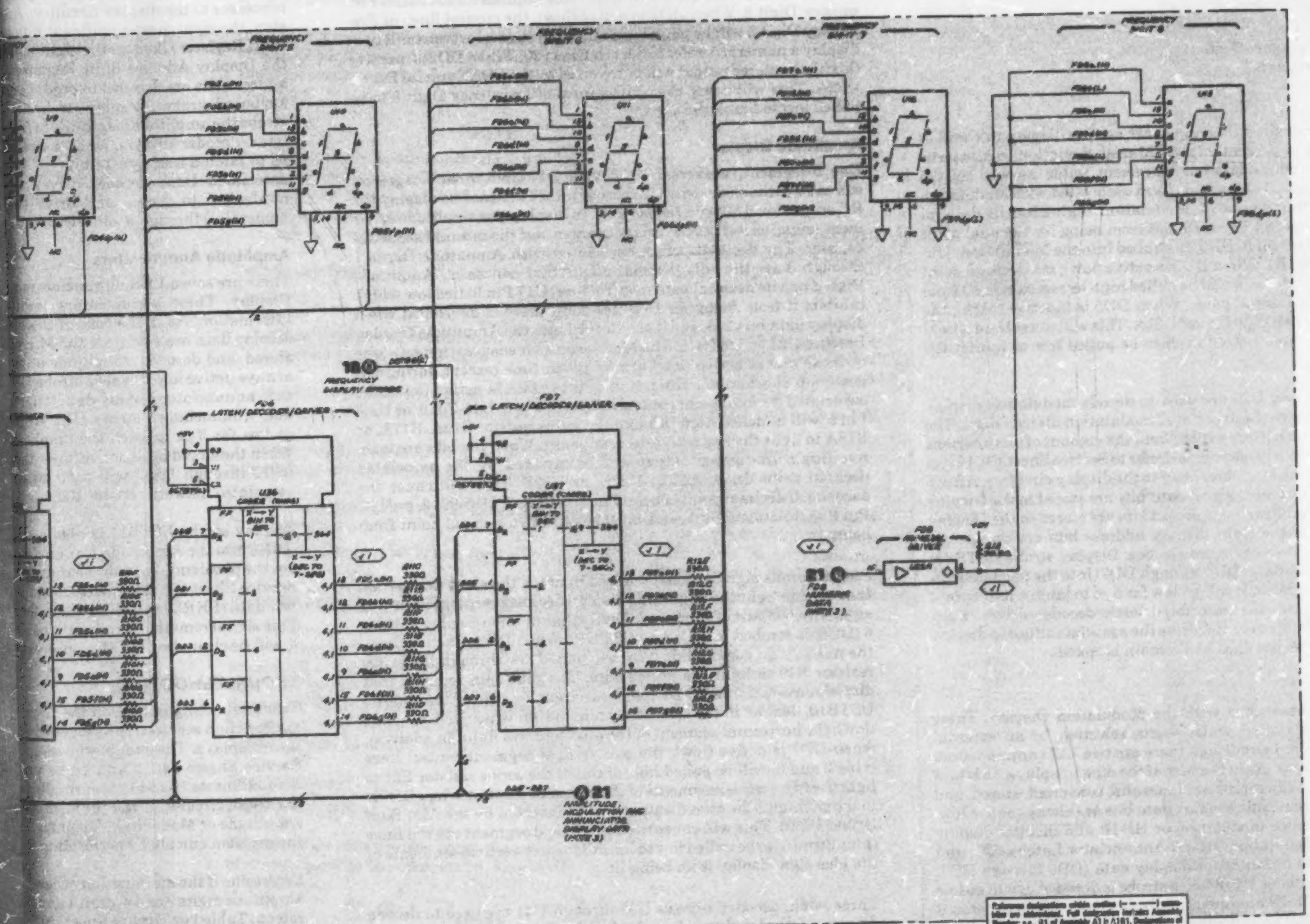

STROBES
AMPL
MODE
FREQ
CONTROL STROBE
CONTROL
AMPLITUDE, MODULATION AND ANNUNCIATOR DISPLAYS
SS21
FREQUENCY DISPLAY
SS20
DISPLAY CONTROL
SS19
MICROPROCESSOR
SS14
ADDRESS BUFFERING AND DECODING, SERIAL I/O AND CONTROL
SS15
FD8 NUMERIC DATA
DECIMAL POINT DRIVE
ADDRESS BUS
DATA BUS
DISPLAY DATA BUS
SERIAL DATA/CLOCK
FREQUENCY DIGITS
FD 1
FD 2
FD 3
FD 4
FD 5
FD 6
FD 7
FD 8
FREQUENCY DECIMAL POINT DRIVE
19
FREQ. DISPLAY STROBE
19
STROBE 19
STROBE 19
STROBE 19
DSTB 5
DSTB 6
DSTB 7
DSTB 8
21
FD8 NUMERIC DATA
DATA DD4-DD7
DATA DD0-DD3
DD0-DD7
DD0-DD7
19
FREQ., AMPLITUDE, MODULATION AND ANNUNCIATOR DISPLAY DATA
21
AMPLITUDE, MODULATION, AND/ ANNUNCIATOR DISPLAY DATA
LATCH/DECODER/DRIVER
20

Figure 8-105. Frequency Displays Block Diagrams


P/O A2 DISPLAY ASSEMBLY (08656-60009)
FREQUENCY DIGIT 1
FD1a(H)
FD1b(H)
FD1c(H)
FD1d(H)
FD1e(H)
FD1f(H)
FD1g(H)
FD1dp(H)
19
FREQUENCY DECIMAL POINT DRIVE
19
FREQUENCY DISPLAY STROBE
DSTB5(L)
FD1 LATCH/DECODER/DRIVER
+5V
U31 CODER (CMOS)
X→Y BIN TO DEC
X→Y (DEC TO 7-SEG)
330Ω
19
FREQUENCY DISPLAY STROBE
DSTB6(L)
FD2 LATCH/DECODER/DRIVER
U32 CODER (CMOS)
FD2a(H)
FD2b(H)
FD2c(H)
FD2d(H)
FD2e(H)
FD2f(H)
FD2g(H)
FREQUENCY, AMPLITUDE, MODULATION AND ANNUNCIATOR DISPLAY DATA (NOTE 3)
19
DD0-DD7
18
+5V
(NOTE 2)
8656A FREQUENCY DISPLAY 2009A


FREQUENCY DIGIT 2
FREQUENCY DIGIT 3
FREQUENCY DIGIT 4
FREQUENCY DIGIT 5
FREQUENCY DIGIT 6
FREQUENCY DIGIT 7
U7
U8
U9
U10
U11
FD2a(H)
FD2b(H)
FD2c(H)
FD2d(H)
FD2e(H)
FD2f(H)
FD2g(H)
FD2dp(H)
FD1dp(H)
FD3dp(H)
FD4dp(H)
FD5dp(H)
FD6dp(H)
FD7a(H)
FD7b(H)
FD7c(H)
FD7d(H)
FD7e(H)
FD7f(H)
FD7g(H)
3,14
NC
18 FREQUENCY DISPLAY STROBE
18 N FREQUENCY DISPLAY STROBE
FD3 LATCH/DECODER/DRIVER
FD4 LATCH/DECODER/DRIVER
FD5 LATCH/DECODER/DRIVER
FD6 LATCH/DECODER/DRIVER
FD7 LATCH/DECODER/DRIVER
+5V
U33 CODER (CMOS)
U34 CODER (CMOS)
U35 CODER (CMOS)
U36 CODER (CMOS)
U37 CODER (CMOS)
FF
X→Y BIN TO BCD
X→Y (BCD TO 7-SEG)
330Ω
R12E
R12C
R12F
R12H
R12G
R12D
R12B
ADB-AD7
21 AMPLITUDE, MODULATION AND ANNUNCIATOR DISPLAY DATA (NOTE 3)
21 FD8 NUMERIC DATA (NOTE 3)


FREQUENCY DIGIT 5
FREQUENCY DIGIT 6
FREQUENCY DIGIT 7
FREQUENCY DIGIT 8
U9
U10
U11
U12
U13
18 DSP8(L)
FREQUENCY DISPLAY STROBE
FD6 LATCH/DECODER/DRIVER
FD7 LATCH/DECODER/DRIVER
U36 CODER (CMOS)
U37 CODER (CMOS)
X→Y BIN TO DEC
X→Y (DEC TO 7-SEG)
FD8 ANNUNCIATOR DRIVER
U22A
21 FD8 NUMERIC DATA (NOTE 3)
DD0-DD7
21 AMPLITUDE, MODULATION AND ANNUNCIATOR DISPLAY DATA (NOTE 3)
330Ω
+5V

Reference designations within outline (— — —) are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A2J1-1 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. DISPLAY DATA BUS (DD0-DD7) IS POSITIVE TRUE FOR NUMERIC DATA, EXCEPT FOR FD8.

   DISPLAY DATA BUS (DD0-DD7) IS NEGATIVE TRUE FOR FD8 NUMERIC, DECIMAL POINT, SIGN AND ANNUNCIATOR DATA.

REFERENCE DESIGNATIONS

A2
R6-13 U6-13,22, 31-37

LOGIC LEVELS

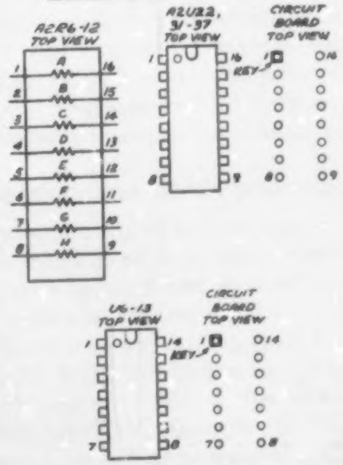
	TTL	CMOS
HIGH	>2V	>3.5V
LOW	<0.8V	<1.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
A2	
U6-13	1990-0592
U22	1820-2186
U31-37	1820-1413

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U22	+5V - 16 ▽ - 1
U31-37	+5V - 16 ▽ - 8


A2R6-12 TOP VIEW
A2U22, 31-37 TOP VIEW
CIRCUIT BOARD TOP VIEW
U6-13 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY

20
P/O A2

Figure 8-106. Frequency Displays Schematic Diagram

SERVICE SHEET 21
P/O A2 DISPLAY ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD4
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

Modulation Display

Two 7-segment, common-cathode devices U4 and U5 are used to display the level of modulation, either the AM depth in percent or the FM peak deviation in kilohertz. They are also used to display the modulation increment value as well as the internally-set decimal HP-IB address. The decimal point associated with Modulation Digit 1 is the only decimal point that can be lit. Modulation Digit 2 has its decimal point control line (U5-Pin 9) tied low which inhibits it from being lit. Decimal point drive is developed when display data bit 5 (DD5) is strobed into the Modulation/HP-IB Annunciator Latches U1 by DSTB1. When DD5 is active (low), the decimal point control line of Modulation Digit 1 (U4-Pin 9) will be pulled high by resistor R14B from the +5V power supply to light the decimal point. When DD5 is inactive (high), the stored output will be inverted by the MD1 dp Driver U21A. This will cause the decimal point control line of Modulation Digit 1 (U4-Pin 9) to be pulled low to inhibit the decimal point from being lit.

Two Latch/Decoder/Drivers U27 and U29 are used to decode modulation display data, store the decoded data, and drive the associated modulation display digit. The associated resistor networks R14 and R16 are used to limit the amount of drive current applied to the display digit. As previously mentioned (refer to Service Sheet 19), 16 bits of serial display data are sent from the Microprocessor to the display circuitry. After a serial-to-parallel conversion, the eight most-significant bits are stored in the Display Data Shift Register U23 and the eight least-significant bits are stored in the Display Address Shift Register U24. Six of the eight display address bits are decoded to produce eleven display strobes and two keyboard strobes. Display strobe DSTB3 is used to strobe the modulation display data (DD0 through DD7) into the two latch/decoder/drivers. When the strobe is decoded, it will go low for 5 μs to latch a half byte (4 bits) of modulation display data into the associated latch/decoder/driver. Each latch/decoder/driver is hard-wired to decode and drive the associated digit to display only numerals 0 through 9 (otherwise the digit will remain blanked).

Modulation/HP-IB Annunciators

There are ten LED annunciators associated with the Modulation Display. These annunciators light to indicate modulation units, source selection, or an external source over or under range condition. In addition, there are two LED annunciators used to indicate remote operation status. As in the case of the other displays, 16 bits of serial display data are sent from the Microprocessor, parallel converted, stored, and decoded. Modulation and HP-IB annunciator display data bits are always active low. Display strobe DSTB1 is used to strobe modulation or HP-IB annunciator display data (DD3 through DD7) into the Modulation/HP-IB Annunciator Latches U1, and DSTB2 is used to strobe modulation annunciator display data (DD0 through DD7) into the Modulation Annunciator Latches U2. When a strobe is decoded, it will go low for 5 μs to latch the modulation or HP-IB annunciator display data. When the stored bit is active (low), the associated LED annunciator DS1 through DS12 will light as current is drawn through the associated network resistor R15.

SERVICE SHEET 21 (Cont'd)

Display strobe DSTB1 is also used to strobe display data bit 2 (DD2) into the Modulation/HP-IB Annunciator Latches U1 to control Frequency Digit 8. When DD2 is active (low), the control lines of Frequency Digit 8 will be pulled high through the series resistor R13 to display a numeral 5 (refer to Service Sheet 20). When DD2 is inactive (high), the stored output will be inverted by the FD8 Numeral Driver U22A. This will cause the control lines of Frequency Digit 8 to be pulled low to blank the digit.

Amplitude Display

One 5-segment, universal +1 device U14 and three 7-segment, common-cathode devices U15 through U17 are used to display the RF output level. They are also used to display the amplitude increment value, as well as the current contents of the internal sequence counter. The decimal points associated with Amplitude Digits 1 through 3 are the only decimal points that can be lit. Amplitude Digit 4 has its decimal point control line (U17-Pin 9) tied low which inhibits it from being lit. Decimal point drive is developed when display data bits 2, 3, and 4 are strobed into the Amplitude Display Latches U38 by DSTB10. The Microprocessor ensures that only one of these bits is active (low) at any given time (except during the power-up subroutine). When one of these bits is active (low), the associated decimal point control line (U14-Pin 8, U15-Pin 9, or U16-Pin 9) will be pulled high through the series resistor R12A, R17A, or R18A to light the respective decimal point. When the bits are inactive (high) the stored output will be inverted by the associated decimal point driver U22D, U22E, or U22F. This will cause the associated decimal point control line (U14-Pin 8, U15-Pin 9, or U16-Pin 9) to be pulled low to inhibit the respective decimal point from being lit.

Plus or minus sign drive is produced in much the same manner as that used to light the amplitude display decimal points. The minus sign, which is part of Amplitude Digit 1, lights when display data bit 6 (DD6) is strobed into U38 by DSTB10. When DD6 is active (low), the minus sign control line (pin 4) is pulled low through the series resistor R19 to light the minus sign. The plus sign requires that display data bits 6 and 7 (DD6 and DD7) both be strobed into U38 by DSTB10. Just as in the case of the minus sign when DD6 is active (low), the horizontal segment of the plus sign will light. In addition, when DD7 is active (low), the two vertical segment control lines (pins 2 and 6) will be pulled high through the series resistor R21 to light the two vertical segments of the plus sign display. When DD7 is inactive (high), the stored output will be inverted by the AD1 Sign Driver U22B. This will cause the two vertical segment control lines (pins 2 and 6) to be pulled low to inhibit the two vertical segments of the plus sign display from being lit.

Three latch/decoder/drivers U39 through U41 are used to decode amplitude display data, store the decoded data, and drive the associated amplitude display digit. The associated resistor networks R17, R18, and R23 are used to limit the amount of drive current applied to the display digit. As previously mentioned (refer to Service Sheet 19), 16 bi
processor to the dis
sion, the eight most
Shift Register U23
the Display Addres
address bits are dec
keyboard strobes. D
strobe the amplitud
latch/decoder/driv
μs to latch a half b
associated latch/d
hard-wired to deco
numerals 0 through

Amplitude Annunc

There are seven LE
Display. These an
information. As in
display data are se
stored, and decoded
always active low.
tude annunciator d
tude Annunciator L
go low for 5 μs to
When the stored bit
DS13 through DS1
associated network

Display strobe DS
(DD0) into the Amp
keyboard column li
Service Sheet 18). W
row data (RKRD) w
This signal remains
it will be cleared by

TROUBLESHOOT

Troubleshooting is
malfunction seems
tion Displays. The
Service Sheets 14,
Service Sheets 18 ar
ing these circuits.
Amplitude or Modu
the problem quickly

Determine if the m
amplitude digits 3 a
refer to Table 1 on S
amplitude and/or r
incorrect, be sure to
1. perform the Tro
vice Sheets 14, 15 a

SERVICE SHEET 21 (Cont'd)

vice Sheet 19), 16 bits of serial display data are sent from the Microprocessor to the display circuitry. After a serial-to-parallel conversion, the eight most-significant bits are stored in the Display Data Shift Register U23 and the eight least-significant bits are stored in the Display Address Shift Register U24. Six of the eight display address bits are decoded to produce eleven display strobes and two keyboard strobes. Display strobes DSTB8 and DSTB9 are used to strobe the amplitude display data (DD0 through DD7) into the three latch/decoder/drivers. When a strobe is decoded, it will go low for 5 μs to latch a half byte (4 bits) of amplitude display data into the associated latch/decoder/driver. Each latch/decoder/driver is hard-wired to decode and drive the associated digit to display numerals 0 through 9, otherwise the digit will remain blanked.

Amplitude Annunciators

There are seven LED annunciators associated with the Amplitude Display. These annunciators light to display amplitude units information. As in the case of the other displays, 16 bits of serial display data are sent from the Microprocessor, parallel converted, stored, and decoded. Amplitude annunciator display data bits are always active low. Display strobe DSTB11 is used to strobe amplitude annunciator display data (DD1 through DD7) into the Amplitude Annunciator Latches U42. When the strobe is decoded, it will go low for 5 μs to latch the amplitude annunciator display data. When the stored bit is active (low), the associated LED annunciator DS13 through DS19 will light as current is drawn through the associated network resistor R22.

Display strobe DSTB11 is also used to strobe display data bit 0 (DD0) into the Amplitude Annunciator Latches U42 to force all six keyboard column lines low so that the row data can be read (refer to Service Sheet 18). When DD0 is active (high), a signal to read key row data (RKRD) will be issued to the keyboard encoding circuitry. This signal remains stored until the row data has been latched, then it will be cleared by the Microprocessor.

TROUBLESHOOTING

Troubleshooting is done on the circuits of Service Sheet 21 when a malfunction seems to be associated with the Amplitude or Modulation Displays. The Troubleshooting Using Signature Analysis on Service Sheets 14, 15 and 16 as well as the Troubleshooting on Service Sheets 18 and 19 is normally performed before troubleshooting these circuits. If the problem seems to be related only to the Amplitude or Modulation Displays, you may wish to try to isolate the problem quickly by performing the following procedure.

Determine if the malfunction occurs in single digits, pairs (such as amplitude digits 3 and 4, digit 1 and the decimal point, and so forth; refer to Table 1 on Service Sheet 19), or multiple digits including the amplitude and/or modulation digits. If multiple digit displays are incorrect, be sure to:

1. perform the Troubleshooting Using Signature Analysis on Service Sheets 14, 15 and 16

SERVICE SHEET 21 (Cont'd)

2. then perform the Troubleshooting on Service Sheets 18 and 19.

If pairs of digits are incorrect, perform the troubleshooting on Service Sheet 19. If single digit displays are incorrect, continue troubleshooting on this service sheet for amplitude or modulation display problems.

NOTE

This troubleshooting information is to be used instead of Troubleshooting Using Signature Analysis on Signal Generators with serial number prefixes 2009A, 2014A and 2018A. If preferred, this information may be used for all Signal Generators regardless of serial number prefix

Test Equipment

Oscilloscope ....HP 1222A

√1 Amplitude and Modulation Display Digital Drive Levels versus Visual LED Output

1. Verify that the seven-segment drive level from the Latch/Decoder/Drivers matches the visual output for the equivalent segment.

2. Verify that the decimal point drive from the latches and drivers matches the visual decimal point output.

√2 Annunciator's Digital Drive Levels versus Visual LED Outputs

If the digital drive level is low, the LED output should be lit.

TROUBLESHOOTING USING SIGNATURE ANALYSIS

Troubleshooting is done on the circuits of Service Sheet 21 when a defect seems to be related to the modulation, amplitude or annunciator displays. If nothing definite is discovered in performing these signature analyzer checks, consider the other possibilites shown on Service Sheet BD4. If any of the signatures are incorrect, recall that the display and strobe data transfer passes through circuitry on Service Sheets 15 and 19 before arriving here.

Test Equipment

Signature Analyzer ....HP 5004A

Purpose. To verify transmission of encoded display data from the Microprocessor to the modulation, amplitude and annunciator display drivers.

NOTE

Signatures are not valid for Signal Generators with serial number prefixes of 2018A and below.

Setup. Connect the signature analyzer as follows:

SERVICE SHEET 21 (Cont'd)

1) GND to ground
2) START to 'SA5' A11TP9
3) STOP to 'SA5' A11TP9
4) CLK to 'SA4' A11TP7

Set the signature analyzer's controls as follows:

1) START-IN
2) STOP-OUT
3) CLK-IN

Set up the Signal Generator as follows:

1) Place the LOGIC/RAM switch A11S1B in the LOGIC postion.
2) Short A2TP14 'TO2' to 'GND'. This enables data transfer.
3) Connect A11TP10 'SA6' to 'SA7' A2TP1.

NOTE

If the Signal Generator's address switch has been set to other than '07', the signatures taken in this test will be incorrect. In this case, reset the address switches to A1=1, A2=1, A3=1, A4=0 and A5=0. Then set the front panel RESET-STBY-ON switch to RESET and back to ON.

Initialize. Briefly short A11TP3 NMI to ground.

NOTES

With careless probing it is possible to get the Microprocessor into a program sequence other than that portion intended for signature analysis. If the +5V signature is incorrect, this has probably happened. Restart the test by setting the RST/RUN switch to RST and then RUN. Briefly touch the NMI test point to ground.

All LEDS should be cycling rapidly on and off.

Probe. Connect the probe to each node shown in Tables 1, 2 and 3. Verify that each signature is correct and stable.

SERVICE SHEET 21 (Cont'd)

Table 1. Decoded Amplitude Signatures

Node	Correct Signature	Comments
+5V	F84P	
U38 #2	P401	AP DIG 1
U38 #5	9CA4	AP ±
U38 #7	2AFA	
U38 #10	620C	AP DP 1
U38 #12	580P	AP DP 2
U38 #15	22FC	AP DP 3
+5V	F84P	
U39 #9	UP60	AP DIG 2
U39 #10	9P35	
U39 #11	4CH5	
U39 #12	PH98	
U39 #13	AA91	
U39 #14	71F0	
U39 #15	0276	
+5V	F84P	
U41 #9	0U7H	AP DIG 4
U41 #10	7P96	
U41 #11	CH03	
U41 #12	8291	
U41 #13	180P	
U41 #14	1732	
U41 #15	19P2	

Table 2. Decoded Annunciator Signatures

Node	Correct Signature	Comments
+5V	F84P	
U1 #2	4PF5	MD DP 1
U1 #5	046A	ADRS
U1 #7	49UH	RMT
U1 #10	27FA	%
U1 #12	C73C	kHz
+5V	F84P	
U2 #2	FP81	HI EXT
U2 #5	34C1	EXT FM
U2 #6	3U35	LO EXT
U2 #9	352H	EXT AM
U2 #12	8405	1K Hz
U2 #15	AFPC	INT AM
U2 #16	UCFP	INT FM
U2 #19	4489	400 Hz
+5V	F84P	
U42 #2	3C63	dB
U42 #5	7HC8	dBf
U42 #8	FU7A	EMF
U42 #9	962P	dBm
U42 #12	P54A	RD KY WRD
U42 #15	UCU0	VOLTS
U42 #16	PHCC	mV
U42 #19	8U6F	μV

Table 3. Frequency Digit 8 Signature

Node	Correct Signature	Comments
+5V	F84P	
U1 #15	L1PO	FR DIG 8

Remove the jumpers between test points and between test point and ground. Reset the LOGIC/RAM switch to RAM.

If the HP-IB address switch was changed, reset the address switch (refer to Service Sheet 17) to the original address. Set the front panel RESET-STBY-ON switch to RESET and back to ON.

P/O A2 ASSEMBLY

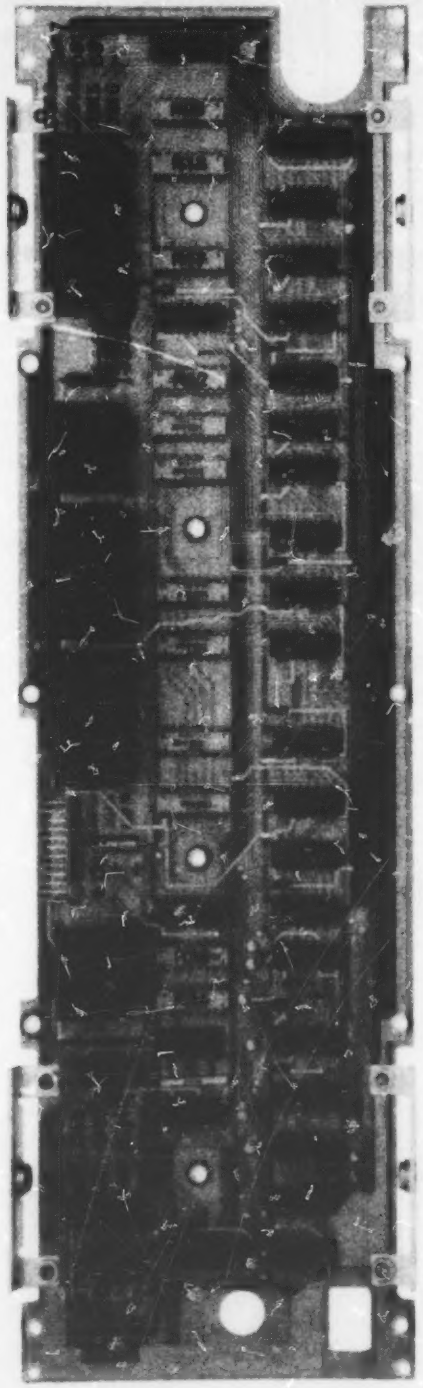
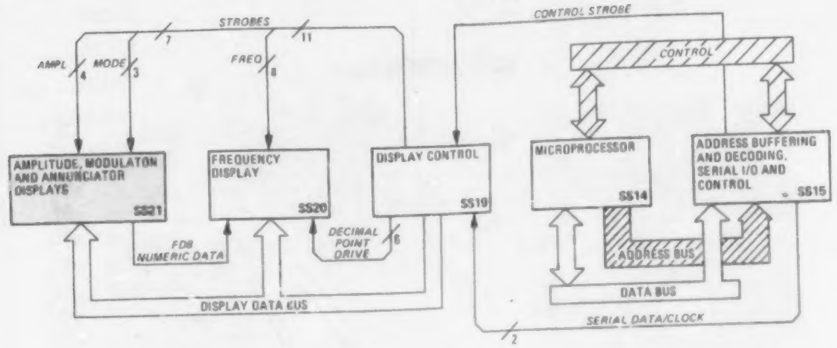


Figure 8-107. Amplitude, Modulation and Annunciator Displays Component Locations


STROBES
7
11
AMPL
4
MODE
3
FREQ
8
CONTROL STROBE
CONTROL
AMPLITUDE, MODULATON AND ANNUNCIATOR DISPLAYS
SS21
FREQUENCY DISPLAY
SS20
DISPLAY CONTROL
SS19
MICROPROCESSOR
SS14
ADDRESS BUFFERING AND DECODING, SERIAL I/O AND CONTROL
SS15
FD8 NUMERIC DATA
DECIMAL POINT DRIVE
6
ADDRESS BUS
DATA BUS
DISPLAY DATA BUS
SERIAL DATA/CLOCK
2

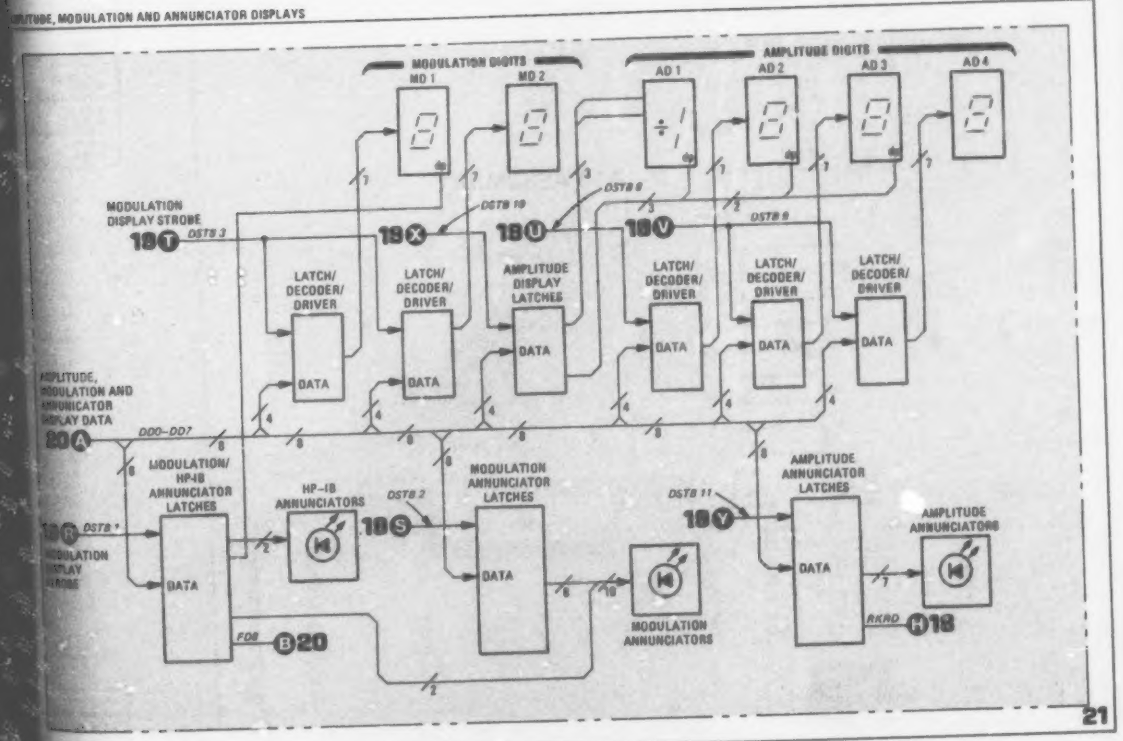
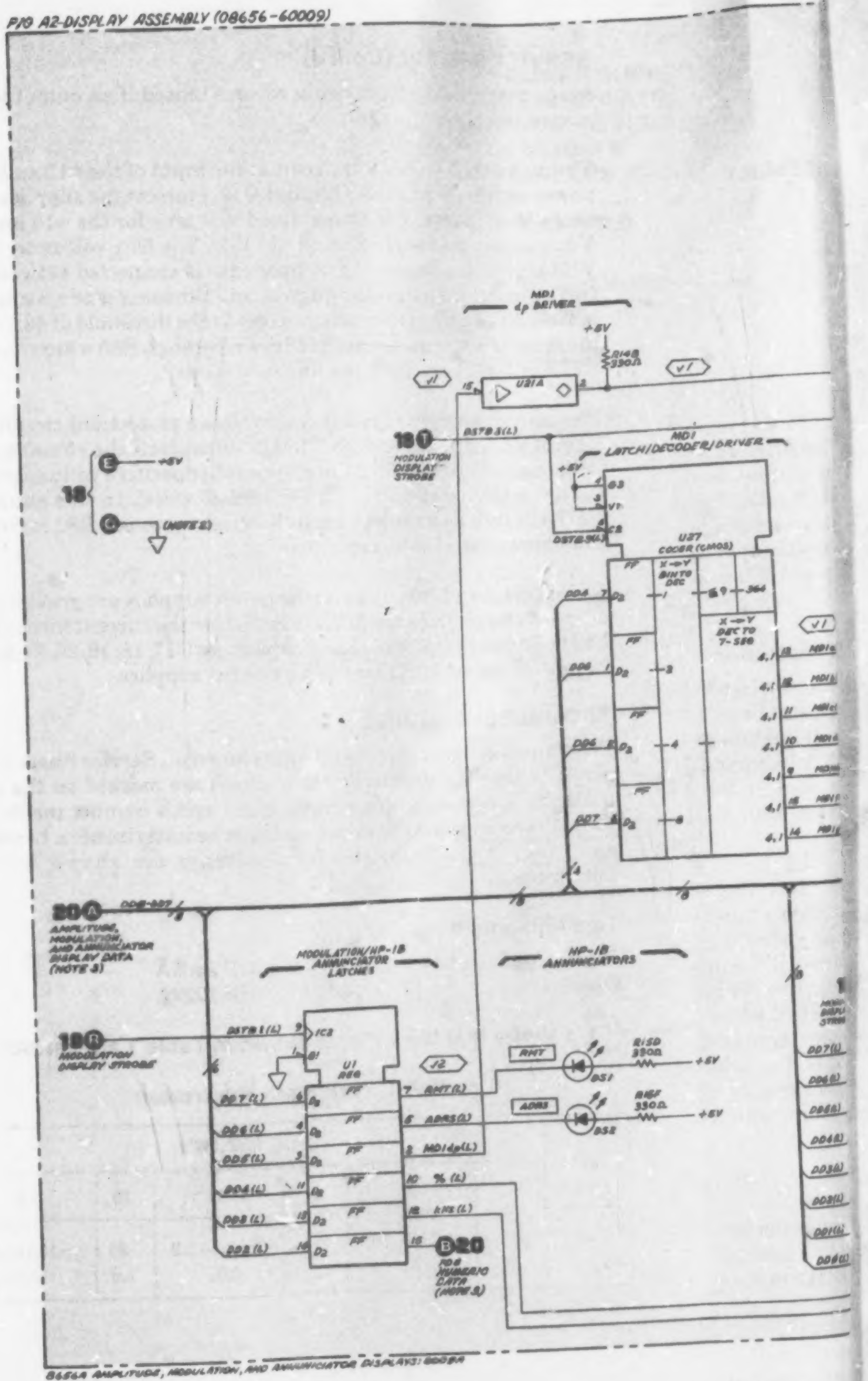
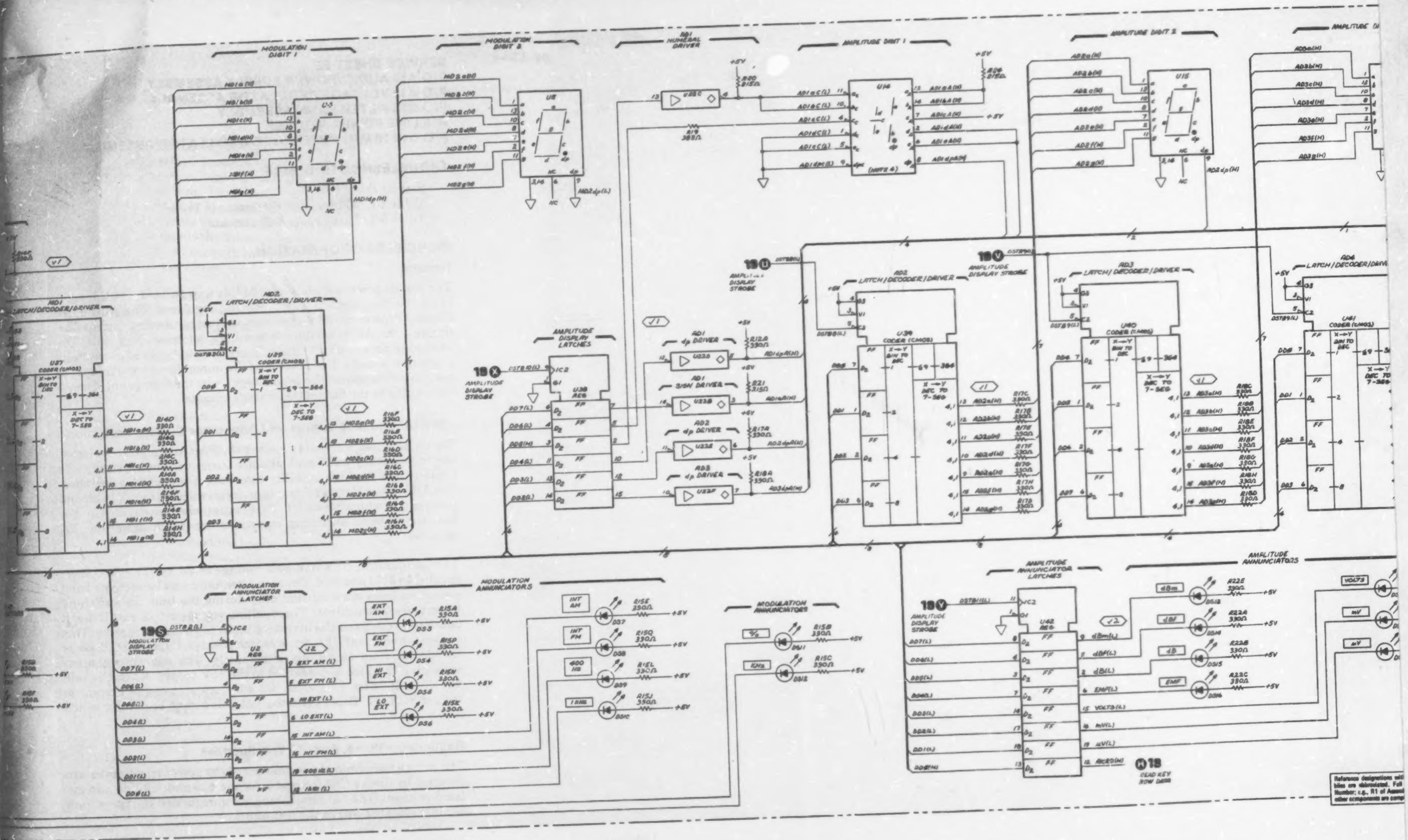
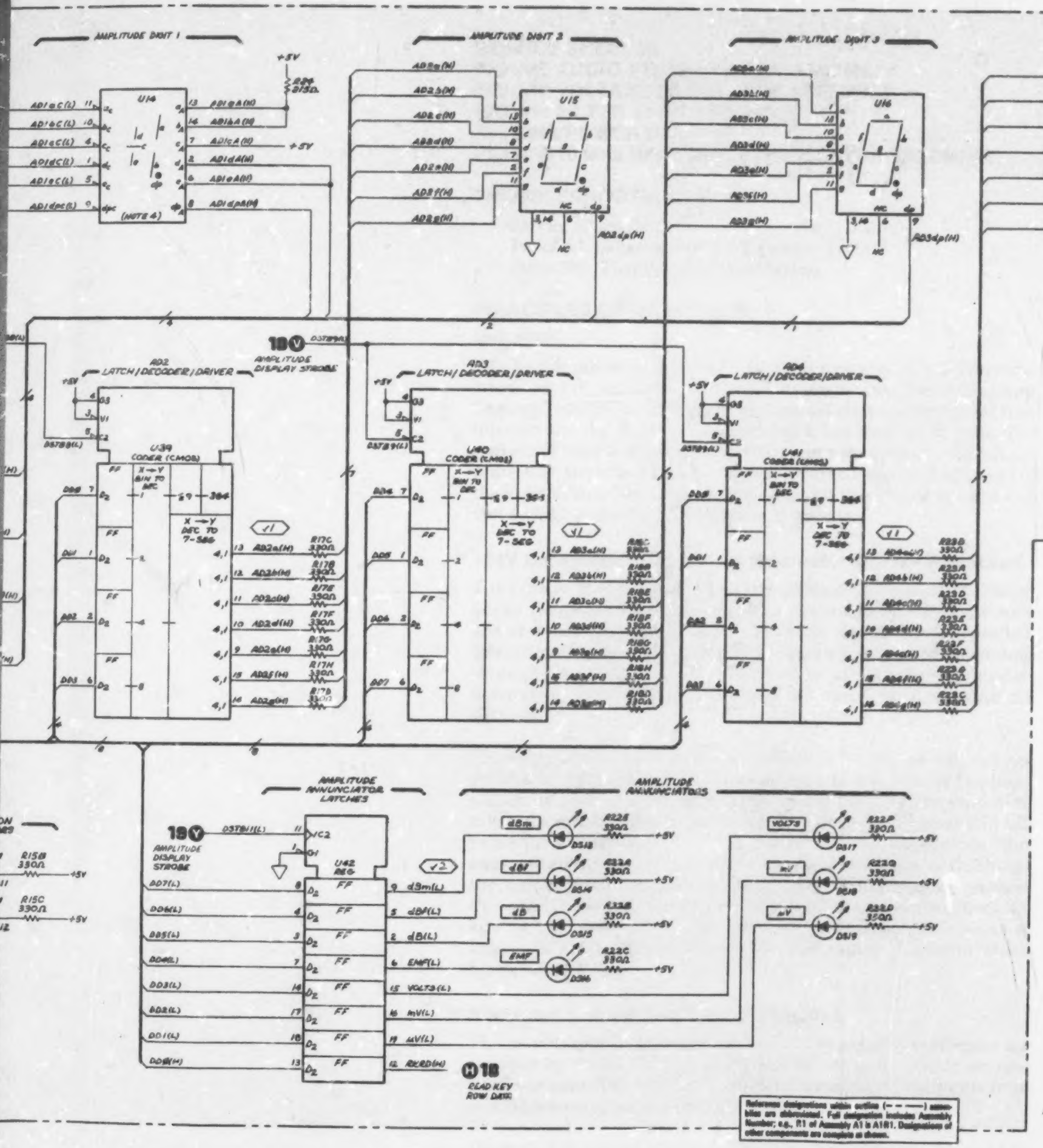

TUDE, MODULATION AND ANNUNCIATOR DISPLAYS
MODULATION DIGITS
MD 1
MD 2
AMPLITUDE DIGITS
AD 1
AD 2
AD 3
AD 4
MODULATION DISPLAY STROBE
19T
DSTB 3
19X
DSTB 10
19U
DSTB 9
19V
DSTB 8
LATCH/ DECODER/ DRIVER
AMPLITUDE DISPLAY LATCHES
DATA
AMPLITUDE, MODULATION AND ANNUNCIATOR DISPLAY DATA
20A
DD0-DD7
8
MODULATION/ HP-IB ANNUNCIATOR LATCHES
HP-IB ANNUNCIATORS
19S
DSTB 2
MODULATION ANNUNCIATOR LATCHES
MODULATION ANNUNCIATORS
19Y
DSTB 11
AMPLITUDE ANNUNCIATOR LATCHES
AMPLITUDE ANNUNCIATORS
19R
DSTB 1
MODULATION DISPLAY STROBE
FD8
B20
RKRO
H18
21

Figure 8-108. Amplitude, Modulation and Annunciator Displays Block Diagrams


P/O A2-DISPLAY ASSEMBLY (08656-60009)
MD1 dp DRIVER
+5V
R148 330Ω
U21A
V1
19T
MODULATION DISPLAY STROBE
DSTB 3(L)
MD1 LATCH/DECODER/DRIVER
U27 CODER (CMOS)
X→Y BIN TO DEC
X→Y DEC TO 7-SEG
DD4
DD5
DD6
DD7
MD1a
MD1b
MD1c
MD1d
MD1e
MD1f
MD1g
18
E
+5V
G
(NOTE 2)
20A
DD0-DD7
AMPLITUDE, MODULATION, AND ANNUNCIATOR DISPLAY DATA (NOTE 3)
MODULATION/HP-IB ANNUNCIATOR LATCHES
HP-IB ANNUNCIATORS
19R
MODULATION DISPLAY STROBE
DSTB 1(L)
U1 REG
J2
RMT
ADRS
R150 330Ω
R151 330Ω
DS1
DS2
RMT(L)
ADRS(L)
MD1dp(L)
% (L)
kHz (L)
B20
FD8 NUMERIC DATA (NOTE 3)
DD7(L)
DD6(L)
DD5(L)
DD4(L)
DD3(L)
DD2(L)
DD1(L)
DD0(L)
8656A AMPLITUDE, MODULATION, AND ANNUNCIATOR DISPLAYS: 8008A



MODULATION DIGIT 1
MODULATION DIGIT 2
AD1 NUMERAL DRIVER
AMPLITUDE DIGIT 1
AMPLITUDE DIGIT 2
AMPLITUDE DI
U3
U8
U14
U15
MD1
LATCH/DECODER/DRIVER
U27
CODER (CMOS)
MD2
LATCH/DECODER/DRIVER
U29
CODER (CMOS)
AMPLITUDE DISPLAY LATCHES
18X
AMPLITUDE DISPLAY STROBE
U38
REG
AD1 dp DRIVER
AD1 SIGN DRIVER
AD2 dp DRIVER
AD3 dp DRIVER
18U
AMPLITUDE DISPLAY STROBE
18V
AMPLITUDE DISPLAY STROBE
AD2
LATCH/DECODER/DRIVER
U39
CODER (CMOS)
AD3
LATCH/DECODER/DRIVER
U40
CODER (CMOS)
AD4
LATCH/DECODER/DRIVER
U41
CODER (CMOS)
X→Y BIN TO DEC
X→Y DEC TO 7-SEG
18S
MODULATION DISPLAY STROBE
MODULATION ANNUNCIATOR LATCHES
U2
REG
MODULATION ANNUNCIATORS
EXT AM
EXT FM
HI EXT
LO EXT
INT AM
INT FM
400 Hz
1 kHz
%
kHz
18Y
AMPLITUDE DISPLAY STROBE
AMPLITUDE ANNUNCIATOR LATCHES
U42
REG
AMPLITUDE ANNUNCIATORS
dBm
dBf
dB
EMF
VOLTS
mV
µV
H18
READ KEY ROW DATA
+5V
330Ω
215Ω
383Ω
Reference designations within ... are abbreviated. Full ... Number; e.g., R1 of Assem... other components are comp...


AMPLITUDE DIGIT 1
AMPLITUDE DIGIT 2
AMPLITUDE DIGIT 3
AMPLITUDE DIGIT 4
U14
(NOTE 4)
U15
U16
U17
+5V
R24 215Ω
AD1aC(L)
AD1bC(L)
AD1cC(L)
AD1dC(L)
AD1eC(L)
AD1dpC(L)
AD1aA(H)
AD1bA(H)
AD1cA(H)
AD1dA(H)
AD1eA(H)
AD1dpA(H)
AD2a(H)
AD2b(H)
AD2c(H)
AD2d(H)
AD2e(H)
AD2f(H)
AD2g(H)
AD2dp(H)
AD3dp(H)
AD4dp(H)
NC
19V
DSTB9(L)
AMPLITUDE DISPLAY STROBE
AD2 LATCH/DECODER/DRIVER
AD3 LATCH/DECODER/DRIVER
AD4 LATCH/DECODER/DRIVER
U39 CODER (CMOS)
U40 CODER (CMOS)
U41 CODER (CMOS)
FF
X→Y BIN TO DEC
X→Y DEC TO 7-SEG
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
R17C 330Ω
R17B 330Ω
R17E 330Ω
R17F 330Ω
R17G 330Ω
R17H 330Ω
R17D 330Ω
R18C 330Ω
R23D 330Ω
AMPLITUDE ANNUNCIATOR LATCHES
AMPLITUDE ANNUNCIATORS
19Y
AMPLITUDE DISPLAY STROBE
DSTB11(L)
U42 REG
DD7(L)
DD6(L)
DD5(L)
DD4(L)
DD3(L)
DD2(L)
DD1(L)
DD0(H)
dBm(L)
dBf(L)
dB(L)
EMF(L)
VOLTS(L)
mV(L)
μV(L)
RKRD(H)
18H
READ KEY ROW DATA
dBm
dBf
dB
EMF
VOLTS
mV
μV
DS13
DS14
DS15
DS16
DS17
DS18
DS19
R22E 330Ω
R22A 330Ω
R22B 330Ω
R22C 330Ω
R22F 330Ω
R22G 330Ω
R22D 330Ω
R15B 330Ω
R15C 330Ω

Reference designations within outline (– – ——) assemblies are abbreviated. Full designation includes Assembly Number, e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. CHASSIS GROUND IS ACHIEVED THROUGH A2J1-1 CONNECTION AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
3. DISPLAY DATA BUS (DD0-DD7) IS POSITIVE TRUE FOR NUMERIC DATA, EXCEPT FOR FDB.

   DISPLAY DATA BUS (DD0-DD7) IS NEGATIVE TRUE FOR FDB NUMERIC, DECIMAL POINT, SIGN AND ANNUNCIATOR DATA.
4. NUMERIC SEGMENT ANODES ARE INDICATED BY SUBSCRIPT "A" AND CATHODES BY SUBSCRIPT "C" AS FOLLOWS:

$$a_C \longrightarrow\!\!|\!\!\longleftarrow a_A$$

REFERENCE DESIGNATIONS

A2
DS1-19 R12,14-29 U1,2,4,5,14-17, 21,22,27,29, 38-42

LOGIC LEVELS

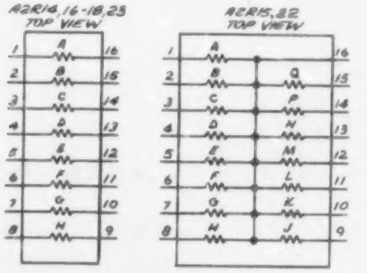
	TTL	CMOS
HIGH	>2V	>3.5V
LOW	<0.8V	<1.5V
< IS MORE NEG. THAN > IS MORE POS. THAN		
OPEN	HIGH	UNDEF.
GROUND	LOW	LOW

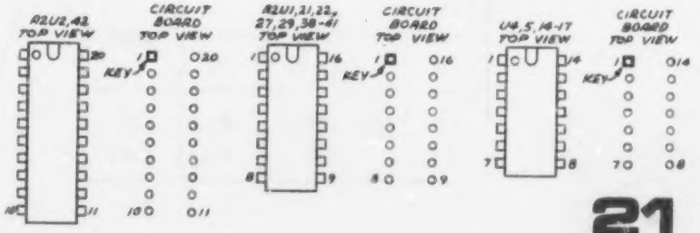
INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
A2	
U1,38	1820-2086
U2,42	1820-1858
U4,5,15-17	1990-0592
U14	1990-0681
U21-22	1820-2186
U27,29,39-41	1820-1413

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
A2	
U1,27,29,38-41	+5V - 16 ▽ - 8
U2,42	+5V - 20 ▽ - 10
U21,22	+5V - 16 ▽ - 1


A2R14,16-18,23 TOP VIEW
A2R15,22 TOP VIEW
A
B
C
D
E
F
G
H
J
K
L
M
N
P
Q


A2U2,42 TOP VIEW
CIRCUIT BOARD TOP VIEW
A2U1,21,22,27,29,38-41 TOP VIEW
CIRCUIT BOARD TOP VIEW
U4,5,14-17 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY

21
P/O A2

Figure 8-109. Amplitude, Modulation and Annunciator Displays Schematic Diagram

SERVICE SHEET 22
P/O A10 AUDIO/POWER SUPPLY ASSEMBLY
P/O A12 VOLTAGE REGULATOR ASSEMBLY
P/O A14 FILTER BANK ASSEMBLY
A15 LINE POWER MODULE
P/O A16 10 MHz REFERENCE OSCILLATOR ASSEMBLY

TROUBLESHOOTING HELP

Service Sheet BD1
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustments

PRINCIPLES OF OPERATION

General

The four dc power supplies are +24 Vdc unregulated, +15 Vdc regulated, +5 Vdc regulated and −15 Vdc regulated. The Attenuator Current Protection circuit protects against continuing current flow through the A9 Attenuator Assembly's latching relay coils. The switching time is about 60 ms. There are two types of overvoltage protection circuits. The first limits the unregulated voltage input to the ±15 volt supplies. The second type limits the voltage out of the +5 volt supply to the Signal Generator's circuits.

+24V Unregulated Supply and Attenuator Current Protection

The unregulated +24 volts switches the Step Attenuator, the Heterodyne frequency band and supplies current to the crystal oven's heater when the high stability time base, Option 001 is installed. The Attenuator Current Protection circuit will short +24V to ground through Q1 which blows F1. This occurs when attenuator and or heterodyne band switching current is drawn for more than 2.2 seconds.

The comparator, U2's reference voltage is set by the +24 voltage divided by R73 and R74. The step attenuator and heterodyne band switching coils draw current only during the time the switching takes place (about 60 ms). The resulting voltage drop across R75 will cause the voltage at the inverting input to go more negative. This causes the output of U2 to try to switch positive. Capacitor C22 keeps the output from switching immediately. The capacitor charges through R72 which is connected to the +5V supply. When the voltage on C22 nears +1.4 volts, Q2 will conduct enough current to trigger SCR Q1. This shorts the +24 volt supply to ground which blows fuse F1.

Regulated +15, +5, and −15 Volt Supplies

The ac voltages from the secondary of the power transformer are rectified by diodes CR6,7,8 and 9 for the +15 and −15 Vdc unregulated voltages. The +5 volts dc supply's unregulated voltage is from rectifiers located within the rear panel.

Diodes CR12, 13 and 14 protect the series regulators, U1, U2 and U3. If the output voltage of the series regulators goes more positive than the unregulated input voltage the diodes will be turned on. This keeps the regulators from being reverse biased if an output is connected to a higher voltage.

The overvoltage protection circuit at the input of the +15 and −15V power supplies (VR5, R65, C21 and Q12) protects the supplies from excess line voltage. The unregulated voltages for the +15 and −15 Vdc supplies are about +25 and −25 Vdc. The 68.1 volt zener diode VR5 and its accompanying components is connected between the two supplies. The normal voltage across the zener diode is approximately 50 Vdc. When the voltage exceeds the threshold of 68.1 volts, the zener will turn on. Current is drawn through R65 which charges C21 until Q12 fires. Then the line fuse blows.

The +5 Vdc supply's crowbar (overvoltage protection) circuit consists of VR6, R80, R81 and Q3. The circuit protects the +5 volt supply if it is shorted to the +15 Vdc supply or other positive voltage greater than the threshold voltage of VR6 (+8.25 volts). In this situation, VR6 will turn on and draw enough current through R80 to fire Q3. This blows the +5 volt supply fuse.

LEDs DS1,2 and 3 are lit when the power supplies are providing an output voltage. Resistors R82, 83 and 84 set the current through the LEDs. Inductors L1, 2 and 3 and capacitors C17, 18, 19, 23, 24, 25, 26, 27 and 28 isolate and filter the associated supplies.

TROUBLESHOOTING

Procedures for checking the circuits shown on Service Sheet 22 are given below. The area or points to check are marked on the schematic by a hexagon with a check mark and a number inside, e.g. ⟨√3⟩. Fixed voltages are shown on the schematic inside a hexagon, e.g. ⟨2V±0.2V⟩. Transistor bias voltages are shown without tolerances.

Test Equipment

Digital Multimeter	HP 3465A
Oscilloscope	HP 1222A

⟨√1⟩ Verify that the voltages shown in Table 1 are correct.

Table 1. Power Suppiy Measurements

Volts	On test point J6-Pin:					
	11	13	9	3	10	2
Vdc Vp-p	+25 1.0	+17 to +13 0.01	+11 1.5	+5.6 to +5.2 0.01	−25 1.0	−13 to −17 0.01

Amplitude, Modulation and Annunciator Displays
P/O A2
SERVICE SHEET 21

everse biased if an output is con-

at the input of the +15 and −15V
d Q12) protects the supplies from
ted voltages for the +15 and −15
25 Vdc. The 68.1 volt zener diode
onents is connected between the
across the zener diode is approxi-
xceeds the threshold of 68.1 volts,
rawn through R65 which charges
fuse blows.

ervoltage protection) circuit con-
circuit protects the +5 volt supply
y or other positive voltage greater
6 (+8.25 volts). In this situation,
h current through R80 to fire Q3.

power supplies are providing an
nd 84 set the current through the
pacitors C17, 18, 19, 23, 24, 25, 26,
ociated supplies.

ts shown on Service Sheet 22 are
check are marked on the sche-
mark and a number inside, e.g.
the schematic inside a hexagon,
voltages are shown without

...HP 3465A
...HP 1222A

own in Table 1 are correct.

ly Measurements

st point J6-Pin:		
3	10	2
+5.6 to +5.2 0.01	−25 1.0	−13 to −17 0.01

A12 ASSEMBLY

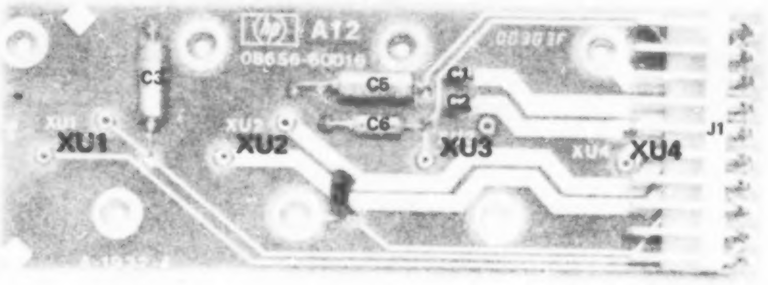


Figure 8-110. Voltage Regulator Component Locations

A14 ASSEMBLY

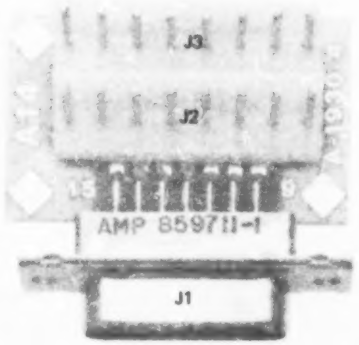


Figure 8-111. Filter Bank Component Locations

P/O A10 ASSEMBLY

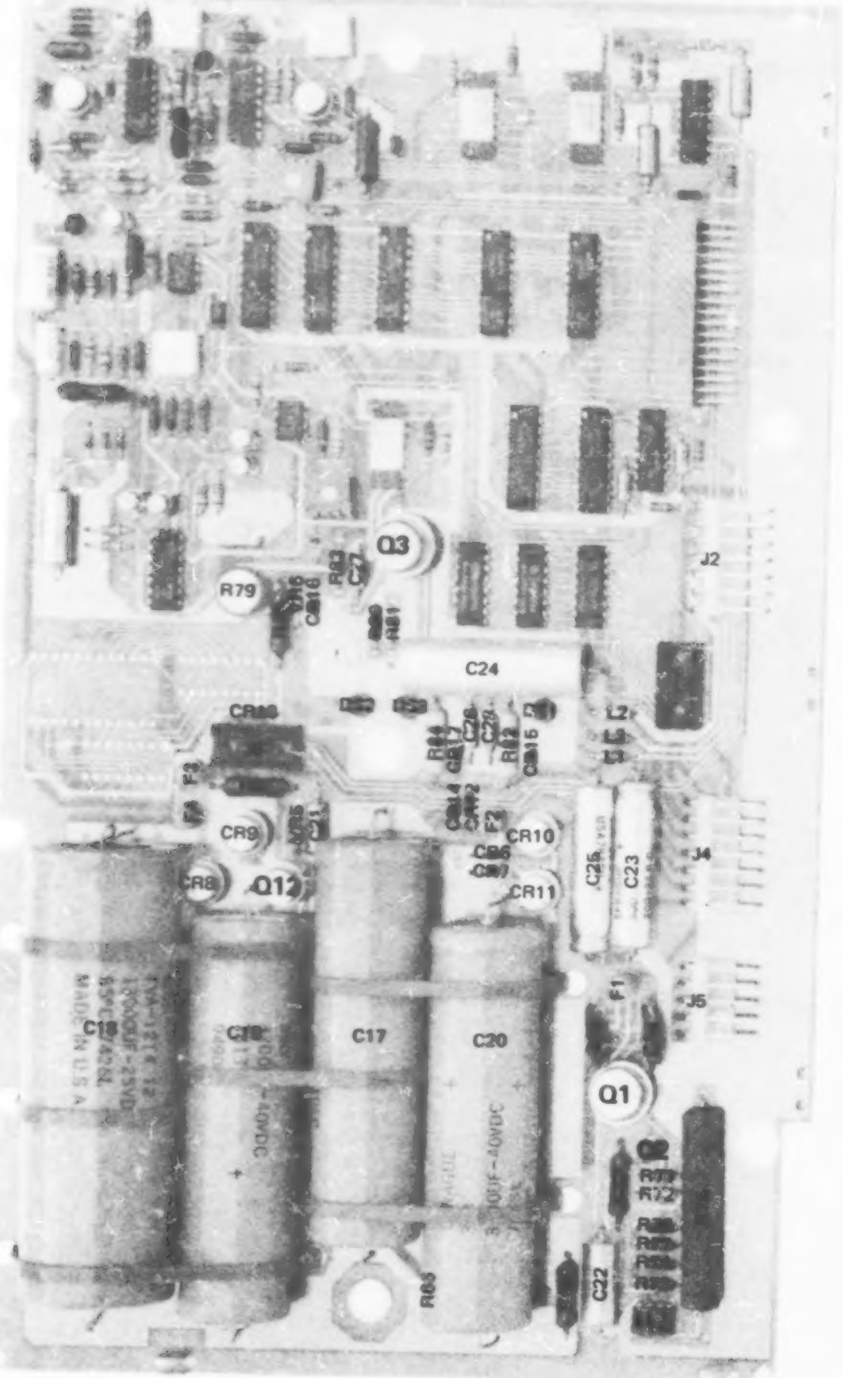
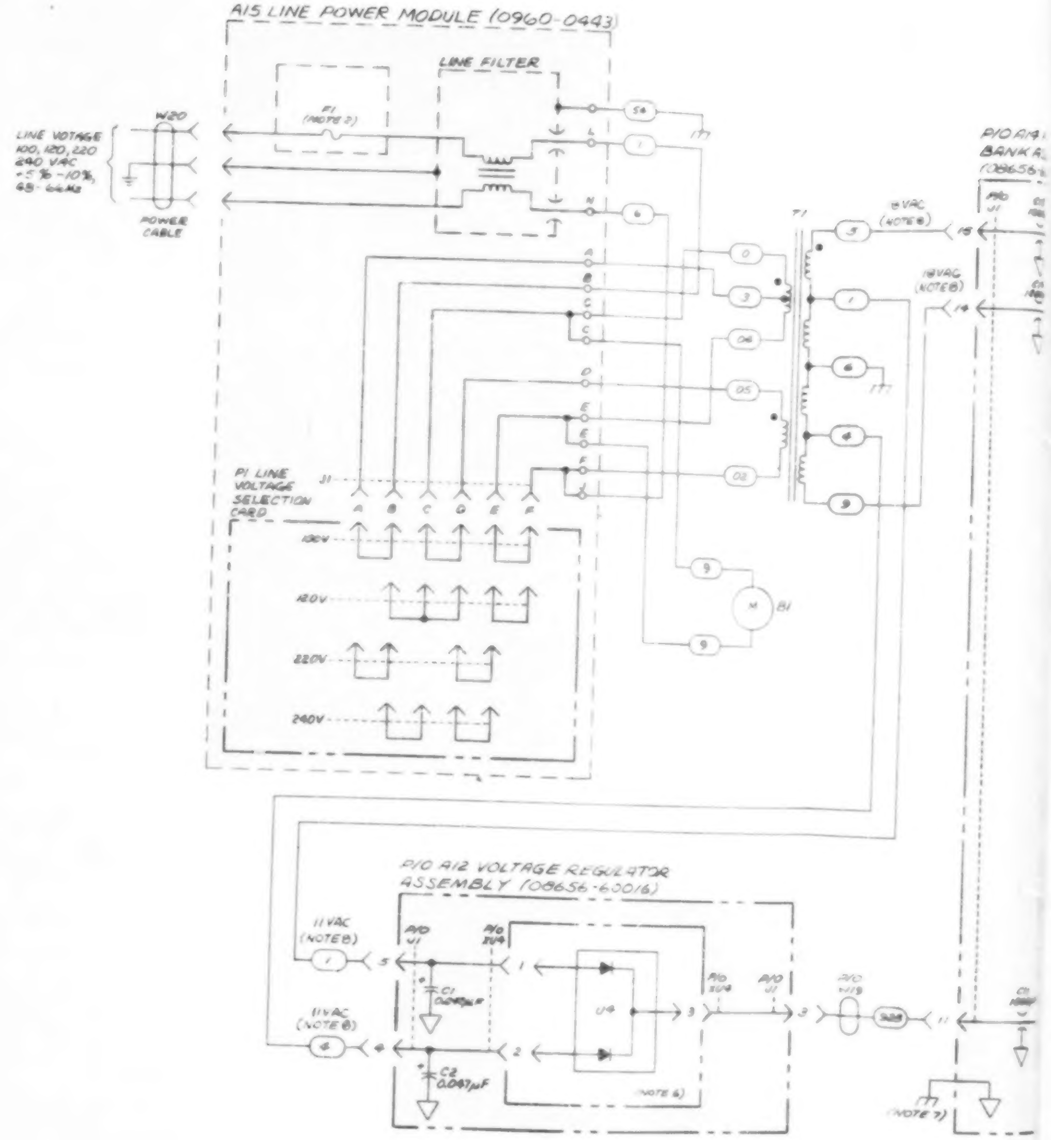

Q3
R79
J2
C24
F3
CR9
CR8
Q12
CR10
CR11
C25
C23
J4
J5
C18
C19
C17
C20
F1
Q1
C22
R63

Figure 8-112. Power Supply (A10 Assembly) Component Locations


A15 LINE POWER MODULE (0960-0443)
LINE FILTER
F1 (NOTE 2)
LINE VOTAGE 100, 120, 220 240 VAC +5% -10%, 48-66Hz
W20
POWER CABLE
P1 LINE VOLTAGE SELECTION CARD
J1
A
B
C
D
E
F
100V
120V
220V
240V
T1
8VAC (NOTE 8)
18VAC (NOTE 8)
B1
P/O A14
BANK A
(08656-
P/O A12 VOLTAGE REGULATOR ASSEMBLY (08656-60016)
11VAC (NOTE 8)
11VAC (NOTE 8)
P/O U1
P/O XU4
U4
C1 0.047μF
C2 0.047μF
(NOTE 6)
P/O W19
(NOTE 7)

WARNING

THIS INSTRUMENT DOES NOT HAVE A PRIMARY POWER SWITCH. THE FOLLOWING VOLTAGES ARE ALWAYS PRESENT WHENEVER THE INSTRUMENT IS CONNECTED TO AN AC OUTLET:

A. LINE VOLTAGE
B. PRIMARY AND SECONDARY AC VOLTAGES.
C. UNREGULATED DC VOLTAGES - (+24V, +15V, +5V AND -15V).
D. REGULATED DC VOLTAGES - (+15V, +5V, AND -15V).

CAUTION

DO NOT CONNECT OR DISCONNECT THE AUDIO/POWER SUPPLY BOARD (A10) OR VOLTAGE REGULATOR BOARD (A12) WITH THE AC POWER CORD CONNECTED, OTHERWISE DAMAGE TO THE INSTRUMENT MAY RESULT.

NOTES

1. SEE TABLE 8-3 FOR SCHEMATIC DIAGRAM NOTES.
2. VALUE OF F1 IS 1.25A SLO-BLO FOR 100/120 VAC, AND 0.6A SLO-BLO FOR 220/240 VAC.
3. A10 CHASSIS GROUND IS ACHIEVED THROUGH A10J5-1 AND 5 CONNECTIONS AND MECHANICAL CONTACT WITH FASTENERS HOLDING PC BOARD TO FRAME.
4. SERVICE TEST POINT. PIN OF DUAL IN-LINE TEST SOCKET J6.
5. A12 CHASSIS GROUND IS ACHIEVED THROUGH MECHANICAL CONTACT WITH FASTENERS HOLDING U1 TO FRAME.
6. CASES OF U2, U3, AND U4 ARE INSULATED FROM CHASSIS GROUND.
7. A14 CHASSIS GROUND IS ACHIEVED THROUGH MECHANICAL CONTACT WITH FASTENERS HOLDING ASSEMBLY TO FRAME.
8. THIS AC VOLTAGE MEASURMENT IS TO CHASEIS GROUND.

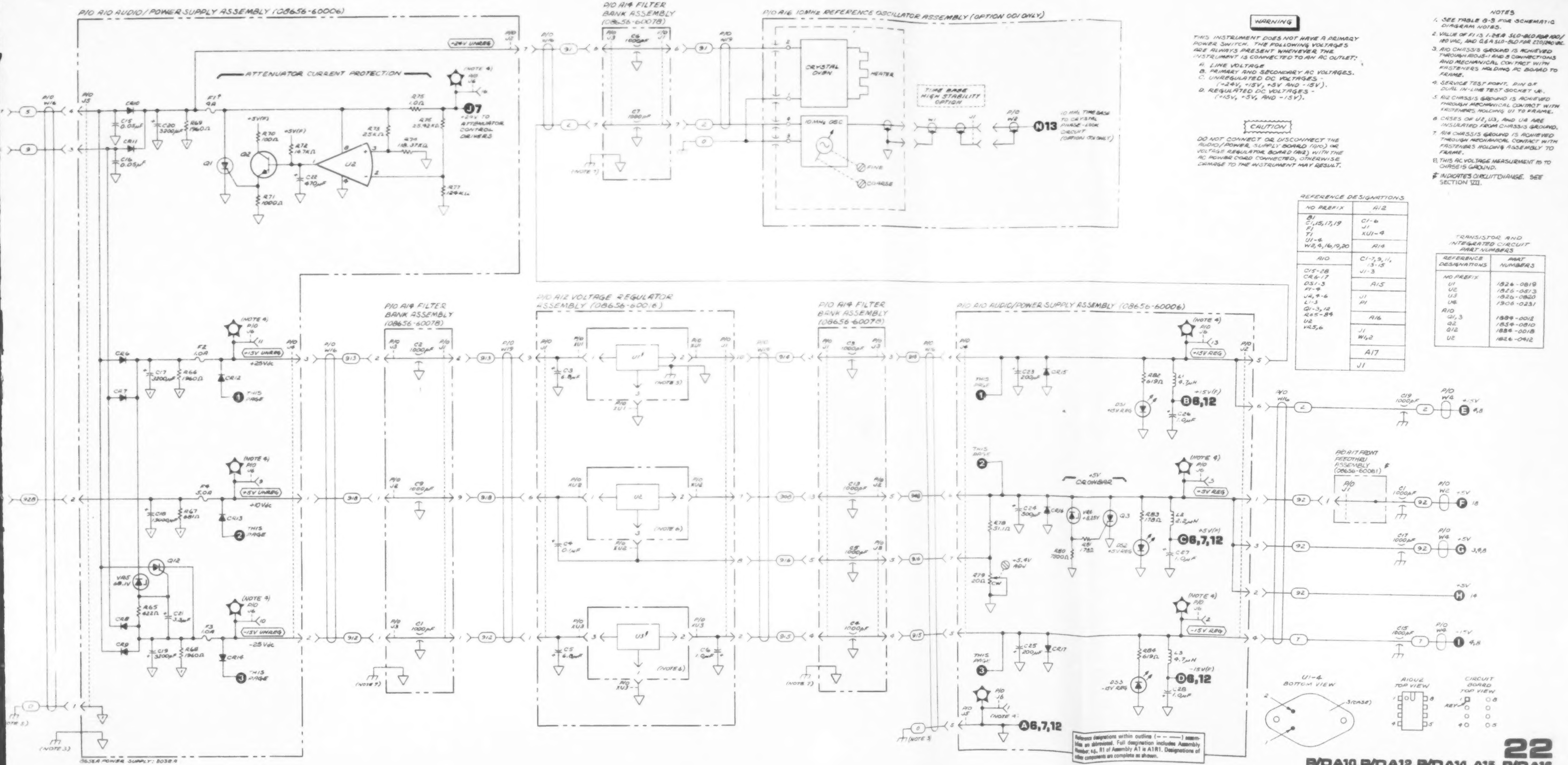
⚡ INDICATES CIRCUIT CHANGE. SEE SECTION VII.

REFERENCE DESIGNATIONS

NO PREFIX	A12
B1 C1,15,17,19 F1 T1 U1-4 W2,4,16,19,20	C1-6 J1 XU1-4
A10	A14
C15-28 CR6-17 DS1-3 F1-4 J2,4-6 L1-3 Q1-3,12 R65-84 U2 VR5,6	C1-7,9,11,13-15 J1-3
	A15
	J1 P1
	A16
	J1 W1,2
	A17
	J1

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
NO PREFIX	
U1	1826-0819
U2	1826-0513
U3	1826-0820
U4	1906-0231
A10	
Q1,3	1884-0012
Q2	1854-0810
Q12	1884-0018
U2	1826-0412


P/O A10 AUDIO/POWER SUPPLY ASSEMBLY (08656-60006)
ATTENUATOR CURRENT PROTECTION
+24V UNREG
+24V TO ATTENUATOR CONTROL DRIVERS
P/O A14 FILTER BANK ASSEMBLY (08656-60078)
P/O A16 10MHz REFERENCE OSCILLATOR ASSEMBLY (OPTION 001 ONLY)
CRYSTAL OVEN
HEATER
10 MHz OSC
FINE
COARSE
TIME BASE HIGH STABILITY OPTION
10 MHz TIME BASE TO CRYSTAL PHASE-LOCK CIRCUIT (OPTION 001 ONLY)
P/O A12 VOLTAGE REGULATOR ASSEMBLY (08656-60018)
+15V UNREG
+25Vdc
+5V UNREG
+10Vdc
-15V UNREG
-25Vdc
THIS PAGE
+15V REG
+5V REG
-15V REG
+5V CROWBAR
P/O A17 FRONT FEEDTHRU ASSEMBLY (08656-60081)
U1-4 BOTTOM VIEW
3(CASE)
A10U2 TOP VIEW
CIRCUIT BOARD TOP VIEW
KEY
8656A POWER SUPPLY: 8038A

Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

22

P/O A10, P/O A12, P/O A14, A15, P/O A16

Figure 8-113. Power Supply Schematic Diagram

APPENDIX A

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms.
DA Pam 738-750	The Army Maintenance Management System (TAMMS).
TM 11-6625-3062-24P	Organizational, Direct Support and General Support Maintenance Manual, Repair Parts and Special Tools List for Signal Generator, HP Model 8656A
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command).

APPENDIX B
COMPONENTS OF END ITEM LIST

Section I. INTRODUCTION

B-1. Scope

This appendix lists integral components of and basic issue items for the Signal Generator to help you inventory items required for safe and efficient operation.

B-2. General

This Components of End Item List is divided into the following sections:

a. Section II. Integral Components of the End Item. These items, when assembled, comprise the Signal Generator and must accompany it whenever it is transferred or turned in. The illustrations will help you identify these items.

b. Section III. Basic Issue Items. Not applicable.

B-3. Explanation of Columns

a. Illustration. This column is divided as follows:

(1) *Figure number.* Indicates the figure number of the illustration on which the item is shown.

(2) *Item number.* The number used to identify item called out in the illustration.

b. National Stock Number. Indicates the National stock number assigned to the item and which will be used for requisitioning.

c. Part Number. Indicates the primary number used by the manufacturer, which controls the design and characteristics of the item by means of its engineering drawings, specifications, standards, and inspection requirements to identify an item or range of items. Following the part number, the Federal Supply Code for Manufacturers (FSCM) is shown in parentheses.

d. Description. Indicates the Federal item name and, if required, a minimum description to identify the item.

e. Location. The physical location of each item listed is given in this column. The lists are designed to inventory all items in one area of the major item before moving on to an adjacent area.

f. Usable on Code. Not applicable.

g. Quantity Required (Qty Reqd). This column lists the quantity of each item required for a complete major item.

h. Quantity. This column is left blank for use during an inventory. Under the Rcvd column, list the quantity you actually receive on your major item. The Date columns are for your use when you inventory the major item at a later date; such as for shipment to another site.

(Next printed page is B-2)

SECTION II INTEGRAL COMPONENTS OF END ITEM

(1) ILLUSTRATION		(2) NATIONAL STOCK NUMBER	(3) DESCRIPTION		(4) LOCATION	(5) USABLE ON CODE	(6) QTY REQD	(7) QUANTITY	
(A) FIG NO.	(B) ITEM NO.		PART NUMBER	(FSCM)				RCVD	DATE
			SIGNAL GENERATOR MODEL HP-8656A						

APPENDIX D
MAINTENANCE ALLOCATION

Section I. INTRODUCTION

D-1. General

This appendix provides a summary of the maintenance operations for Signal Generator. It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

D-2. Maintenance Function

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/-operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

D-3. Column Entries

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2. Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate "work time" figures will be shown for each category. The number of task-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C - Operator/Crew
O - Organizational

F - Direct Support
H - General Support
D - Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

D-4. Tool and Test Equipment Requirements (Sect. III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

D-5. Remarks (Sect. IV)

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II.

(Next printed page is D-3)

SECTION II MAINTENANCE ALLOCATION CHART FOR

SIGNAL GENERATOR HP8656A

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQPT.	(6) REMARKS
			C	O	F	H	D		
00	SIGNAL GENERATOR HP-8656A MTBF 19,084	INSPECT			0.1				
		TEST			0.7			17	C,D
		TEST				4.1		1-13,21	A
		TEST					4.1		
		CALIBRATE				5.7		1,8-17 19	A
		REPLACE			0.1				
		REPAIR				10.		6-18	A,B
		REPAIR					10.		
01	DISPLAY ASSY 08656-6009 A2	TEST					1.0		
		REPLACE				0.6		8	E
		REPAIR					4.0		
01	LOW FREQ LOOP ASSY 08656-60003 A3	TEST					1.0		
		REPLACE				0.5		8	
		REPAIR					4.0		
03	HI FREQ LOOP ASSY 08656-60001 A4	TEST					1.0		
		REPLACE				0.5		8	
		REPAIR					4.0		
04	OUTPUT ASSY 08656-60118 A6	TEST					1.0		
		REPLACE				0.5		8	E
		REPAIR					4.0		
05	FREQ MULT ASSY 08656-60004 A8	TEST					1.0		
		REPLACE				0.5		8	E
		REPAIR					4.0		
06	ATTENTUATOR ASSY 08656-60018 A9	TEST					1.0		
		REPLACE				0.5		8	
		REPAIR					4.0		
07	AUDIO/PS ASSY 08656-60006 A10	TEST					1.0		
		REPLACE				0.5		8	
		REPAIR					4.0		
08	MICROP/MEM ASSY 08656-60121 A11	TEST					1.0		
		REPLACE				0.5		8	
		REPAIR					4.0		
09	10 MHZ REF OSC 0950-0411 A16	TEST					1.0		
		REPLACE				0.5		8	E
		REPAIR					4.0		

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS FOR SIGNAL GENERATOR HP8656A

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
1	H	MODULATION ANALYZER	6625-01-081-4156	HP8901A
2	H	AM/FM TEST SOURCE	4931-01-088-2149	HP11715A
3	H	ATTENUATOR, FIXED	5985-00-167-0544	HP8491A/OP56
4	H	LOOP ANTENNA		008640-60501
5	H	AMPLIFIER, WIDEBAND	6625-01-065-0305	HP8447D/OP10
6	H	DISTORTION ANALYZER	6625-01-087-7285	HP339A
7	H	TEST OSCILLATOR	6625-00-937-4961	HP651B
8	H,F	TOOL KIT, ELECTRICIANS	5180-00-610-8177	TK-105G
9	H	DIGITAL MULTIMETER	6625-01-039-7922	HP3465A
11	H	POWER METER	6625-01-033-5050	HP436A/OP22
12	H	POWER SENSOR	6625-01-028-2882	HP8484A
13	H	SPECTRUM ANALYZER		HP8558
14	H	SPECTRUM ANALYZER	6625-01-128-7868	HP8568A
15	H	CONTROLLER	7420-01-026-1686	HP9825A
16	H	OSCILLOSCOPE		HP1801A
17	H	SIGNAL SOURCE	5963-01-137-5713	HP8640A
18	H,F	FREQUENCY COUNTER		HP5328/OP31
19	H	SIGNATURE ANALYZER	6625-01-049-8516	HP5004A
20	H	ATTENUATOR, FIXED	5985-00-167-0543	HP8491A/OP20
21	H	PLIERS, SOFT JAWED		HP8710-0986
22	H,F	SCREWDRIVER, POZIDRIV		

SECTION IV. REMARKS

REFERENCE CODE	REMARKS
A	TEST, REPAIR, AND CALIBRATE BY USATSG AT GENERAL SUPPORT.
B	REPAIR CONSISTS OF REPLACEMENT OF SUBASSEMBLIES AND MAINFRAME COMPONENTS AS REQUIRED.
C	OPERATOR CHECKS PERFORMED AT DIRECT SUPPORT LEVEL. DOES NOT CHECK ALL SPECIFICATION PARAMETERS.
D	IN-SYSTEM CHECK TO VERIFY HP-IP BUS INTERFACE OPERATION DEPENDS UPON SYSTEM IN WHICH UNIT IS INSTALLED. SOFTWARE CONTROLLED BY SYSTEM CONTROL UNIT.
E	ITEMS A1, A5, A7, A12 THRU A15, A17, B1, FL1, T1, AND W1-W21 ARE THROW-AWAYS.

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Stateside Army pot
ATTN: AMSTA-US
Stateside, N.J. 07703-5007

DATE SENT 4 April 1978

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5840-340-14&P	23 Jan 74	Radar Set AN/PRC-76

BE EXACT. . PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO	
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
E-5				For item 2, change the NSN to read: 5835-00-134-9186. REASON: Accuracy.
E-8		E-3		Identify the cover on the junction box (item no. 5). REASON: It is a separate item and is not called out on figure 19.
E-9				Add the cover of the junction box as an item in the listing for figure 19. REASON: Same as above.

SAMPLE

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER	SIGN HERE
SSG I. M. DeSpiritof 999-1776	SSG I.M. DeSpiritof

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